	Hits	Search Text	DBs
1	8028	((345/30,50,55,87-89,92,98-100) or (315/169.1,169.3,169.4) or (361/278,283.1) or (257/444) or (340/525/438/75) or (348/249,294-324,332) or (356/478)).CCLS.	USPAT; US-PGPUB
2	221	(((345/30,50,55,87-89,92,98-100) or (315/169.1,169.3,169.4) or (361/278,283.1) or (257/444) or (340/525/438/75) or (348/249,294-324,332) or (356/478)).CCLS.) and (activ$2 adj2 matrix adj2 device)	USPAT; US-PGPUB
3	50	((((345/30,50,55,87-89,92,98-100) or (315/169.1,169.3,169.4) or (361/278,283.1) or (257/444) or (340/525/438/75) or (348/249,294-324,332) or (356/478)).CCLS.) and (activ$2 adj2 matrix adj2 device)) and (DAC D/A (digital adj5 analog adj2 convert$3))	USPAT; US-PGPUB
4	9152	((345/1,9,30,50,55,67,87-89,90-93,98-100,147,149,197,204,208,694,696) or (315/169.1,169.3,169.4) or (361/278,283.1) or (257/444) or (340/525/438/75) or (348/249,294-324,332) or (356/478) or (745/98,100)).CCLS.	USPAT; US-PGPUB
5	9152	((345/1,9,30,50,55,67,87-89,90-93,98-100,147,149,197,204,208,694,696) or (315/169.1,169.3,169.4) or (361/278,283.1) or (257/444) or (340/525/438/75) or (348/249,294-324,332) or (356/478) or (745/98,100)).CCLS.	USPAT; US-PGPUB
6	57	(((345/1,9,30,50,55,67,87-89,90-93,98-100,147,149,197,204,208,694,696) or (315/169.1,169.3,169.4) or (361/278,283.1) or (257/444) or (340/525/438/75) or (348/249,294-324,332) or (356/478) or (745/98,100)).CCLS.) and ((DAC D/A (digital adj5 analog adj2 convert$5)) same substrat$2)	USPAT; US-PGPUB
7	857	((DAC D/A (digital adj5 analog adj2 convert$5)) same substrat$2)	USPAT; US-PGPUB
8	398	((DAC D/A (digital adj5 analog adj2 convert$5)) with substrat$2)	USPAT; US-PGPUB
9	122	((DAC D/A (digital adj5 analog adj2 convert$5)) with substrat$2)	EPO; JPO; DERWENT; IBM_TDB

US006049321A

United States Patent [19]

Sasaki

[11] Patent Number: 6,049,321

[45] Date of Patent: Apr. 11, 2000

[54] **LIQUID CRYSTAL DISPLAY**

[75] Inventor: **Minoru Sasaki**, Tokyo, Japan

[73] Assignee: **Kabushiki Kaisha Toshiba**, Kawasaki, Japan

[21] Appl. No.: **08/938,333**

[22] Filed: **Sep. 25, 1997**

[30] **Foreign Application Priority Data**

Sep. 25, 1996 [JP] Japan 8-253547
Jul. 11, 1997 [JP] Japan 9-186151

[51] **Int. Cl.**[7] **G09G 3/36**

[52] **U.S. Cl.** **345/99**; 345/98; 345/100; 345/96

[58] **Field of Search** 345/99, 98, 100, 345/209, 92, 96, 205, 206, 94, 88

[56] **References Cited**

U.S. PATENT DOCUMENTS

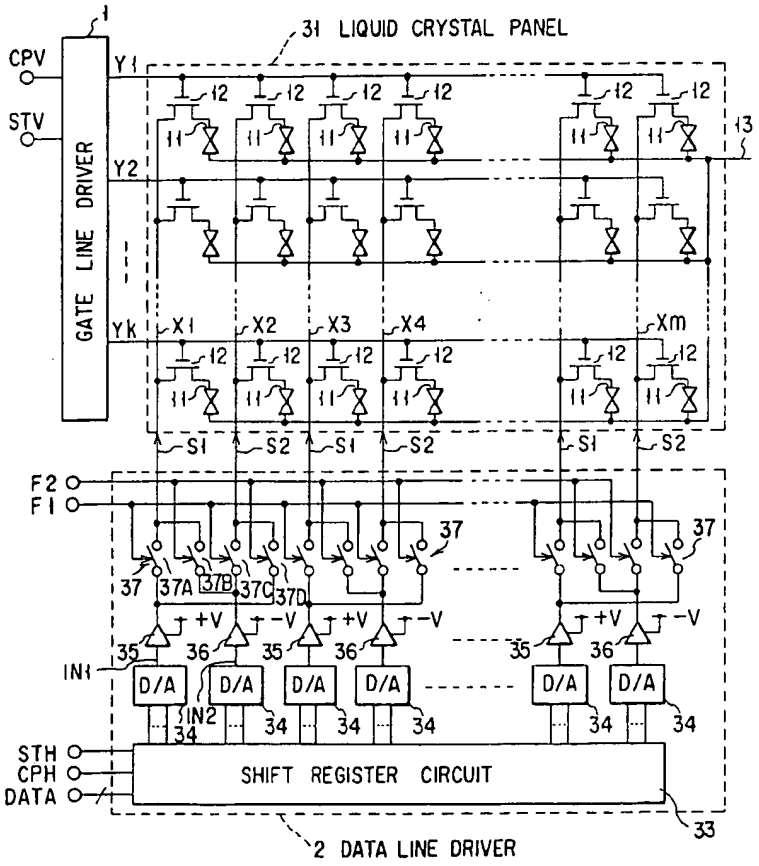
5,602,561 2/1997 Kawaguchi et al. 345/99
5,748,165 5/1998 Kubota et al. 345/96

Primary Examiner—Richard A. Hjerpe
Assistant Examiner—Francis Nguyen
Attorney, Agent, or Firm—Pillsbury Madison & Sutro LLP

[57] **ABSTRACT**

A liquid crystal display includes a matrix array of liquid crystal pixels, data lines formed along columns of the pixels, TFTs assigned to the pixels for causing the data lines to be electrically connected to the pixels of a selected row, and a data line driver which drives the data lines and has a first video bus for transmitting analog pixel signals of the positive polarity for the pixels of one of odd and even columns in a selected row, a second video bus for transmitting analog pixel signals of the negative polarity for the pixels of the other one of the odd and even columns in the selected row, sample-hold units each assigned to adjacent two of the data lines to simultaneously sample-hold the pixel signals on the first and second video buses, and a shift register circuit for enabling the operations of the sample-hold units sequentially. Particularly, each sample-hold unit has a first switch circuit for causing the first and second video buses to be connected to one of the adjacent two data lines and the other one of the adjacent two data lines, and a second switch circuit for causing the first and second video buses to be connected to the other one of the adjacent two data lines and the one of the adjacent two data lines, and the shift register circuit has a logic circuit for periodically switching between the first and second switch circuits of each sample-hold unit.

17 Claims, 9 Drawing Sheets



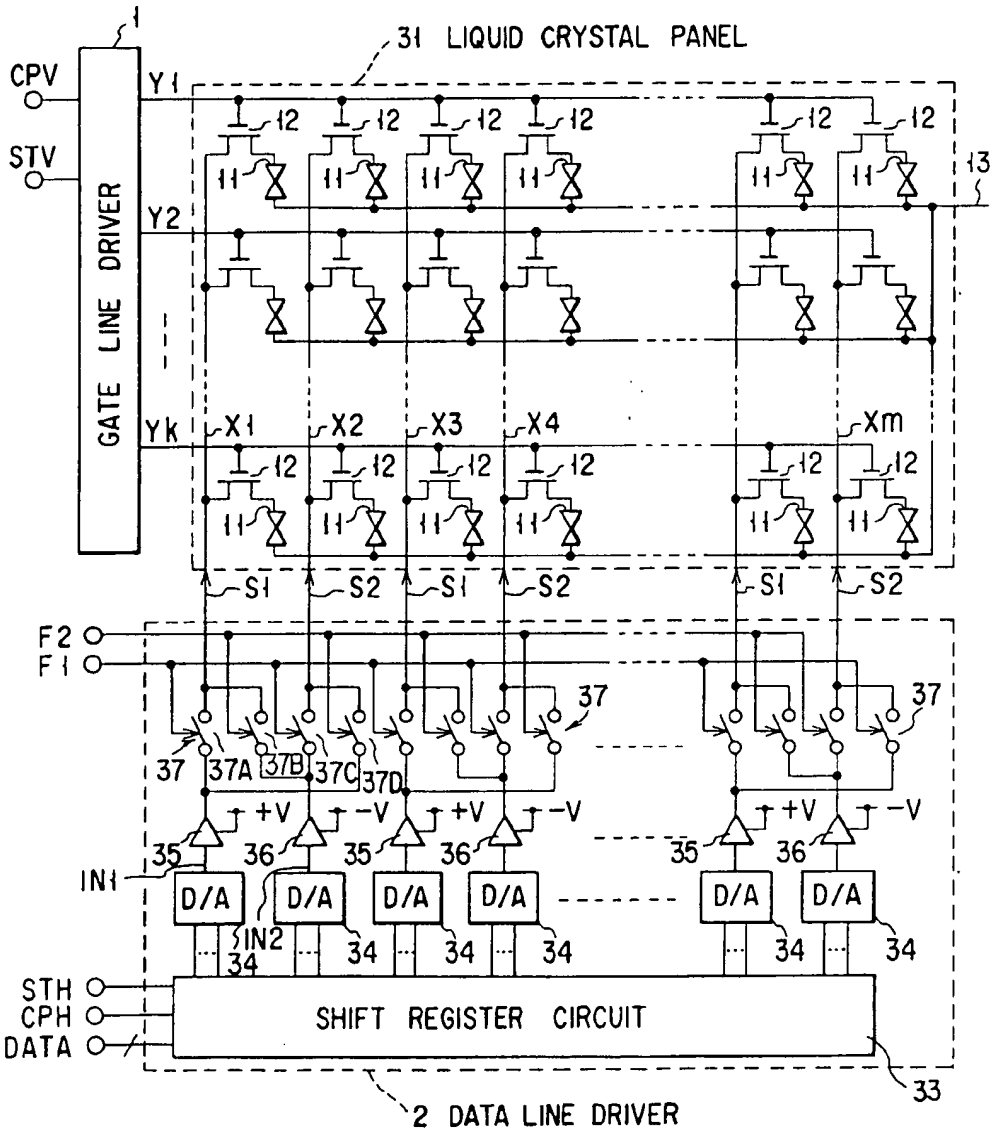

1
31 LIQUID CRYSTAL PANEL
CPV
STV
GATE LINE DRIVER
Y1
Y2
Yk
X1
X2
X3
X4
Xm
11
12
13
S1
S2
F2
F1
37
37A
37B
37C
37D
+V
-V
35
36
IN1
IN2
D/A
34
STH
CPH
DATA
SHIFT REGISTER CIRCUIT
33
2 DATA LINE DRIVER

FIG. 1

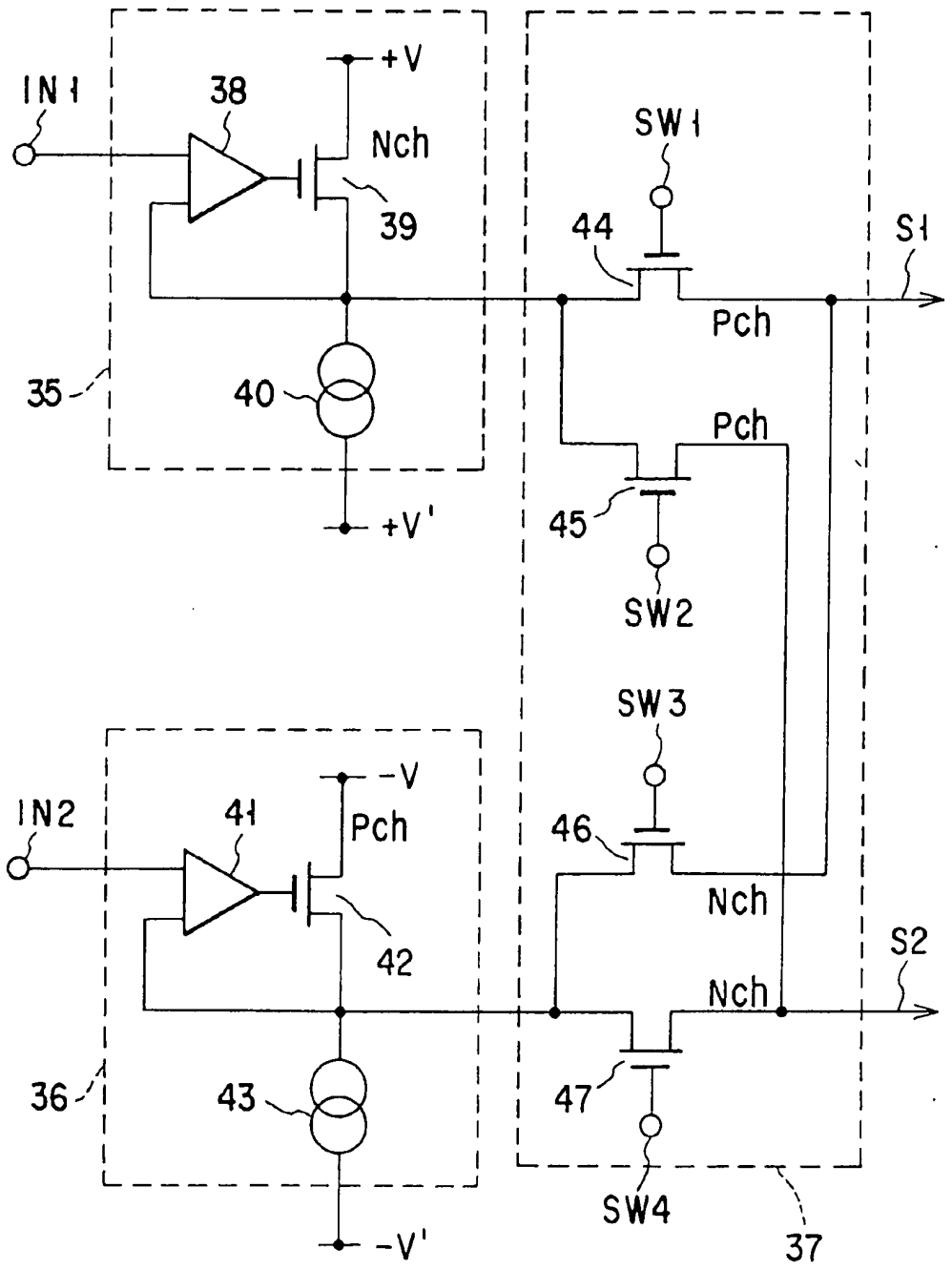

IN1
38
+V
Nch
39
SW1
44
S1
Pch
35
40
Pch
45
+V'
SW2
SW3
IN2
41
-V
Pch
46
Nch
S2
42
Nch
36
43
47
SW4
37
-V'

FIG. 2

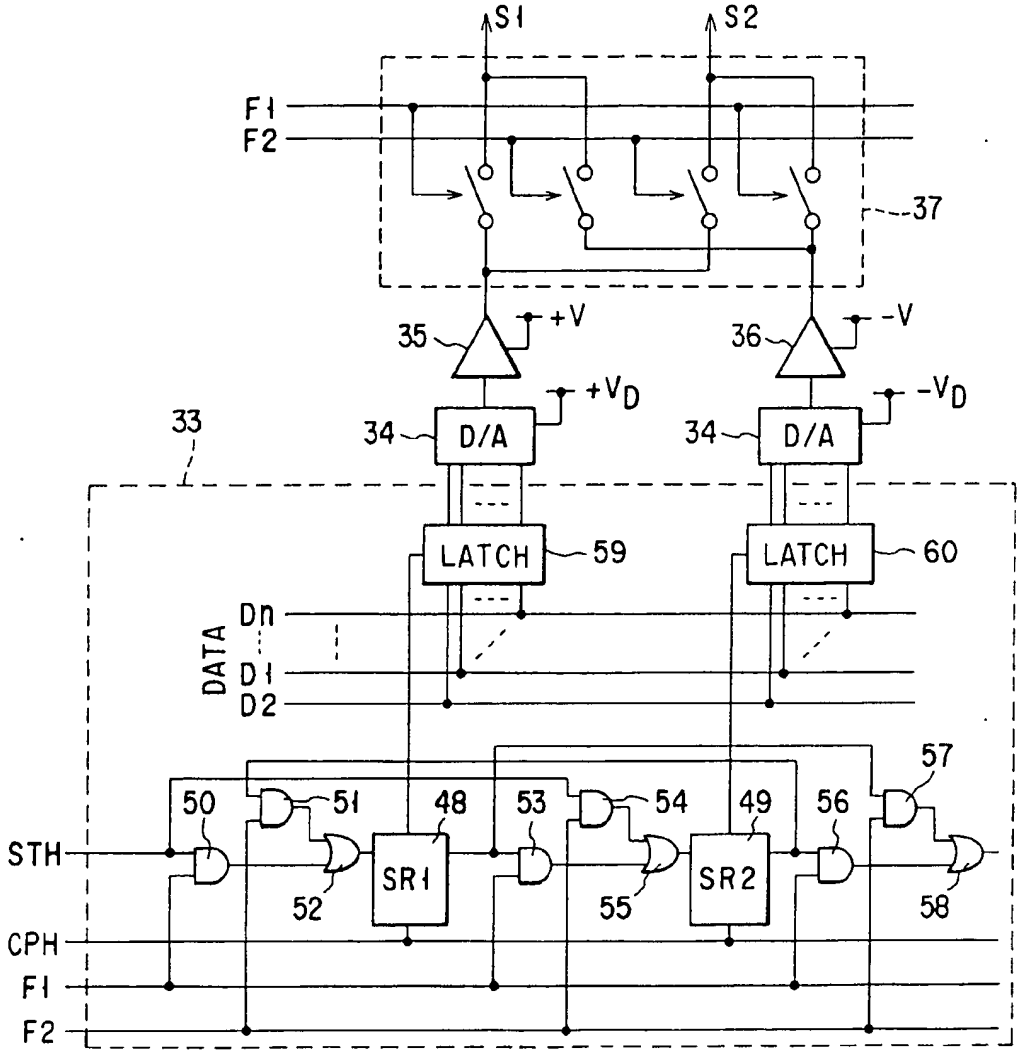

S1
S2
F1
F2
37
35
+V
36
-V
+VD
-VD
33
34
D/A
34
D/A
LATCH
59
LATCH
60
Dn
DATA
D1
D2
57
50
51
48
53
54
49
56
STH
52
SR1
55
SR2
58
CPH
F1
F2

FIG. 3

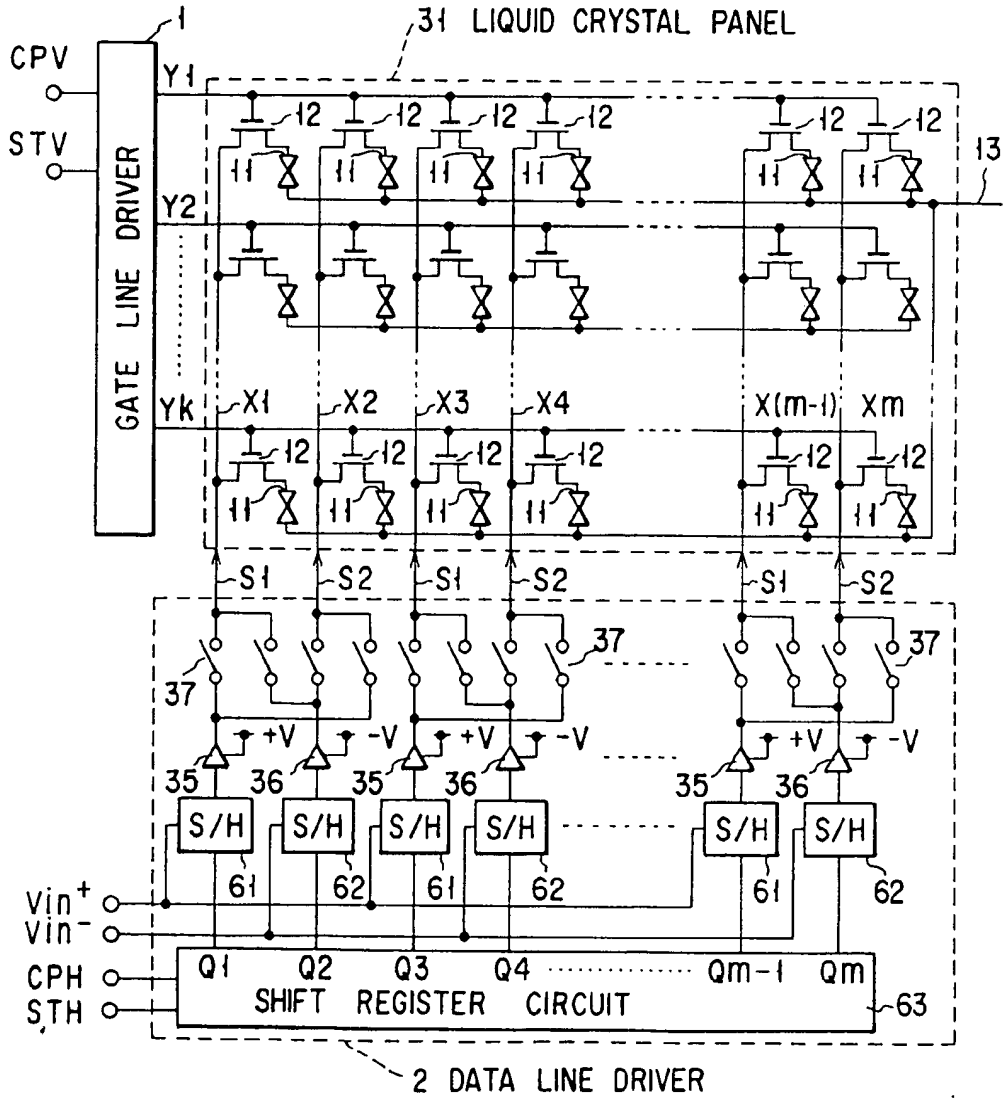

1
31 LIQUID CRYSTAL PANEL
CPV
STV
GATE LINE DRIVER
Y1
Y2
Yk
X1
X2
X3
X4
X(m-1)
Xm
11
12
13
S1
S2
37
+V
-V
35
36
S/H
61
62
Vin+
Vin-
CPH
STH
Q1
Q2
Q3
Q4
Qm-1
Qm
SHIFT REGISTER CIRCUIT
63
2 DATA LINE DRIVER

FIG. 4

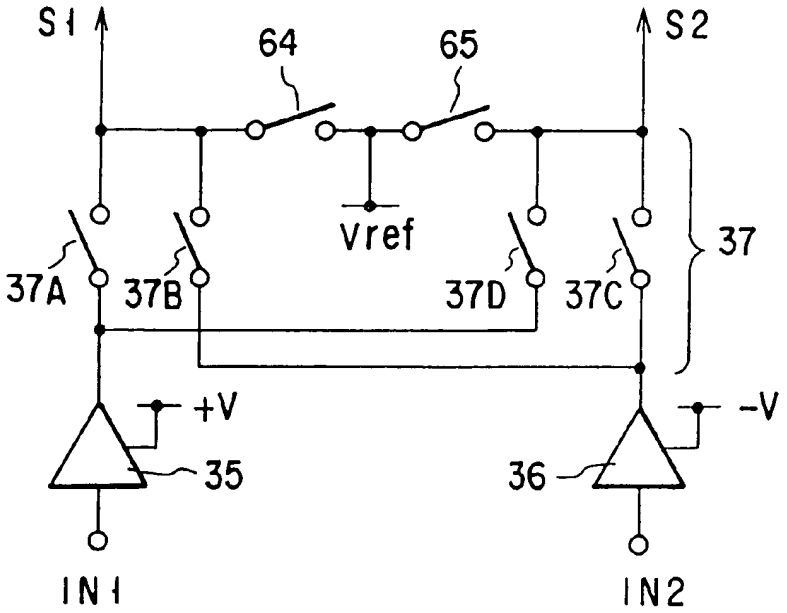

S1
S2
64
65
Vref
37
37A
37B
37D
37C
+V
-V
35
36
IN1
IN2

FIG. 5

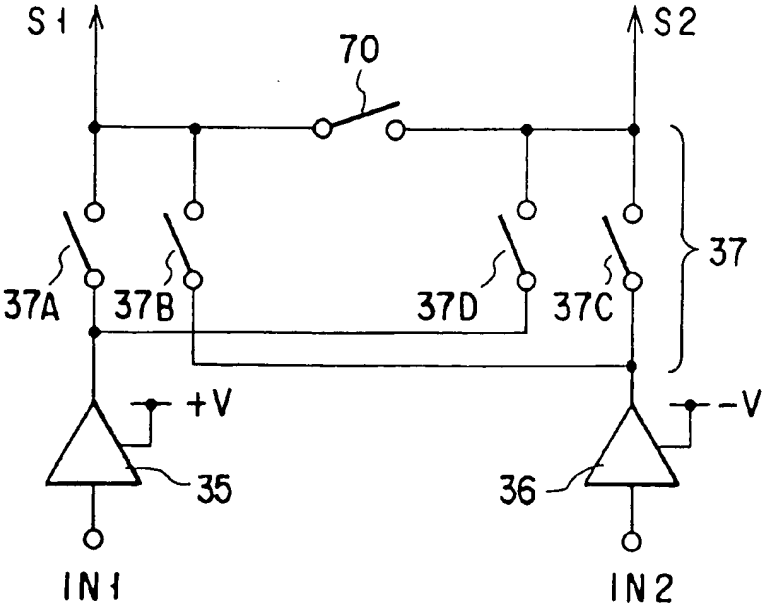

S1
S2
70
37
37A
37B
37D
37C
+V
-V
35
36
IN1
IN2

FIG. 6

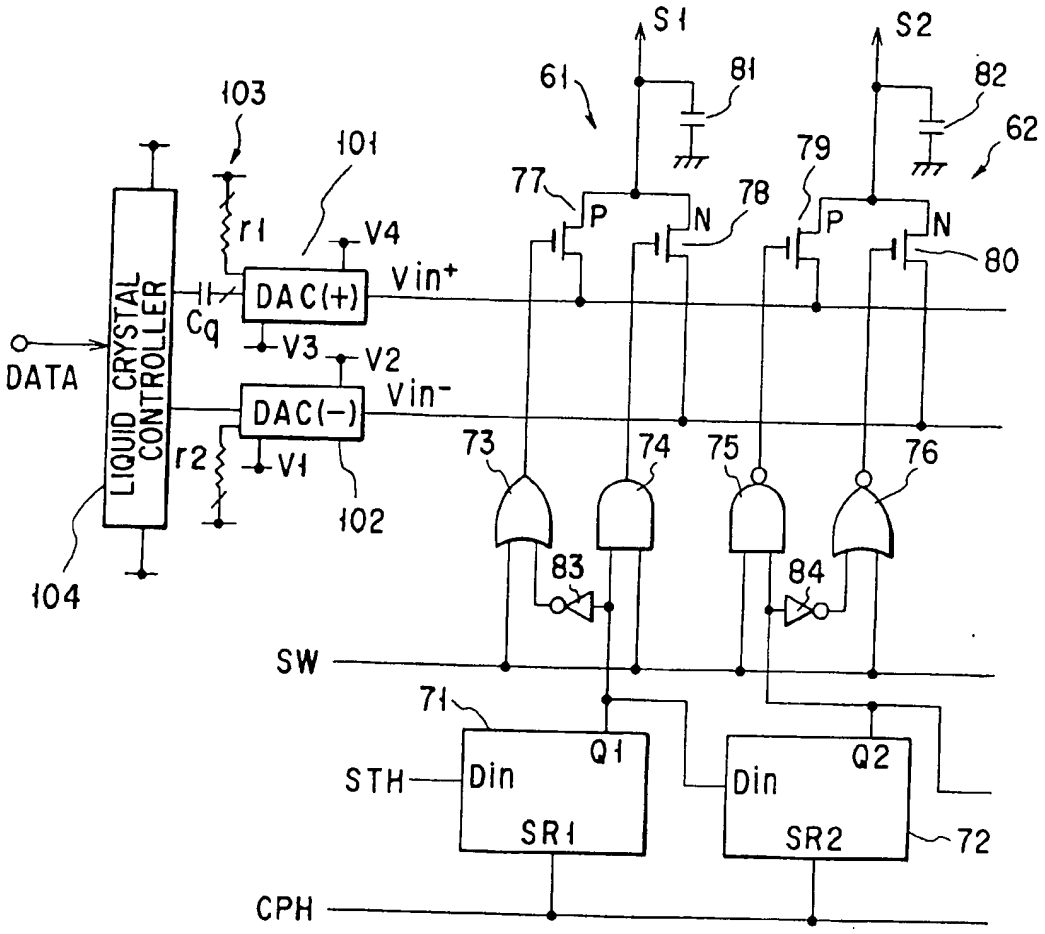

S1
S2
61
81
82
62
103
101
79
77
78
P
N
r1
V4
Vin+
80
DAC(+)
Cq
V3
V2
DATA
LIQUID CRYSTAL CONTROLLER
DAC(-)
Vin-
73
74
75
76
r2
V1
102
104
83
84
SW
71
Q1
Q2
STH
Din
SR1
SR2
72
CPH

FIG. 7

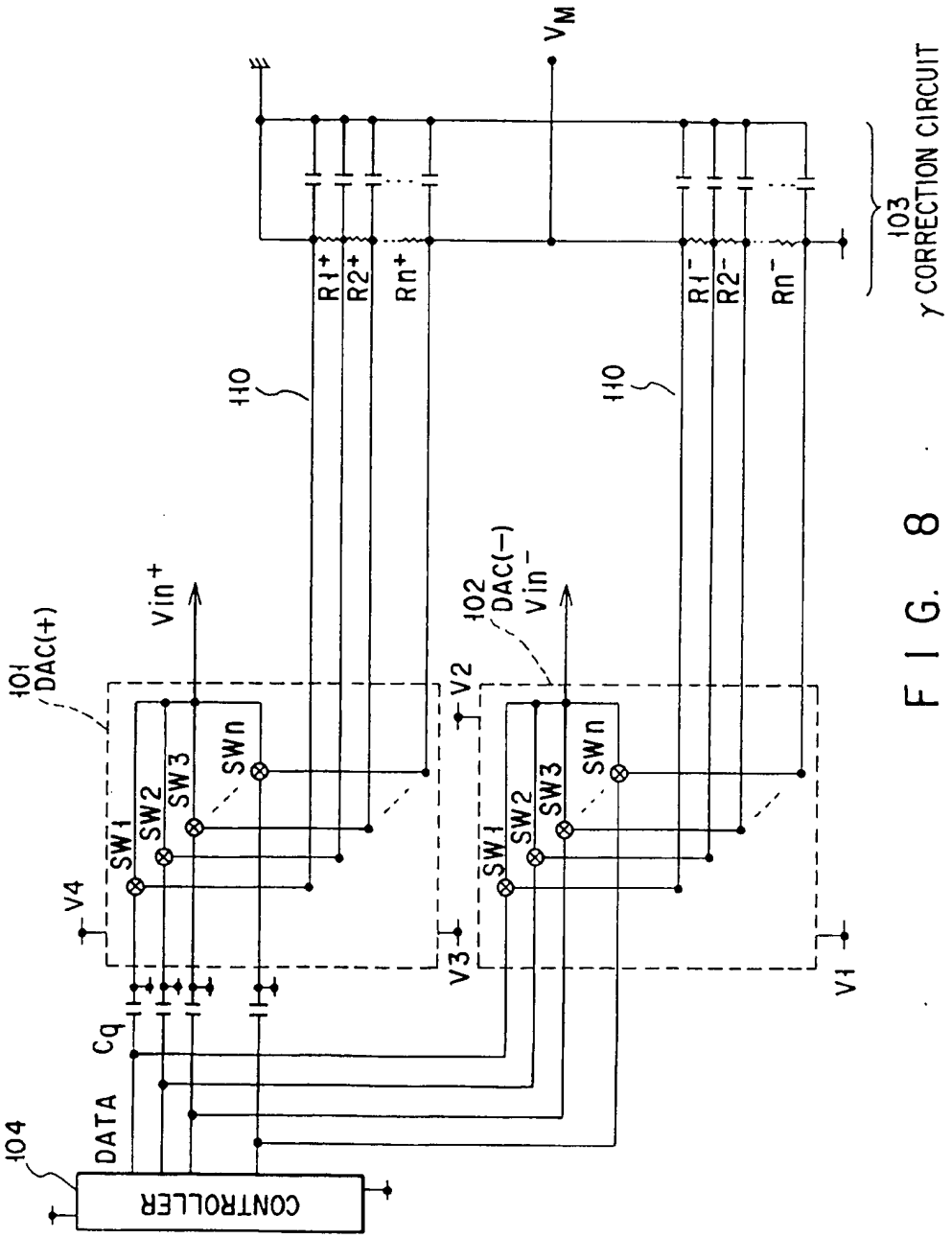

VM
R1+
R2+
Rn+
R1-
R2-
Rn-
103
γ CORRECTION CIRCUIT
110
110
101
DAC(+)
Vin+
102
DAC(-)
Vin-
V2
V4
V3
V1
SW1
SW2
SW3
SWn
Cq
DATA
104
CONTROLLER

FIG. 8

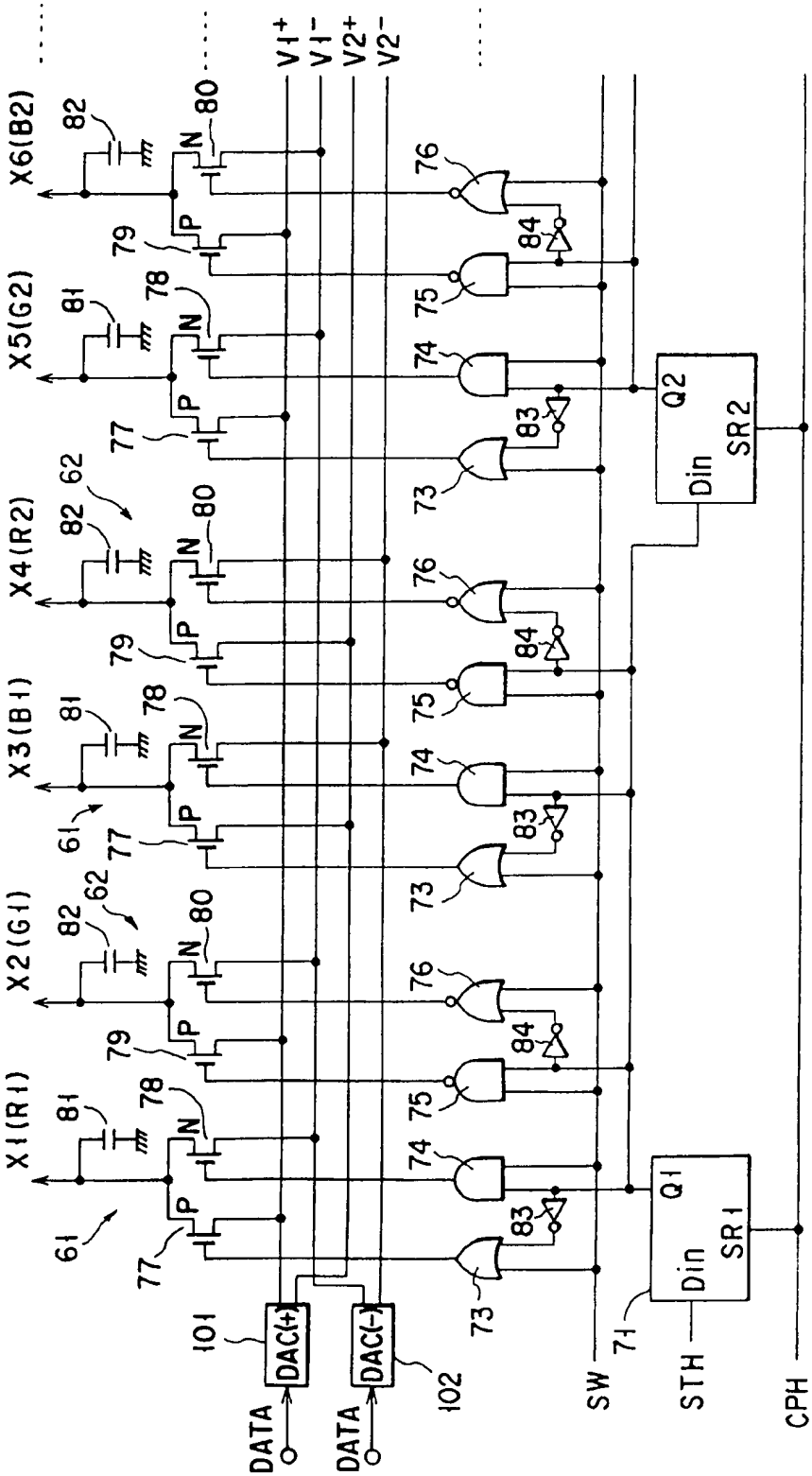

V1+
V1-
V2+
V2-
X6(B2)
X5(G2)
X4(R2)
X3(B1)
X2(G1)
X1(R1)
82
81
62
61
80
78
79
77
76
75
74
73
84
83
Q2
SR2
Q1
SR1
Din
101
102
DAC(+)
DAC(-)
DATA
DATA
SW
71
STH
CPH

FIG. 9

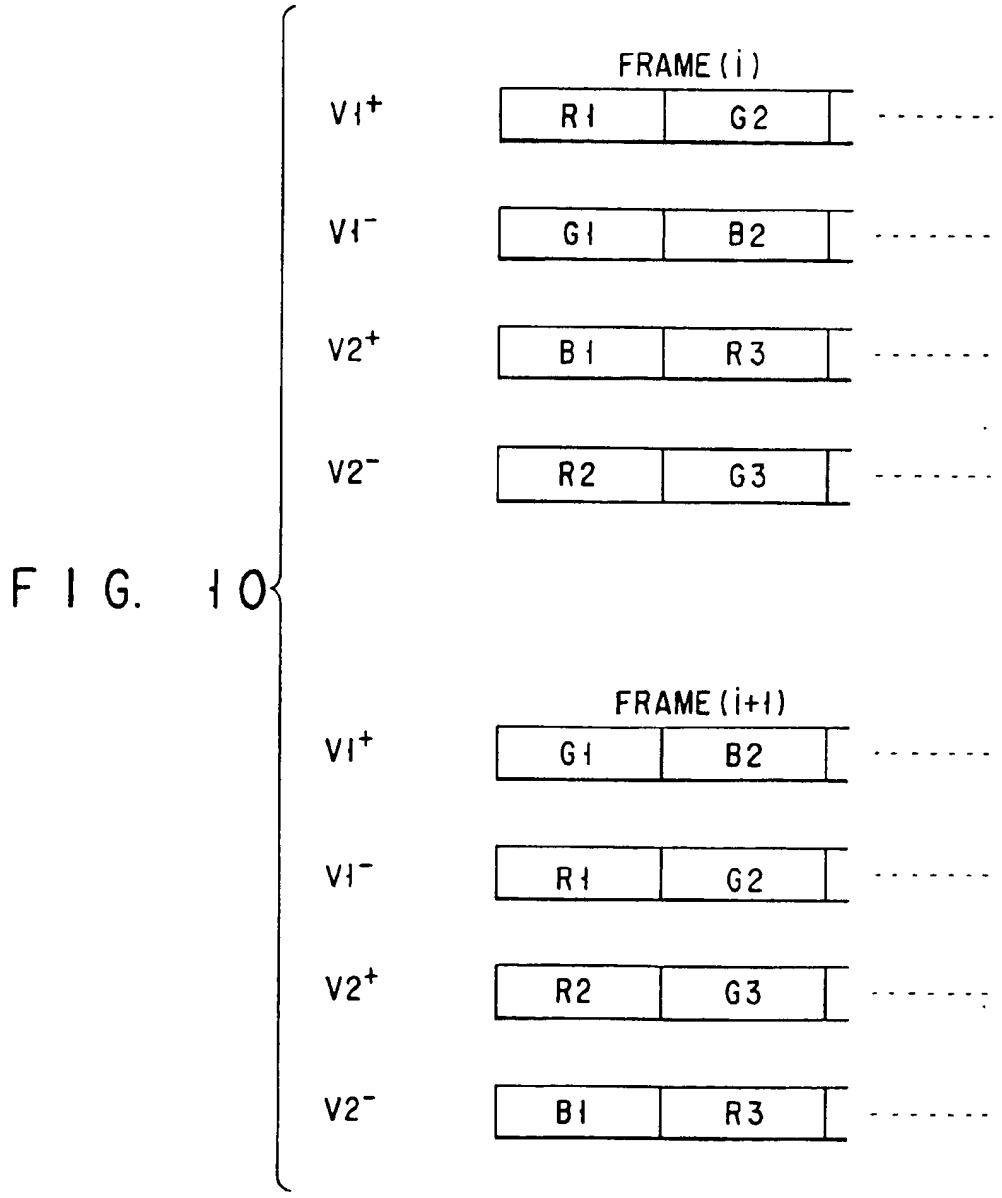

FRAME (i)
V1+
R1
G2
V1-
G1
B2
V2+
B1
R3
V2-
R2
G3
FRAME (i+1)
V1+
G1
B2
V1-
R1
G2
V2+
R2
G3
V2-
B1
R3

FIG. 10

LIQUID CRYSTAL DISPLAY

BACKGROUND OF THE INVENTION

The present invention relates to a flat-panel display used as an image monitor for a computer and a television receiver and particularly to a liquid crystal display driven by a signal voltage whose polarity is periodically reversed.

In recent years, liquid crystal displays have been widely used in views of merits of thickness, light weight, and low power consumption. The liquid crystal display has a structure in which a liquid crystal layer is held between an array substrate and a counter substrate. Each of the array substrate and the counter substrate, for example, has a light transmitting and insulating property, and the liquid crystal layer is made of liquid crystal composition filled into a gap between the array substrate and the counter substrate. The array substrate comprises a matrix array of pixel electrodes, a plurality of scanning lines formed along columns of the pixel electrodes, a plurality of signal lines formed along rows of the pixel electrode, and a first alignment film covering the entire matrix array of pixel electrodes. The scanning lines serve to select the corresponding rows of the pixel electrodes, and the signal lines serve to apply pixel electrode signal voltages to the pixel electrodes of the selected row. The counter substrate has a counter electrode facing the matrix array of pixel electrodes, and a second alignment film covering the entire counter electrode. The first and second alignment films are provided for causing liquid crystal molecules of the liquid crystal layer to be set in a twisted nematic (TN) alignment when no potential difference exists between the pixel electrode and the counter electrode. When light is incident to the liquid crystal layer from one substrate side through a polarizing plate, light rotates along the twist of the liquid crystal molecules aligned in the thickness direction of the liquid crystal layer, so as to be guided to the other substrate, and selectively transmitted through a polarizing plate. If a potential difference is provided between the pixel electrode and the counter electrode, the molecules are tilted up by an angle, which is proportional to the potential difference, from the plane parallel to the substrate surface where an image is displayed. As a result, light transmittance is changed.

In an active matrix liquid crystal display, a plurality of thin film transistors (TFT) are respectively formed near intersections of the scanning lines (or gate lines) and the signal line (or data lines), and each used as a switching element for selectively driving the corresponding pixel electrode. Each TFT has a gate connected to one scanning line, and a source-drain path connected between one signal line and one pixel electrode. The TFT is turned on in response to a rise of a scanning pulse from the scanning line, and supplies the pixel signal voltage to the pixel electrode from the signal line. The pixel electrode and the counter electrode are associated with the liquid crystal layer to constitute a liquid crystal capacitance to be charged according to the potential difference between these electrodes. This potential difference is maintained by the liquid crystal capacitance even after the TFT is turned off in response to a fall of the scanning pulse.

In a case where the electric field is kept in the same direction, materials other than the liquid crystal tend to gather one electrode side, thereby causing the life of the liquid crystal layer to be shortened. Conventionally, a technique of reversing the polarity of the pixel signal voltage with respect to the potential of the counter electrode every one frame period, for example, is known as a solution of the problem. If the polarity of the pixel signal voltage is reversed in the same manner for all the pixel electrodes during the frame period, this causes generation of flickers which deteriorate the image quality. To reduce the flickers, there is used a drive method of driving adjacent columns of the pixel electrodes by the pixel signal voltages of the different polarities. For example, for a certain frame period, pixel signal voltages of the negative polarity are applied to the pixel electrodes connected to the even-numbered signal lines, and signal voltages of the positive polarity are applied to the pixel electrodes connected to the odd-numbered signal lines. For a next frame period, pixel signal voltages of the negative polarity are applied to the pixel electrodes connected to the odd-numbered signal lines, and pixel signal voltages of the positive polarity are applied to the pixel electrodes connected to the even-numbered signal lines.

There is also known a drive method of further driving adjacent rows of the pixel electrodes by pixel signal voltages of the different polarities. For each frame period, pixel signal voltages of the positive polarity are applied to the odd rows of the pixel electrodes connected to the odd-numbered signal lines, and the even rows of the pixel electrodes connected to the even-numbered signal lines. Moreover, pixel signal voltages of the negative polarity are applied to the odd rows of the pixel electrodes connected to the even-numbered signal lines, and the even rows of the pixel electrodes connected to the odd-numbered signal lines.

With this drive method, the polarity of the pixel signal voltage is reversed for each of the pixel electrodes arranged two-dimensionally on the liquid crystal display screen. As a result, the flickers can be prevented from being visually recognized easily.

However, a voltage of about ±5 V is normally needed to control the liquid crystal. Due to this, it is necessary for a signal line driver to have a driving ability which can obtain a sufficient voltage accuracy in a large output dynamic range of 10 V. This causes an increase in power consumed by the liquid crystal display.

BRIEF SUMMARY OF THE INVENTION

An object of the present invention is to provide a liquid crystal display capable of reducing power consumption while maintaining an excellent display quality.

According to the first aspect of the present invention, there is provided a liquid crystal display which comprises a matrix array of pixels to be selected for each row, a plurality of signal lines connected to the pixels of a selected row, a plurality of D/A converters, arranged to correspond to the signal lines, for converting digital pixel signals externally supplied for the pixels of the selected row into analog pixel signals, an amplifying section for amplifying the pixel signals obtained from the D/A converters, and a switch section for outputting the pixel signals obtained from the amplifying section to the signal lines.

The amplifying section has groups of first and second amplifying circuits each for amplifying the pixel signals obtained from adjacent two of the D/A converters in the opposite polarities. The first amplifying circuit is connected to a positive power source to amplify the pixel signal in the positive polarity, and the second amplifying circuit is connected to a negative power source to amplify the pixel signal in the negative polarity. The switch section has groups of switch circuits each for causing two of the signal lines to be exchanged and output the pixel signals obtained from the first and second amplifying circuits.

According to the display constituted as mentioned above, since each amplifying circuit is operated in a single polarity,

power consumption can be reduced. The D/A converters perform the digital-analog conversion without changing the polarity, accuracy of the conversion can be improved. Moreover, each set of the D/A converter and the amplifying circuit is used in common for adjacent two signal lines. Therefore, the circuitry size can be reduced.

According to the second aspect of the present invention, there is provided a liquid crystal display which comprises a matrix array of pixels to be selected for each row, a plurality of signal lines connected to the pixels of a selected row, a first video bus for transmitting an analog pixel signal of the positive polarity assigned to one of odd and even columns of the pixels present in the selected row, a second video bus for transmitting an analog pixel signal of the negative polarity assigned to the other one of the odd and even columns of the pixels present in the selected row, and groups of sample-hold circuits, arranged to correspond to the signal lines, for sequentially sample-holding the pixel signals transmitted by the first and second video buses. The sample-hold circuits of each group have a first switch circuit for causing the first and second video buses to be connected to one of adjacent two signal lines and the other of the adjacent two signal lines, and a second switch circuit for causing the first and second video buses to be connected to the other of the adjacent two signal lines and the one of the adjacent two signal lines. The first and second switch circuits are selectively turned on to simultaneously sample-hold the pixel signals transmitted by the first and second video buses and causing the two signal lines to be exchanged and output the pixel signals, respectively.

According to the display constituted as mentioned above, when the liquid crystal display is used to display a color image, the first and second video buses are used in common for color pixels (R-G, G-B, B-R) adjacent to each other in rows. Since each video bus transmits the pixel signal of a single polarity, power consumed due to the parasitic capacitance of the video bus can be reduced. Moreover, the adjacent signal lines can be driven by only these video buses. Such a decrease in the number of video buses enables to reduce the circuitry size.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

FIG. **1** is a circuit diagram of an active matrix liquid crystal display according to a first embodiment of the present invention;

FIG. **2** is a circuit diagram showing a main structure of a data line driver shown in FIG. **1**;

FIG. **3** is a circuit diagram for explaining a modification of the data line driver shown in FIG. **1**;

FIG. **4** is a circuit diagram of an active matrix liquid crystal display according to a second embodiment of the present invention;

FIG. **5** is a circuit diagram for explaining a first modification of the data line driver shown in FIG. **4**;

FIG. **6** is a circuit diagram for explaining a second modification of the data line driver shown in FIG. **1**;

FIG. **7** is a circuit diagram for explaining a third modification of the data line driver shown in FIG. **4**;

FIG. **8** is a circuit diagram showing D/A converters shown in FIG. **7** along with their peripheral circuits, in detail;

FIG. **9** is a circuit diagram for explaining a fourth modification in which the data line driver shown in FIG. **7** is applied to a color display; and

FIG. **10** is a view showing pixel data streams to be supplied to the data line driver shown in FIG. **9**.

DETAILED DESCRIPTION OF THE INVENTION

An active matrix liquid crystal display according to one embodiment of the present invention will now be described with reference to the accompanying drawings.

FIG. **1** is a circuit diagram of the liquid crystal display. The liquid crystal display comprises a gate line driver **1**, a data line driver **2**, and a liquid crystal panel **31**. The liquid crystal panel **31** has an array substrate and a counter substrate, each having a light transmitting property, and a liquid crystal layer which is held by the array and counter substrates and made of liquid crystal composition filled in the gap therebetween. The array substrate has a glass substrate, a matrix array of nxm pixel electrodes **11** formed on the glass substrate, n gate lines Y1 to Yn formed along rows of the pixel electrodes **11**, m data, lines X1 to Xm formed along columns of the pixel electrodes **11**, nxm thin film transistors (TFT) **12** formed near intersections of the gate lines Y1 to Yn and the data lines X1 to Xm as switching elements, and a first alignment film covering the entire matrix array of the pixel electrodes **20**. The counter substrate has a glass substrate, a light shielding film formed to mask an area surrounding each pixel electrode **11**, a color filter for filtering light to selectively transmit color components of red, green, and blue, a counter electrode **13** opposing to the matrix array of pixel electrodes **11**, and a second alignment film covering the entire counter electrode **22**. The first and second alignment films are provided for causing liquid crystal molecules to be set in a twisted nematic (TN) alignment when no potential difference exists between the pixel electrode **11** and the counter electrode **13**. Each TFT **12** has a gate connected to one of the gate lines Y1 to Yn, and a source-drain path connected between one of the data lines X1 to Xm and one of the pixel electrodes **11**. Each pixel electrode **11** is associated with the counter electrode **13** and the liquid crystal layer to constitute a liquid crystal capacitance CLC. Two polarizing plates are adhered onto the outer surfaces of the array and counter substrates to be right angles with each other. The gate line driver **1** and the data line driver **2** are located outside the matrix array of the pixel electrodes **11** in the glass surface of the array substrate.

The gate line driver **1** is controlled by control signals supplied from an external liquid crystal controller to perform an operation of sequentially driving the gate lines Y1 to Yn in each frame period. The control signals for the gate line driver **1** include a vertical start signal STV to be generated every one frame period and a vertical clock signal CPV to be generated every one horizontal scanning period. The operation of the gate line driver **1** is performed by use of a shift register circuit which shifts the vertical start signal STV in synchronism with the vertical clock signal CPV.

The data line driver **2** is controlled by control signals supplied from the external liquid crystal controller to perform an operation of sequentially driving the data lines X1 to Xn in each horizontal scanning period. The control signals for the data line driver **2** include a horizontal start signal STH to be generated every one horizontal scanning period, a digital video signal constituted by series items of pixel data DATA to be generated every one horizontal scanning period, a horizontal clock signal CPH to be generated for each pixel data DATA, and frame signals F1 and F2. The data line driver **2** comprises b shift register circuit **33**, m D/A converters **34**, m/2 first amplifying circuits **35**, m/2 second amplifying circuits **36**, and m/2 analog switches **37**.

The shift register circuit **33** performs a serial-parallel conversion of pixel data DATA by shifting the horizontal

start signal STH in synchronism with the horizontal clock signal CPH, latching pixel data DATA of a video signal at the time when the horizontal start signal STH is shifted, and outputting the pixel data DATA to the D/A converter **34** corresponding to the shift position of the horizontal start signal STH. The m D/A converters **34** are arranged to correspond to the data line X1 to Xm, and sample-hold pixel data DATA supplied from the shift register circuit **33** to convert each pixel data DATA to an analog pixel signal. The m/2 amplifying circuits **35** are connected commonly to a positive power line +V, and amplify the pixel signals from the odd-numbered D/A converters **34** in the positive polarity. The m/2 second amplifying circuits **36** are connected commonly to a negative power line −V, and amplify the pixel signals from the even-numbered D/A converters **34** in the negative polarity. In other words, the pixel signals from the adjacent two D/A converters **34** are amplified by the amplifying circuits **35** and **36** in the opposite polarities. The m/2 analog switches **37** are connected to the m/2 amplifying circuits **35** and **36**. Each analog switch **37** is controlled by frame signals F1 and F2 supplied from the external liquid crystal controller, and supplies the pixel signals of the opposite polarities obtained from the amplifying circuits **35** and **36** of the corresponding group, to the adjacent two data lines, alternatively.

More specifically, the frame signal F1 is set to be in a high level for a preceding frame period of two continuous frame periods, and to be in a low level for a following frame period of the two frame periods. The frame signal F2 is set to be in a low level for the preceding frame period of the two continuous frame periods, and to be in a high level for the following frame period of the two frame periods. Each analog switch **37** comprises first to fourth switching elements **37A** to **37D**. The first switching element **37A** is connected between one first amplifying circuit **35** and one odd-numbered data line. The second switching element **37B** is connected between one second amplifying circuit **36** and the odd-numbered data line. The third switching element **37C** is connected between the second amplifying circuit **36** and one even-numbered data line. The fourth switching element **37D** is connected between the first amplifying circuit **35** and the even-numbered data line. The switching elements **37A** and **37C** cause the amplifying circuits **35** and **36** to be electrically connected to the odd-numbered data line and the even-numbered data line when the frame signal F1 is in a high level, and to be electrically disconnected from the odd-numbered data line and the even-numbered data line when the frame signal F1 is in a low level. The switching elements **37B** and **37D** cause the amplifying circuits **36** and **35** to be electrically connected to the odd-number data line and the even-numbered data line when the frame signal F2 is in a high level, and to be electrically disconnected from the odd-numbered data line and the even-numbered data line when the frame signal F2 is in a low level. To correctly assign pixel signals to the pixels arranged in rows, the external liquid crystal controller has a memory for storing series items of pixel data to be supplied to the shift register circuit **33**, and reverses the order of every two adjacent pixel data items the preceding or following frame period.

In the preceding frame period, pixel signals of the positive polarity are output from the m/2 first amplifying circuits **35** to the data lines X1, X3, X5 . . . , and pixel signals of the negative polarity are output from the m/2 second amplifying circuits **36** to the data lines X2, X4, X6, X8 . . . . In the following frame period, pixel signals of the negative polarity are output from the second amplifying circuit **36** to the data lines X1, X3, X5, . . . , and pixel signals of the positive polarity are output from the first amplifying circuit **35** to the data lines X2, X4, X6, ... The destination of the pixel signals of the positive and negative polarities is changed between the pair of the data lines X1 and X2, the pair of the data lines X3 and X4, and the pair of the data lines X5 and X6 every one frame period. In other words, the pair of the data lines X1 and X2, the pair of the data lines X3 and X4, and the pair of the data lines X5 and X6 are driven in a V-line reverse manner by the pixel signals of the positive and negative polarities which are reversed every one frame period.

FIG. **2** shows the main structure of the data line driver **2** shown in FIG. **1**. Input terminals IN1 and IN2 are connected to receive the pixel signals supplied from the adjacent two D/A converters **34**. The first amplifying circuit **35** comprises a differential amplifier **38**, an N-channel transistor **39**, and a constant current source **40**. The drain of the transistor **39** is connected to a positive power line +V, and the source thereof is connected to a power line +V' through the constant current source **40**. The source output of the transistor **39** is fed back to the differential amplifier **38**. On the other hand, the second amplifying circuit **36** comprises a differential amplifier **41**, a P-channel transistor **42**, and a constant current source **43**. The drain of the transistor **42** is connected to a negative power line −V, and the source thereof is connected to a power line −V' through the constant current source **43**. The source output of the transistor **42** is fed back to the differential amplifier **41**. Regarding the labels such as "+V" and "−V", the potential polarities are not determined directly from the ground potential, and determined from a reference potential depending on the center level between the power line potentials. Actually, the power line potentials are set to +V=10 V, −V=5 V, +V'=5 V, and −V'=0 V. According to the above-mentioned structure, the first amplifying circuit **35** amplifies the pixel signal input from the input terminal IN1 and outputs the pixel signal whose polarity is positive with respect to the reference potential. The second amplifying circuit **36** amplifies the pixel signal input from the input terminal IN2 and outputs the pixel signal whose polarity is negative with respect to the reference potential.

The analog switch **37** comprises P-channel transistors **44**, **45** and N-channel transistors **46** and **47**, which are formed as switching elements **37A**, **37D**, **37B**, and **37C**, respectively. The gate of the transistor **44** is connected to a terminal SW1 which receives an inverted signal (or F2) of the frame signal F1. The gate of the transistor **45** is connected to a terminal SW2 which receives an inverted signal (or F1) of the frame signal F2. The gate of the transistor **46** is connected to a terminal SW3 which receives the frame signal F2. The gate of the transistor **47** is connected to a terminal SW4 which receives the frame signal F2. For the frame period in which the frame signal F1 is set to be in a high level and the frame signal F2 is set to be in a low level, the P-channel transistor **44** and the N-channel transistor **47** are turned on, and the P-channel transistor **45** and the N-channel transistor **46** are turned off. At this time, the pixel signal from the first amplifying circuit **35** is output to the odd-numbered data line through the output terminal S1. The output signal of the second amplifying circuit **36** is output to the even-numbered data line through the output terminal S2.

On the other hand, for the frame period in which the frame signal F1 is set to be in a low level and the frame signal F2 is set to be a high level, the P-channel transistor **45** and the N-channel transistor **46** are turned on, and the P-channel transistor **44** and the N-channel transistor **47** are turned off. At this time, the pixel signal from the first amplifying circuit **35** is output to the even-numbered data line through the

output terminal S2. The output signal of the second amplifying circuit 36 is output to the odd-numbered data line through the output terminal S1.

According to the above-explained embodiment, the pixel signals output from the first amplifying circuits 35 are always set to have the positive polarity. The pixel signals output from the first amplifying circuits 36 are always set to have the negative polarity. Due to this, the dynamic ranges of the amplifying circuits 35 and 36 can be determined based on the necessary liquid crystal drive voltage without considering the reversion of the voltage polarity. As a result, electrical power can be prevented from be wastefully consumed by the amplifying circuits. Moreover, each D/A converter 34 may generate a voltage in that one of the positive and negative polarities which conform to the voltage polarity of the pixel signal output from the corresponding amplifying circuit 35 or 36. As a result, the accuracy of the D/A conversion can be improved as reducing the power consumption.

The liquid crystal display of this embodiment may be constituted to perform an HV reverse drive in which the voltage polarities of the pixel signals to be applied to the data lines are additionally reversed every row. In this case, the analog switches 37 may be controlled by signals which are reversed every one horizontal scanning period, in place of the frame signals F1 and F2. In this driving form, the voltages applied to the liquid crystal pixels in adjacent rows and adjacent columns differ from each other. This increases a spatial frequency, thereby further suppressing the image deterioration such as flickers and a line scroll.

Moreover, the transistors 44 to 47 shown in FIG. 2 may be formed of CMOS transistors. The transistors included in the analog switch 37 and the amplifying circuits 35 and 36 may be formed of thin film transistors (TFT), which are formed on the array substrate together with the thin film transistors allocated to the respective pixel electrodes 11. These thin film transistor may be formed of well-known staggered type TFTs. In this case, each thin film transistor is obtained by forming a polycrystalline silicon layer of a predetermined shape on the glass substrate, forming a silicon oxide film covering the entire surface of the polycrystalline silicon layer and serving as a gate insulating film, forming a gate electrode united with the gate line Y1, Y2, . . . , or Yn on the gate insulating film, and forming a source electrode united with data line X1, X2, . . . , or Xm and a drain electrode of the same layer as the source electrode, on the gate electrode via an interlayer insulating film. Moreover, the shift register circuit 33 may be obtained by combining well-known flip-flop circuits having TFT elements formed on the array substrate together with the thin film transistors 12 allocated to the pixel electrodes 11.

In the case where the transistors have a common structure in the liquid crystal display, the required number of manufacturing steps is reduced. Therefore, it is possible to manufacture the liquid crystal display with low cost.

A modification of the data line driver shown in FIG. 1 will be described with reference to FIG. 3:

In the first embodiment, the order of every adjacent two pixel data items was reversed in the memory of the external liquid crystal controller to allocate the pixel signals to the pixels arranged in rows within the successive two frame periods. Regarding the modification shown in FIG. 3, the shift register circuit 33 is structured such that the order of the pixel data items to be supplied to every adjacent two D/A converters 34 is reversed every one frame period.

FIG. 3 specifically shows that part of the data line driver 2 which drives the first and second data lines. The horizontal start signal STH is supplied to registers 48 and 49 in a forward or opposite order through logic gates 50 to 55 controlled by the frame signals F1 and F2.

For the preceding period in which the frame signal F1 is set to be in a high level and the frame signal F2 is set to be in a low level, the AND gates 50, 53, and 56 are opened, and the AND gates 51, 54, and 57 are closed. As a result, the horizontal start signal STH is supplied to the register 48 through the AND gate 50 and the OR gate 52. The output of the register 48 is directly supplied to a latch 59 on one hand, and to the register 49 through the AND gate 53 and the OR gate 55 on the other hand. Thereby, the horizontal start signal STH is transferred to the registers 48, 49, . . . in this order, in synchronism with the horizontal clock signal CPH. Latches 59, 60, . . . latch pixel data DATA on data buses D1 . . . Dn at timing when the horizontal start signal STH is held and output by the respective registers 48, 49, ... Then, the latched pixel data DATA are supplied to the corresponding D/A converters 34.

For the following period in which the frame signal F1 is set to be in a low level and the frame signal F2 is set to be in a high level, the AND gates 51, 54, and 57 are opened, and the AND gates 50, 53, and 56 are closed. As a result, the horizontal start signal STH is supplied to the register 49 through the AND gate 54 and the OR gate 55. The output of the register 49 is directly supplied to the latch 60 on one hand, and to the register 48 through the AND gate 51 and the OR gate 52 on the other hand. Thereby, the horizontal start signal STH is transferred to the registers 49, 48, . . . in this order. In other words, as compared with the preceding frame period, the output order of the odd- and even-numbered registers is reversed.

The operations of the D/A converters 34, the amplifying circuits 35 and 36, and the switches 37 are the same as the case of the first embodiment.

According to the above-mentioned modification, the pixel signals of the positive and negative polarities are correctly allocated to the pixels arranged in rows without reversing the order of pixel data items outside the display to perform the polarity reverse drive. Therefore, the circuit required for reversing the order of the pixel data items outside the display can be eliminated.

An active matrix liquid crystal display according to the second embodiment of the present invention will be described with reference to FIG. 4. The liquid crystal display has substantially the same structure as that of the display shown in FIG. 1 except for the data line driver 2. In FIG. 4, the portions common to the first embodiment are shown by the same reference numerals, and the explanation is omitted.

The data line driver 2 shown in FIG. 4 performs a serial-parallel conversion on analog pixel signals supplied from the external liquid crystal controller by use of sample-hold circuits. In the data line driver 2, a shift register circuit 63 has m registers connected in series such that the horizontal start signal STH is shifted in synchronism with the horizontal clock signal CPH. Register outputs Q1, Q2, Q3, . . . Qm are connected to m sample-hold circuits 61 and 62 arranged to correspond to the data lines X1, X2, X3, . . . Xm. These registers are connected to each other as shown in FIG. 3 such that the output order of the odd and even-numbered registers is reversed.

In FIG. 4, 61 denotes m/2 odd-numbered sample-hold circuits, and 62 denotes m/2 even-numbered sample-hold circuits. The sample-hold circuits 61 are connected to a video bus Vin+ which transmits an RGB analog video signal of the positive polarity, so as to sample-hold the analog

video signal in response to each horizontal start signal from the register output terminals Q1, Q3, Q5, . . . , Qm−1 and supply them to the odd-numbered amplifying circuits 35 as pixel signals. The sample-hold circuits 62 are connected to a video bus Vin− which transmits an RGB analog video signal of the positive polarity, so as to sample-hold the analog video signal in response to each horizontal start signal from the register output terminals Q2, Q4, Q6, . . . , Qm and supply them to the even-numbered amplifying circuits 36 as pixel signals. The amplifying circuits 35 are connected commonly to the positive power line +V to amplify the pixel signals from the odd-numbered sample-hold circuits 61 in the positive polarity. The second amplifying circuits 36 are connected commonly to the negative power line −V to amplify the pixel signals from the even-numbered sample-hold circuits 62 in the negative polarity. In other words, the pixel signals from the adjacent two sample-hold circuits 61 and 62 are amplified by the amplifying circuits 35 and 36 in the opposite polarities. The m/2 analog switches 37 are, connected to m/2 groups of amplifying circuits 35 and 36. Each analog switches 37 are controlled by the external liquid crystal controller in the same manner as that of the first embodiment, so as to supply the pixel signals of the opposite polarities obtained from the amplifying circuits 35 and 36 of the corresponding group to the adjacent two data lines, alternatively.

According to the above-mentioned structure, for the frame period in which the frame signal F1 is set to be in a high level and the frame F2 is set to be in a low level, the horizontal start signal STH is output from the shift register circuit 63 in the order of Q1, Q2, Q3, . . . , Qm, so as to enable the sample-hold operation. As a result, the sample-hold circuits 61 and 62 sample-hold the video signals on the video buses Vin+ and Vin− in their order. Since the operations of the analog switches 37 are the same as those in the first embodiment, the pixel signals of the positive polarity are supplied to the odd-numbered data lines X1, X3, X5, . . . through the amplifying circuits 35, and the voltages of the negative polarity are supplied to the even-numbered data lines X2, X4, X6, . . . through the amplifying circuits 36.

For the frame period in which the frame signal F1 is set to be in a low level and the frame F2 is set to be in a high level, the horizontal start signal STH is output from the shift register circuit in the order of Q2, Q1, Q4, Q3, . . . , so as to enable the sample-hold operation. As a result, the operation order of the sample-hold circuits 61 and 62 corresponding to the adjacent two data lines in this frame period is opposite to the preceding frame period. Since the operations of the analog switches 37 are the same as those in the first embodiment, the voltages of the negative polarity are supplied to the odd-numbered data lines X1, X3, X5, . . . through the amplifying circuits 35, and the voltages of the positive polarity are supplied to the even-numbered data lines X2, X4, X6, . . . through the amplifying circuits 36.

According to the above-mentioned embodiment, the pixel signals output from the first amplifying circuits 35 are always set to have the positive polarity, and the pixel signals output from the second amplifying circuits 36 are always set to have the negative polarity. Due to this, the dynamic ranges of the amplifying circuits 35 and 36 can be determined based on the necessary liquid crystal drive voltage without considering the reversion of the voltage polarity. As a result, electrical power can be prevented from be wastefully consumed by the amplifying circuits.

The first modification of the data line driver 2 shown in FIG. 4 will be explained with reference to FIG. 5.

In this modification, each analog switch 37 is structured to further comprise a switching element 64 connected between the output terminal S1 and a reference power line Vref, and a switching element 65 connected between the output terminal S2 and the reference power line Vref. The reference power line Vref is set to be a reference potential equal to an intermediate level between the potential of the positive power line +V and the potential of the negative power line −V. In operation, all switching elements 37A to 37D are opened immediately before the pixel signals of the positive and negative polarities are output to the adjacent two data lines through the output terminals S1 and S2. During this time, the switching elements 64 and 65 are closed. The switching elements 64 and 65 discharge electric charges stored in the parasitic capacitances of the two data lines, and set the data lines to be potentials equal to the reference voltage. Thereafter, when the pixel signals of the positive and negative polarities are output from the first and second amplifying circuits 35 and 36, these data lines are charged from the reference potential to potentials corresponding to the pixel signals.

According to the above-mentioned structure, the amplifying circuits 35 and 36 can perform charging of each data line with a reduced driving ability. That is, an excellent operation reliability can be obtained without making the structure of amplifying circuits 35 and 36 complicated in consideration of the withstanding voltage. Regarding the circuit other than the analog switches 37, it can be formed in the same structure as the first embodiment or the third embodiment.

The second modification of the data line driver 2 shown in FIG. 4 will be explained with reference to FIG. 6.

In this modification, each analog switch 37 is structured to further comprise a switching element 70 connected between the output terminals S1 and S2. Similar to the first embodiment, the data line driver 2 performs the polarity reversion of the liquid crystal signal voltage by causing the outputs of the first and second amplifying circuits 35 and 36 to be exchanged. More specifically, all the switching elements 37A to 37D are opened immediately before the pixel signals of the positive and negative polarities are output to the adjacent two data lines through the output terminals S1 and S2. During this time, the switching element 70 is closed. The switching element 70 discharges electric charges stored in the parasitic capacitances of the two data lines, and set the data lines to be the same, potentials, which are substantially equal to the reference voltage Vref. Thereafter, when the pixel signals of the positive and negative polarities are output from the first and second amplifying circuits 35 and 36, these data lines are charged from the reference potential to potentials corresponding to the pixel signals.

According to the above-mentioned structure, the amplifying circuits 35 and 36 can perform charging of each data line with a reduced driving ability. That is, an excellent operation reliability can be obtained without making the structure of amplifying circuits 35 and 36 complicated in consideration of the withstanding voltage. Moreover, since a potential difference can be canceled by the charges moving from one of the adjacent data lines to the other, power consumption can be reduced.

The third modification of the data line driver 2 shown in FIG. 4 will be explained with reference to FIG. 7.

In this modification, the switches 35 shown in FIG. 4 are eliminated. Instead, each of m sample-hold circuits 61 and 62 is connected to both video buses Vin+ and Vin−. The sample-hold circuit 61 has a P-channel transistor 77 connected between the video bus Vin+ and the output terminal S1, and an N-channel transistor 78 connected between the

video bus Vin− and the output terminal S1. The sample-hold circuit 62 has a P-channel transistor 79 connected between the video bus Vin− and the output terminal S2, and an N-channel transistor 80 connected between the video bus Vin− and the output terminal S2. In FIG. 7, 81 and 82 denote parasitic capacitances of the data lines which are respectively connected to the output terminals S1 and S2 and serve to hold the voltages of the pixel signals output from the output terminals S1 and S2.

The video line Vin+ is driven by a D/A converter 101, and the video line Vin− is driven by a D/A converter 102. These D/A converters 101 and 102 are provided outside the array substrate and formed to have the same structure.

The gate of the P-channel transistor 77 is connected to the output terminal of an OR gate 73, and the gate of the N-channel transistor 78 is connected to the output terminal of an AND gate 74. The gate of the P-channel transistor 79 is connected to the output terminal of a NAND gate 75, and the gate of the N-channel transistor 80 is connected to the output terminal of a NOR gate 76.

The OR gate 73, AND gate 74, NAND gate 75, and NOR gate 76 are connected to receive a switching signal SW. The AND gate 74 is connected to the output terminal of a register 71, and the NAND gate 75 is connected to the output terminal of a register 72. The OR gate 73 is connected to the output terminal of the register 72 through an inverter 83, the NOR gate 76 is connected to the output terminal of the register 72 through an inverter 84. The registers 71 and 72 are connected in series with each other so as to constitute the shift register circuit for sequentially shifting the horizontal start signal STH in synchronism with the horizontal clock CPH.

The above-structured data line driver 2 operates as follows:

If the switching signal SW is in a low level, the OR gate 73 is set to a state that the signal is passed therethrough, the output of the AND gate 74 is in a low level, the output of the NAND gate 75 is in a high level, and the NOR gate 76 is set to a state that the signal is reversed and passed therethrough. Therefore, the P-channel transistor 77 is set to be in a conductive state by the output of the register 71, and the N-channel transistor 78 and the P-channel transistor 79 are turned off. The N-channel transistor 80 is set to be in a conductive state by the output of the register 71. As a result, the video signal Vin+ of the positive polarity is output to the output terminal S1 based on the output of the register 71. The video signal Vin− of the negative polarity is output to the output terminal S2 based on the output of the register 72.

If the switching signal SW is in a high level, the OR gate 73 is in a high level, the AND gate 74 is set to a state that the signal is passed therethrough, the output of the NAND gate 75 is set to a state that the signal is reversed and passed therethrough, and the output of the NOR gate 76 is in a low level. Therefore, the P-channel transistor 77 is turned off, and the N-channel transistor 78 is set to be in a conductive state by the output of the register 71. The P-channel transistor 79 is set to be in a conductive state by the output of the register 72, and the N-channel transistor 80 is turned off. As a result, the video signal Vin− of the negative polarity is output to the output terminal S1 based on the output of the register 71. The video signal Vin+ of the positive polarity is output to the output terminal S2 based on the output of the register 72.

Accordingly, the video signal Vin+ of the positive polarity and the video signal Vin− of the negative polarity are alternatively output to the output terminals S1 and S2 in accordance with the change of the switching signal SW. Thereby, the liquid crystal pixels are driven by the voltages whose polarity is periodically reversed.

In this case, the respective logic gates 73 to 76, 83, 84, and the respective switching elements 77 to 78 may be formed of the well-known TFT structure. Moreover, the registers 71 and 72 may be formed of TFT elements combined to serve as a well-known flip-flop circuit. In this case, similar to the first embodiment, the manufacturing cost of the liquid crystal display can be reduced by commonly forming these transistor elements together with the thin film transistors for the pixel electrodes, in the same step.

FIG. 8 shows the D/A converters 101 and 102 along with their peripheral circuits, in detail. The D/A converters 101 and 102 are of a voltage selection type. Specifically, each of the D/A converters 101 and 102 are connected to commonly receive pixel data DATA output from an external liquid crystal controller 104, and has a set of analog switches SW1 to SWn to be switched on the basis of the pixel data. The analog switches SW1 to SWn combines voltages generated from γ correction circuit 103 and supplied through analog signal lines 110 to output an analog pixel signal of a voltage level corresponding to pixel data DATA to the video bus Vin+ or Vin−.

As shown in FIG. 8, the D/A converter 101 is formed to operate under a voltage between the power lines which are respectively set to 3 V and 4 V. The D/A converter 102 is formed to operate under a voltage between the power lines which are respectively set to 1 V and 2 V. In this case, the threshold voltage of the analog switches SW1 to SWn of the D/A converter 101 differs from those of the D/A converter 102. Therefore, capacitors Cq are inserted between the liquid crystal controller 104 and the D/A converter 101 to attain capacitive couplings therebetween. Then, a bias voltage is applied to one end of each of capacitors Cq. The bias voltage is regulated such that the voltage level of input pixel data matches the threshold level of the analog switches SW1 to SWn. Therefore, the D/A converters 101 and 102 of the same structure can operate under different operation voltages. In this modification, the bias voltage is applied to the capacitors Cq. However, dummy data for charging the capacitors Cq may be input toward the capacitors Cq before inputting pixel data. Thereby, the voltage level of data can be adjusted without applying a special bias voltage.

Moreover, the γ correction circuit 103 comprises resisters R1+ to Rn+ and R1− to Rn− connected in series. Since an optical response of the liquid crystal material slightly differs depending on the positive and negative voltages, γ correction must be made in each of the drive voltage of the positive polarity and the drive voltage of the negative polarity. Due to this, a potential terminal VM which is connected to a central point between the series circuit of resistors R1+ to Rn for the γ correction to the voltage of the positive polarity and the series circuit of resistors R1− to Rn− for the γ correction to the voltage of the negative polarity, and the potential of the potential terminal is controlled, so as to determine the voltages across the circuit of the resistors R1+ to Rn+ and the circuit of the resistors R1− to Rn−.

The fourth modification of the data line driver 2 shown in FIG. 7 and serving as a color display will be explained with reference to FIG. 9.

In this modification, analog pixel signals of R1 (Red), G1 (Green), B1 (Blue), R2 (Red), G2 (Green), B2 (Blue), . . . are sequentially output to data lines X1, X2, X3, X4, X5, X6, . . . P-channel TFTs 77 and 79 for driving the data lines X1, X2, X5, X6 are connected commonly to an output video line V1+

of the D/A converter **101**. N-channel TFTs **78** and **80** for driving the data lines X1, X2, X5, X6 are connected commonly to an output video line V1− of the D/A converter **102**. P-channel TFTs **77** and **79** for driving the data lines X3, X4 are connected commonly to an output video line V2+ of the D/A converter **101**. N-channel TFTs **78** and **80** for driving the data lines X3, X4 are connected commonly to an output video line V2− of the D/A converter **102**. The gates of the P-channels **77** and **79** and N-channel TFTs for driving the data lines X1 to X4 are connected to the common register **71** through logic circuits **73** to **76**. Regarding the data line **7** and the following data lines, they are arranged such that the above-mentioned structure is periodically repeated, and each group of TFTs for driving four data lines commonly receives an output signal from the corresponding register.

The operation of the data line driver **2** will be explained. For example, in the case of data lines X1, X2, similar to the modification shown in FIG. 6, an enable signal is input to the P-channel TFT **77** for driving the data line X1 and the N-channel TFT **80** for driving the data line X2 at common timing by the logic gates **73** and **76**. Therefore, the signal voltage on the video line V1+ is supplied to the data line X1 through the P-channel TFT **77**. At the same time, the signal voltage on the video line V1− is supplied to the data line X2 through the P-channel TFT **80**. Moreover, an enable signal is input to the P-channel TFT **77** for driving the data line X3 and the N-channel TFT **80** for driving the data line X2 at common timing. Therefore, the signal voltage on the video line V2+ is supplied to the data line X3 through the P-channel TFT **77**. At the same time, the signal voltage on the video line V2− is supplied to the data line X4 through the P-channel TFT **80**.

FIG. **10** shows pixel data streams to be supplied to the two D/A converters **101** and **102** from the liquid crystal controller shown in FIG. **9**.

For an i-th frame period, the data stream of pixel data R1 for data line X1, pixel data G2 for data line; X5, . . . is input to the D/A converter **101** to drive the video line V1+. The data stream of pixel data G1, B2, . . . is input to the D/A converter **102** to drive the video line V1−. The data stream of pixel data B1, R3, . . . is input to the D/A converter **101** to drive the video line V2+. Moreover, the data stream of pixel data R2, G3, . . . is input to the D/A converter **102** to drive the video line V2−. The D/A converter **101** converts each of pixel data R1, G2, . . . to an analog pixel signal of the positive polarity to be supplied to the video line V1+, and also converts each of pixel data B1, R3, . . . to an analog pixel signal of the positive polarity to be supplied to the video line V2+. On the other hand, the D/A converter **102** converts each of pixel data G1, B2, . . . to an analog pixel signal of the negative polarity to be supplied to they video line V1−, and also converts each of pixel data R2, G3, . . . to an analog pixel signal of the negative polarity to be supplied to the video line V2−.

For a next (i+1)-th frame period, the data stream of pixel data G1 for data line X2, pixel data B2 for data line X6, . . . is input to the D/A converter **101** to drive the video line V1+. The data stream of pixel data R1, G2, . . . is input to the D/A converter **102** to drive the video line V1−. The data stream of pixel data R2, G3, . . . is input to the D/A converter **101** to drive the video line V2+. Moreover, the data stream of pixel data B1, R3, . . . is input to the D/A converter **102** to drive the video line V2−. The D/A converter **101** converts each of pixel data G1, B2, . . . to an analog pixel signal of the positive polarity to be supplied to the video line V1+, and also converts each of pixel data R2, G3 . . . to an analog pixel signal of the positive polarity to be supplied to the video line V2+. On the other hand, the D/A converter **102** converts each of pixel data R1, G2, . . . to an analog pixel signal of the negative polarity to be supplied to the video line V1−, and also converts each of pixel data B1, R3 . . . to an analog pixel signal of the negative polarity to be supplied to the video line V2−.

According to the above modification, the video line Vin+ for transmitting the voltage of the analog pixel signal of the positive polarity and the video line Vin− for transmitting the voltage of the analog pixel signal of the negative polarity is separated from each other. As a result, electrical power consumed by the parasitic capacitances of the video lines Vin+ and Vin− can be reduced. Also, the video signal band width can be expanded. Moreover, the pixel signals of different colors such as R (Red), G (Green) can be transmitted through a common video line. Therefore, the number of the video lines can be decreased to reduce the circuitry size.

I claim:

1. A liquid crystal display comprising:

a matrix array of liquid crystal pixels;

a plurality of signal lines formed along columns of the liquid crystal pixels;

a plurality of driving transistors assigned to said liquid crystal pixels, for causing said signal lines to be electrically connected to the liquid crystal pixels of a selected row; and

a signal line driver for driving said signal lines, wherein said signal line driver includes:

a signal distribution controller for causing digital pixel signals serially supplied for the liquid crystal pixels of the selected row to be output in parallel,

a plurality of D/A converters arranged to correspond to said signal lines, for converting digital pixel signals output in parallel from said signal distribution controller into analog pixel signals,

an amplifying section for amplifying the pixel signals obtained from the D/A converters, and

a switch section for outputting the pixel signals obtained from the amplifying section to the signal lines;

said amplifying section includes groups of first and second amplifying circuits for amplifying the pixel signals obtained from adjacent two of said D/A converters in different polarities;

said first amplifying circuit is connected to a first power source to amplify the pixel signal in a positive polarity;

said second amplifying circuit is connected to a second power source to amplify the pixel signal in a negative polarity;

said switch section includes a plurality of switch circuits each for periodically exchanging adjacent two of said signal lines which receive the pixel signals obtained from said first and second amplifying circuits of a corresponding group;

each switch circuit includes a first switching element connected between said first amplifying circuit and one of said adjacent two signal lines, a second switching element connected between said first amplifying circuit and the other one of said adjacent two signal lines, a third switching element connected between said second amplifying circuit and the one of said adjacent two signal lines, and a fourth switching element connected between said second amplifying circuit and the other one of said adjacent two signal lines;

a pair of first and fourth switching elements and a pair of said second and third switching elements are controlled to alternately turn on in predetermined cycles by a control signal supplied externally;

said first and second switching elements are constituted by transistors of a first conductivity type; and

said third and fourth switching elements are constituted by transistors of a second conductivity type.

2. A liquid crystal display according to claim **1**, wherein said signal distribution controller includes signal order reversing means for reversing the order of every two serially-supplied digital pixel signals to cope with the exchange operations of said switch circuits.

3. A liquid crystal display according to claim **1**, wherein components of said signal line driver are formed together with said driving transistors on an array substrate.

4. A liquid crystal display comprising:

a matrix array of liquid crystal pixels;

a plurality of signal lines formed along columns of the liquid crystal pixels;

a plurality of driving transistors assigned to said liquid crystal pixels, for causing said signal lines to be electrically connected to the liquid crystal pixels of a selected row; and

a signal line driver for driving said signal lines, wherein said signal line driver includes:

a signal distribution controller for causing digital pixel signals serially supplied for the liquid crystal pixels of the selected row to be output in parallel,

a plurality of D/A converters arranged to correspond to said signal lines, for converting digital pixel signals output in parallel from said signal distribution controller, into analog pixel signals,

an amplifying section for amplifying the pixel signals obtained from the D/A converter; and

a switch section for outputting the pixel signals obtained from the amplifying section to the signal lines;

said amplifying section includes groups of first and second amplifying circuits for amplifying the pixel signals obtained from adjacent two of said D/A converters in different polarities;

said first amplifying circuit is connected to a first power source to amplify the pixel signal in a positive polarity;

said second amplifying circuit is connected to a second power source to amplify the pixel signal in a negative polarity;

said switch section includes a plurality of switch circuits each for periodically exchanging adjacent two of said signal lines which receive the pixel signals obtained from said first and second amplifying circuits of a corresponding group; and

said signal distribution controller includes a plurality of latch circuits arranged to correspond to said D/A converters, each for latching a corresponding one of the serially-supplied digital pixel signals, and a shift register circuit for sequentially enabling said latch circuits; and

said shift register circuit includes latch order reversing means for reversing the latch order of every two latch circuits to cope with the operations of said switch circuits.

5. A liquid crystal display comprising:

a matrix array of liquid crystal pixels;

a plurality of signal lines formed along columns of the liquid crystal pixels;

a plurality of driving transistors assigned to said liquid crystal pixels, for causing said signal lines to be electrically connected to the liquid crystal pixel of a selected row; and

a signal line driver for driving said signal lines, wherein said signal line driver includes:

a signal distribution controller for causing digital pixel signals serially supplied for the liquid crystal pixels of the selected row to be output in parallel,

a plurality of D/A converters arranged to correspond to said signal lines, for converting digital pixel signals output in parallel from said signal distribution controller, into analog pixel signals,

an amplifying section for amplifying the pixel signals obtained from the D/A converters, and

a switch section for outputting the pixel signals obtained from the amplifying section to the signal lines;

said amplifying section includes groups of first and second amplifying circuits for amplifying the pixel signals obtained from adjacent two of said D/A converters in different polarities;

said first amplifying circuit is connected to a first power sources to amplify the pixel signal in a positive polarity;

said second amplifying circuit is connected to a second power source to amplify the pixel signal in a negative polarity;

said switch section includes a plurality of switch circuits each for periodically exchanging adjacent two of said signal lines which receive the pixel signals obtained from said first and second amplifying circuits of a corresponding group; and

each switch circuit includes a canceling section for canceling a difference between the potentials of said adjacent two signal lines prior to outputting the pixel signals from said first and second amplifying circuits.

6. A liquid crystal display according to claim **5**, wherein said canceling section includes a pair of switching elements each connected between a corresponding one of the adjacent two signal lines and a reference potential terminal set to an intermediate level for potential reversion.

7. A liquid crystal display according to claim **5**, wherein said canceling section includes a switching element connected between said adjacent two signal lines.

8. A liquid crystal display comprising:

a matrix array of liquid crystal pixels;

a plurality of signal lines formed along columns of the liquid crystal pixels;

a plurality of driving transistors assigned to said liquid crystal pixels, for causing said signal lines to be electrically connected to the liquid crystal pixels of a selected row; and

a signal line driver for driving said signal lines, wherein said signal line driver includes:

a first video bus for transmitting analog pixel signals of a positive polarity for the liquid crystal pixels of one of odd and even columns in a selected row,

a second video bus for transmitting analog pixel signal of a negative polarity for the liquid crystal pixels of the other one of the odd and even columns in the selected row,

a plurality of sample-hold units each assigned to corresponding adjacent two of said signal lines to simultaneously sample-hold the pixel signals transmitted through said first and second video buses, and

a timing control circuit for sequentially enabling the operations of said sample-hold unit;

each sample-hold unit includes a first switch circuit for causing the first and second video buses to be respectively connected to one of the adjacent two signal lines and the other one of the adjacent two signal lines, and a second switch circuit for causing the first and second video buses to be respectively connected to the other one of the adjacent two signal lines and the one of the adjacent two signal lines;

said timing control circuit includes changing means for periodically switching between the first and second switch circuits of each sample-hold unit;

each sample-hold unit includes first and second switching elements serving as said first switch circuit, and third and fourth switching elements serving as said second switch circuit, said first switching element being connected between said first video bus and one of said adjacent two signal lines, said second switching element being connected between said second video bus and the other one of said adjacent two signal lines, said third switching element being connected between said first video bus and one of said adjacent two signal lines, and said fourth switching element being connected between said second video bus and the other one of said adjacent two signal lines;

said first and third switching elements are constituted by transistors of a first conductivity type, and said second and fourth switching elements are constituted by transistors of a second conductivity type.

9. A liquid crystal display according to claim **8**, wherein said liquid crystal pixels are arranged in a predetermined color order, said first and second video buses transmit color pixel signals set to have an order corresponding to the color order of the liquid crystal pixels in a selected row as the analog pixel signals of a positive polarity and the analog pixel signals of a negative polarity.

10. A liquid crystal display according to claim **8**, wherein said signal line driver further includes a first D/A converter for converting digital pixel signal into the analog pixel signals of a positive polarity to drive said first video bus, and a second D/A converter for converting the digital pixel signals into the analog pixel signals of a negative polarity to drive said second video bus.

11. A liquid crystal display according to claim **10**, wherein said first and second D/A converters have the same structure except that the first and second D/A converters are connected to different power sources to obtain the analog pixel signals of the positive and negative polarities.

12. A liquid crystal display comprising:

a matrix array of liquid crystal pixels;

a plurality of signal lines formed along columns of the liquid crystal pixels;

a plurality of driving transistors assigned to said liquid crystal pixels, for causing said signal lines to be connected electrically to the liquid crystal pixels of a selected row; and

a signal line driver for driving said signal lines, wherein said signal line driver includes:

a first video bus for transmitting analog pixel signals of a positive polarity for the liquid crystal pixels of one of odd and even columns in a selected row,

a second video bus for transmitting analog pixel signals of a negative polarity for the liquid crystal pixels of the other one of the odd and even columns in the selected row,

a plurality of sample-hold units each assigned to corresponding adjacent two of said signal lines to simultaneously sample-hold the pixel signal transmitted through said first and second video buses, and

a timing control circuit for sequentially enabling the operations of said sample-hold units;

each sample-hold unit includes a first switch circuit for causing the first and second video buses to be respectively connected to one of the adjacent two signal lines and the other one of the adjacent two signal lines, and a second switch circuit for causing the first and second video buses to be respectively connected to the other one of the adjacent two signal lines and the one of the adjacent two signal lines;

said timing control circuit includes changing means for periodically switching between the first and second switch circuits of each sample-hold unit;

said signal line driver further include a first D/A converter for converting digital pixel signals into the analog pixel signals of a positive polarity to drive said first video bus, and a second D/A converter for converting the digital pixel signals into the analog pixel signals of a negative polarity to drive said second video bus;

said first and second D/A converters have the same structure except that the first and second D/A converters are connected to different power sources to obtain the analog pixel signals of the positive and negative polarities; and

one of said first and second D/A converters is formed to receive the digital pixel signals through capacitive means.

13. A liquid crystal display comprising:

a matrix array of liquid crystal pixels;

a plurality of signal lines formed along columns of the liquid crystal pixels;

a plurality of driving transistors assigned to said liquid crystal pixels for causing said signal lines to be electrically connected to the liquid crystal pixels of a selected row; and

a signal line driver for driving said signal lines, wherein said signal line driver includes:

a first video bus for transmitting analog pixel signals of a positive polarity for the liquid crystal pixels of one of odd and even columns in a selected row,

a second video bus for transmitting analog pixel signals of a negative polarity for the liquid crystal pixels of the other one of the odd and even columns in the selected row,

a plurality of sample-hold units each assigned to corresponding adjacent two of said signal lines to simultaneously sample-hold the pixel signals transmitted through said first and second video buses, and

a timing control circuit for sequentially enabling the operations of said sample-hold units;

each sample-hold unit includes a first switch circuit for causing the first and second video buses to be respectively connected to one of the adjacent two signal lines and the other one of the adjacent two signal lines and a second switch circuit for causing the first and second video buses to be respectively connected to the other one of the adjacent two signal lines and the one of the adjacent two signal lines;

said timing control circuit includes changing means for periodically switching between the first and second switch circuits of each sample-hold unit;

said signal line driver further includes a first D/A converter for converting digital pixel signals into the analog pixel signals of a positive polarity to drive said first video bus, and a second D/A converter for converting the digital pixel signals into the analog pixel signals of a negative polarity to drive said second video bus; and

said signal line driver includes first γ correcting means for correcting a γ characteristic of said first D/A converter and second γ correcting means for correcting a γ characteristic of said second D/A converter.

14. A liquid crystal display comprising:

a matrix array of liquid crystal pixels,

a plurality of signal lines formed along columns of the liquid crystal pixels;

a plurality of driving transistors assigned to said liquid crystal pixels for causing said signal lines to electrically connected to the liquid crystal pixels of a selected row; and

a signal line driver for driving said signal lines, wherein said signal line driver includes:

a first video bus for transmitting analog pixel signals of a positive polarity for the liquid crystal pixels of one of odd and even columns in a selected row,

a second video bus for transmitting analog pixel signals of a negative polarity for the liquid crystal pixels of the other one of the odd and even columns in the selected row,

a plurality of sample-hold units each assigned to corresponding adjacent two of said signal lines to simultaneously sample-hold the pixel signals transmitted through said first and second video buses, and

a timing control circuit for sequentially enabling the operations of said sample-hold units;

each sample-hold unit includes a first switch circuit for causing the first and second video buses to be respectively connected to one of the adjacent two signal lines and the other one of the adjacent two signal lines, and a second switch circuit for causing the first and second video buses to be respectively connected to the other one of the adjacent two signal lines and the one of the adjacent two signal lines;

said timing control circuit includes changing means for periodically switching between the first and second switch circuits of each sample-hold unit; and

said sample-hold unit includes a canceling section for canceling a difference between the potentials of said adjacent two signal lines prior to outputting of the pixel signals.

15. A liquid crystal display according to claim **14**, wherein said canceling section includes a pair of switching elements each connected between a corresponding one of the adjacent two signal lines and a reference potential terminal set to an intermediate level for potential reversion.

16. A liquid crystal display according to claim **14**, wherein said canceling section includes a switching element connected between said adjacent two signal lines.

17. A liquid crystal display comprising:

a matrix array of liquid crystal pixels;

a plurality of signal lines formed along columns of the liquid crystal pixels;

a plurality of driving transistors assigned to said liquid crystal pixels for causing said signal lines to be electrically connected to the liquid crystal pixels of a selected row; and

a signal line driver for driving said signal lines, wherein said signal line driver includes:

a first video bus for transmitting analog pixel signals of a positive polarity for the liquid crystal pixels of one of odd and even columns in a selected row,

a second video bus for transmitting analog pixel signals of a negative polarity for the liquid crystal pixels of the other one of the odd and even columns in the selected row,

a plurality of sample-hold units each assigned to corresponding adjacent two of said signal lines to simultaneously sample-hold the pixel signals transmitted through said first and second video buses, and

a timing control circuit for sequentially enabling the operations of said sample-hold units;

each sample-hold unit includes a first switch circuit for causing the first and second video buses to be respectively connected to one of the adjacent two signal lines and the other one of the adjacent two signal lines, and a second switch circuit for causing the first and second video buses to be respectively connected to the other one of the adjacent two signal lines and the one of the adjacent two signal lines;

said timing control circuit includes changing means for periodically switching between the first and second switch circuits of each sample-hold unit;

a preset number of bus groups each constituted by said first and second video buses are provided;

said sample-hold units are divided into blocks each constituted by the preset number of adjacent sample-hold units for sample-holding the pixel signals transmitted by the first and second video buses of different bus groups; and

said timing control circuit is arranged to sequentially enable the operations of said blocks.

* * * * *

US006380917B2

(12) **United States Patent**
Matsueda et al.

(10) **Patent No.: US 6,380,917 B2**
(45) **Date of Patent: *Apr. 30, 2002**

(54) **DRIVING CIRCUIT OF ELECTRO-OPTICAL DEVICE, DRIVING METHOD FOR ELECTRO-OPTICAL DEVICE, AND ELECTRO-OPTICAL DEVICE AND ELECTRONIC EQUIPMENT EMPLOYING THE ELECTRO-OPTICAL DEVICE**

(75) Inventors: **Yojiro Matsueda**, Chino; **Tokuroh Ozawa**, Suwa, both of (JP)

(73) Assignee: **Seiko Epson Corporation**, Tokyo (JP)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/202,517**

(22) PCT Filed: **Apr. 16, 1998**

(86) PCT No.: **PCT/JP98/01729**

§ 371 Date: **Dec. 17, 1998**

§ 102(e) Date: **Dec. 17, 1998**

(87) PCT Pub. No.: **WO98/48317**

PCT Pub. Date: **Oct. 29, 1998**

(30) **Foreign Application Priority Data**

Apr. 18, 1997 (JP) 9-102293

(51) **Int. Cl.**[7] **G09G 3/36**

(52) **U.S. Cl.** **345/89**; 345/211; 345/210; 345/95

(58) **Field of Search** 345/87, 88, 89, 345/98, 99, 100, 147, 204, 205, 211, 94, 95, 208, 210

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,937,578	A	6/1990	Shioda
5,017,914	A	5/1991	Uchida et al.
5,396,123	A	3/1995	Minamizaki

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

EP	0-483-972	A	9/1991
EP	0 601 713	A	6/1994
FR	2-698-202	A	11/1992
GB	2-217-128	A	10/1989

(List continued on next page.)

OTHER PUBLICATIONS

Matsueda, Y., et al. "Low–Temperature Poly–Si TFT–LCD with Integrated 6–bit Digital Data Drivers", *SID 96 Digest*, pp. 21–24.

Electronics and Communications in Japan, Part II: Electronics, "Poly–Si TFT and Driver Integration Technology," H. Ohshima et al.; vol. 77, No. 7, Jul. 1994,New York, pp. 46–54.

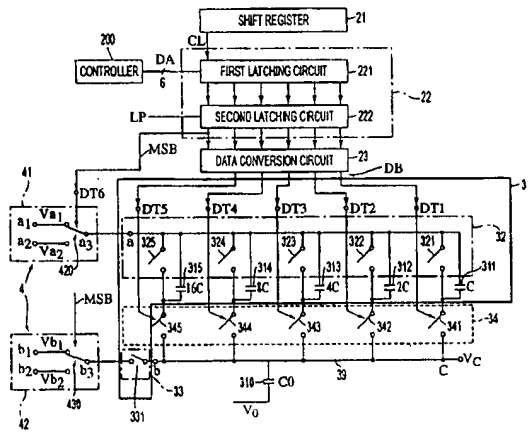
(List continued on next page.)

Primary Examiner—Xiao Wu
(74) *Attorney, Agent, or Firm*—Oliff & Berridge, PLC

(57) **ABSTRACT**

A driving circuit of an electro-optical device such as a liquid crystal device is compatible with digital image signals and implements a DA converting function and a γ correcting function by a relatively simple and small-scale circuit configuration. The driving circuit of the liquid crystal device is provided with a DAC 3 for issuing a voltage signal V_C corresponding to N bits of digital image data D_A that indicate a gray scale value to a signal line of the liquid crystal device. Depending on whether the value of a most significant bit is "0" or "1," the DAC 3 brings the output driving voltage characteristic close to the optical characteristics of the liquid crystal device according to the a pair of first or second reference voltages so as to make a γ correction.

33 Claims, 17 Drawing Sheets



U.S. PATENT DOCUMENTS

5,453,757	A		9/1995	Date et al.
5,648,791	A	*	7/1997	Date et al. 345/89
5,680,149	A		10/1997	Koyama et al.
5,686,936	A		11/1997	Maekawa et al.
5,764,207	A		6/1998	Maekawa et al.
5,796,384	A	*	8/1998	Kim 345/147
6,061,046	A	*	5/2000	An 345/98

FOREIGN PATENT DOCUMENTS

JP	A 57-52228	3/1982
JP	A 58-97918	6/1983
JP	A-59-107628	6/1984
JP	A-62-131233	6/1987
JP	A-63-52121	3/1988
JP	A-01-009375	1/1989
JP	A-1-233919	9/1989
JP	A-2-154292	6/1990
JP	A-2-226975	9/1990
JP	A-2-245794	10/1990
JP	A-3-190429	8/1991
JP	A-3-214818	9/1991
JP	A-4-46386	2/1992
JP	A-4-195189	7/1992
JP	A-5-94159	4/1993
JP	A-5-100635	4/1993
JP	A-5-102857	4/1993
JP	A 5-303080	11/1993
JP	A 6-59648	3/1994
JP	A-6-75543	3/1994
JP	A-6-178238	6/1994
JP	A-6-222741	8/1994
JP	A 6-268522	9/1994
JP	A2 7191303	7/1995
JP	A-7-261714	10/1995
JP	A-7-295520	11/1995
JP	A-7-295521	11/1995
JP	A-8-227283	9/1996
JP	A-8-234697	9/1996
JP	A-8-286641	11/1996
JP	A-9-73283	3/1997
JP	A-9-179530	7/1997
WO	WO A1 9503629	2/1995

OTHER PUBLICATIONS

Review of the Electrical Communication Laboratories, "A 10–In. Diagonal Active Matrix Monochrome Liquid–Crystal Display," S. Sakai et al.; vol. 36, No. 4, Jul. 1988, Tokyo, pp. 395–401.

Nikkei Business Publications, Inc., "Driver LSI Problems Solved by Low Voltage Single Power Supply", *Flat Panel Display 1991* , Nov. 26, 1990, pp. 168–172.

Nikkei Business Publications, Inc., "A 13–inch EWS High–Definition TFT Liquid Crystal Panel with Improved Picture Quality by Means of Dot Inversion Driving", *Flat Panel Display 1993*, Dec. 10, 1992, pp. 120–123.

* cited by examiner

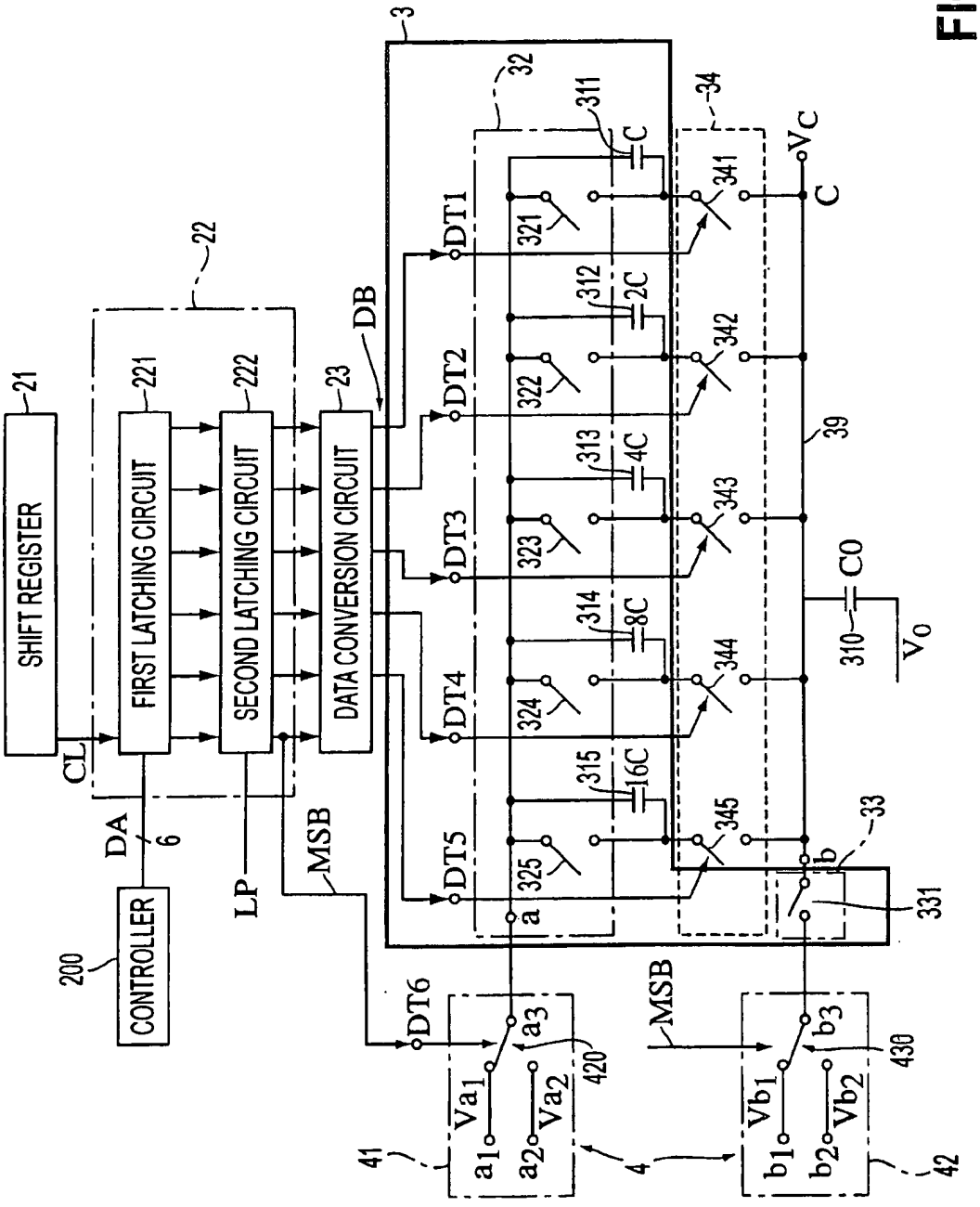

SHIFT REGISTER
FIRST LATCHING CIRCUIT
SECOND LATCHING CIRCUIT
DATA CONVERSION CIRCUIT
CONTROLLER
CL
DA
LP
MSB
DB
DT1
DT2
DT3
DT4
DT5
DT6
C
2C
4C
8C
16C
CO
VC
VO
Va1
Va2
Va3
Vb1
Vb2
Vb3
a1
a2
a3
b1
b2
b3
a
b
21
22
221
222
23
200
3
32
33
34
39
41
42
4
420
430
331
310
311
312
313
314
315
321
322
323
324
325
341
342
343
344
345

FIG. 1

FIG. 2

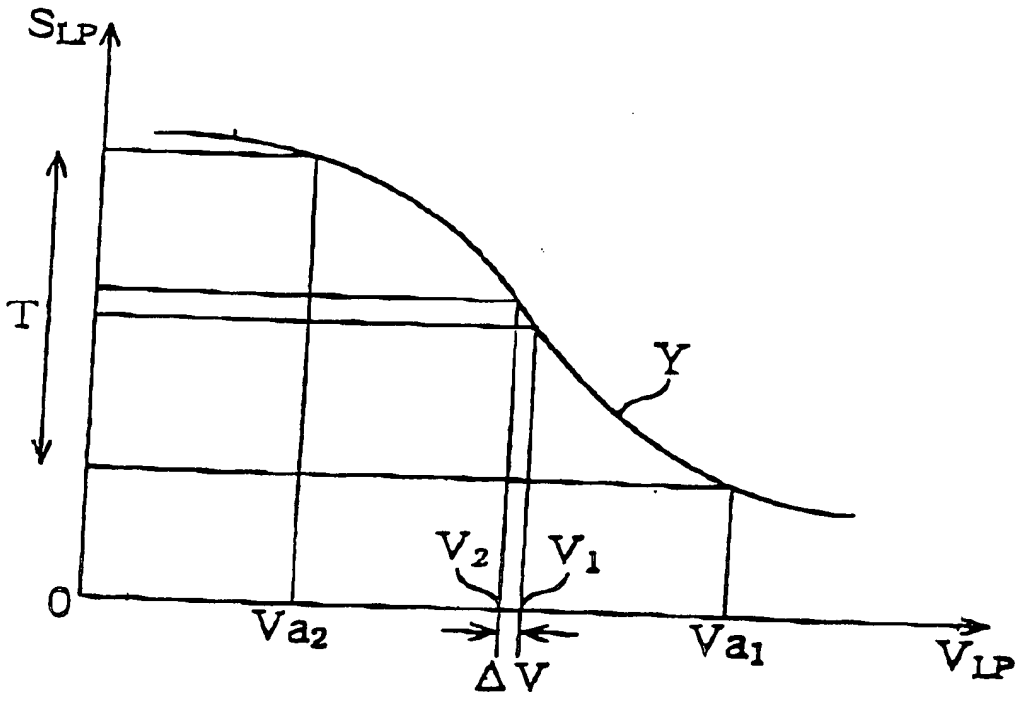
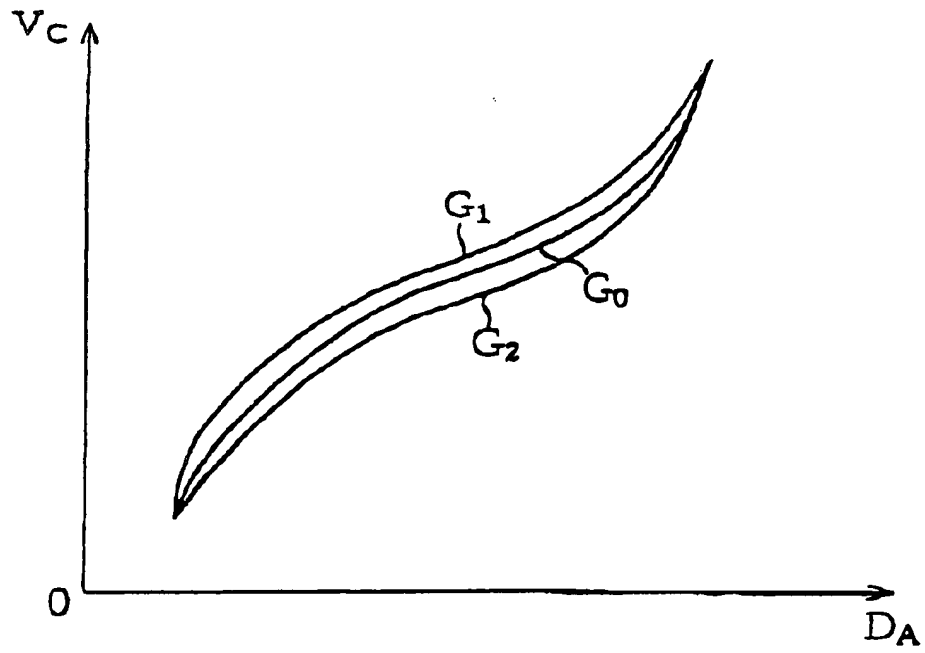
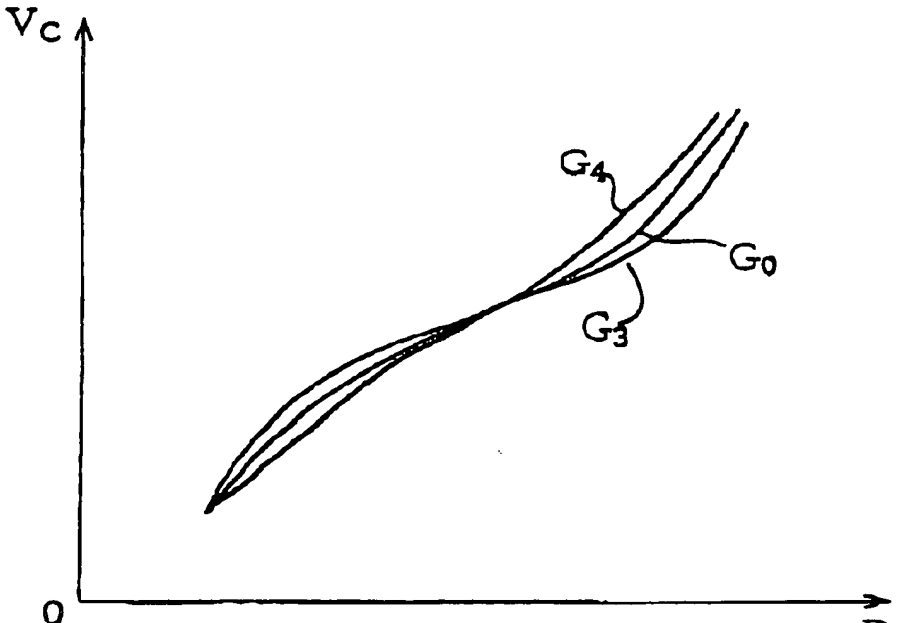


FIG. 3



(A)



(B)

FIG. 4

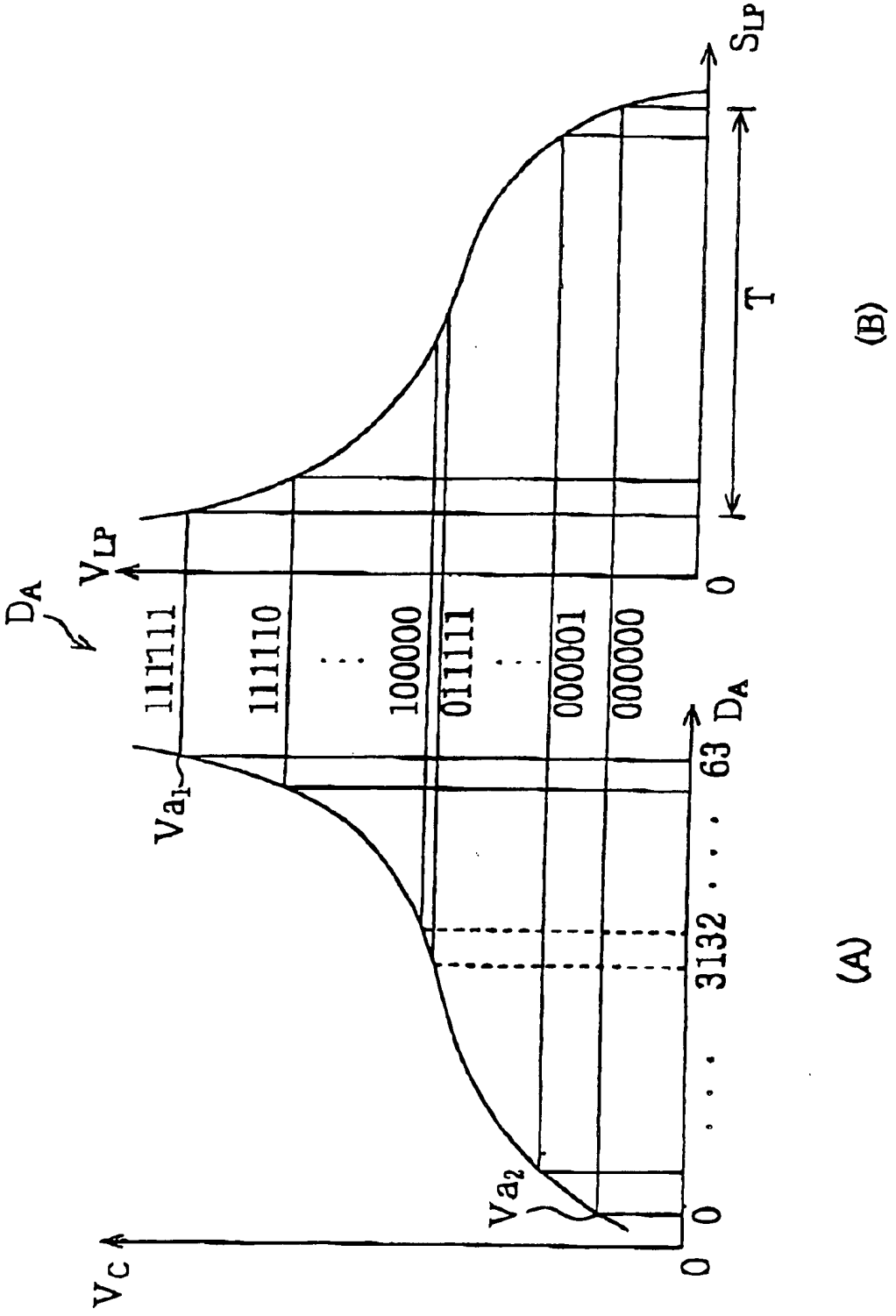

S_{LP}
T
(B)
V_{LP}
D_A
111111
111110
100000
011111
000001
000000
0
Va_1
D_A
63
3132
0
Va_2
V_C
0
(A)

FIG. 5

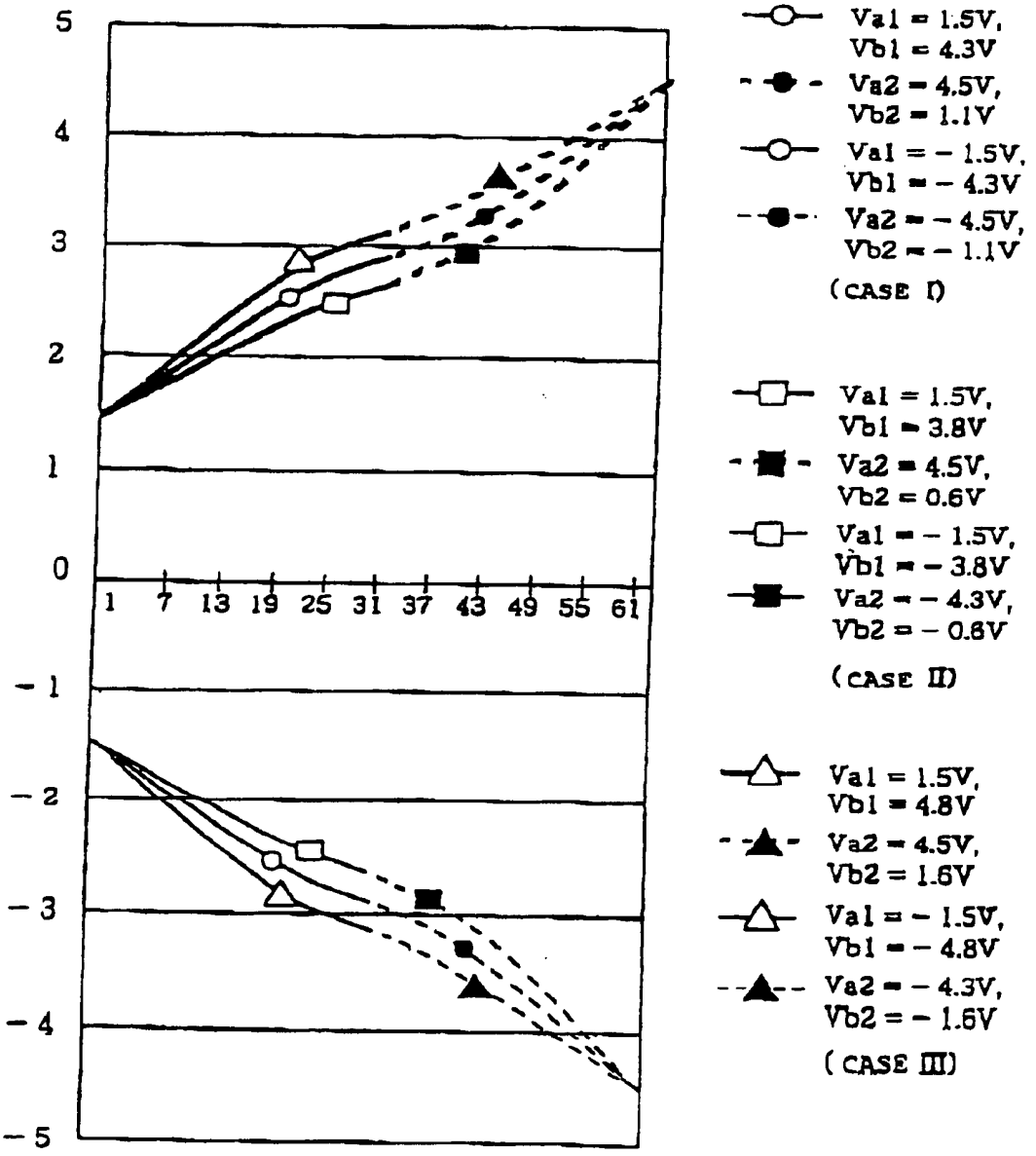

5
4
3
2
1
0
−1
−2
−3
−4
−5
1
7
13
19
25
31
37
43
49
55
61
Va1 = 1.5V,
Vb1 = 4.3V
Va2 = 4.5V,
Vb2 = 1.1V
Va1 = − 1.5V,
Vb1 = − 4.3V
Va2 = − 4.5V,
Vb2 = − 1.1V
(CASE I)
Va1 = 1.5V,
Vb1 = 3.8V
Va2 = 4.5V,
Vb2 = 0.6V
Va1 = − 1.5V,
Vb1 = − 3.8V
Va2 = − 4.3V,
Vb2 = − 0.8V
(CASE II)
Va1 = 1.5V,
Vb1 = 4.8V
Va2 = 4.5V,
Vb2 = 1.6V
Va1 = − 1.5V,
Vb1 = − 4.8V
Va2 = − 4.3V,
Vb2 = − 1.6V
(CASE III)

FIG. 6

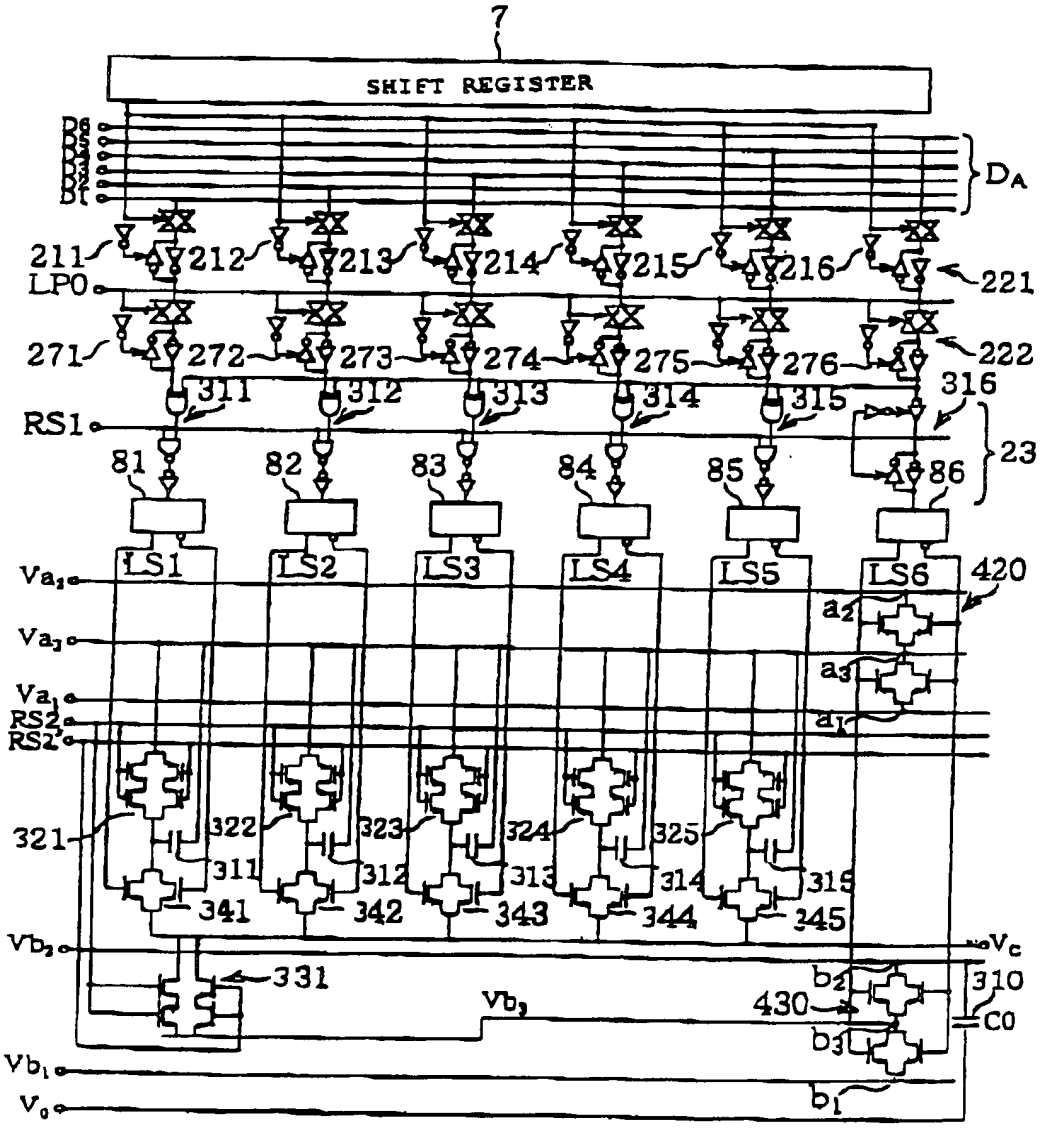

7
SHIFT REGISTER
D6
D5
D4
D3
D2
D1
DA
211
212
213
214
215
216
221
LP0
271
272
273
274
275
276
222
311
312
313
314
315
316
RS1
81
82
83
84
85
86
23
LS1
LS2
LS3
LS4
LS5
LS6
420
Va1
Va2
Va3
RS2
RS2'
321
322
323
324
325
311
312
313
314
315
341
342
343
344
345
Vb2
Vc
331
Vb3
430
b2
b3
310
C0
Vb1
V0
b1

FIG. 7

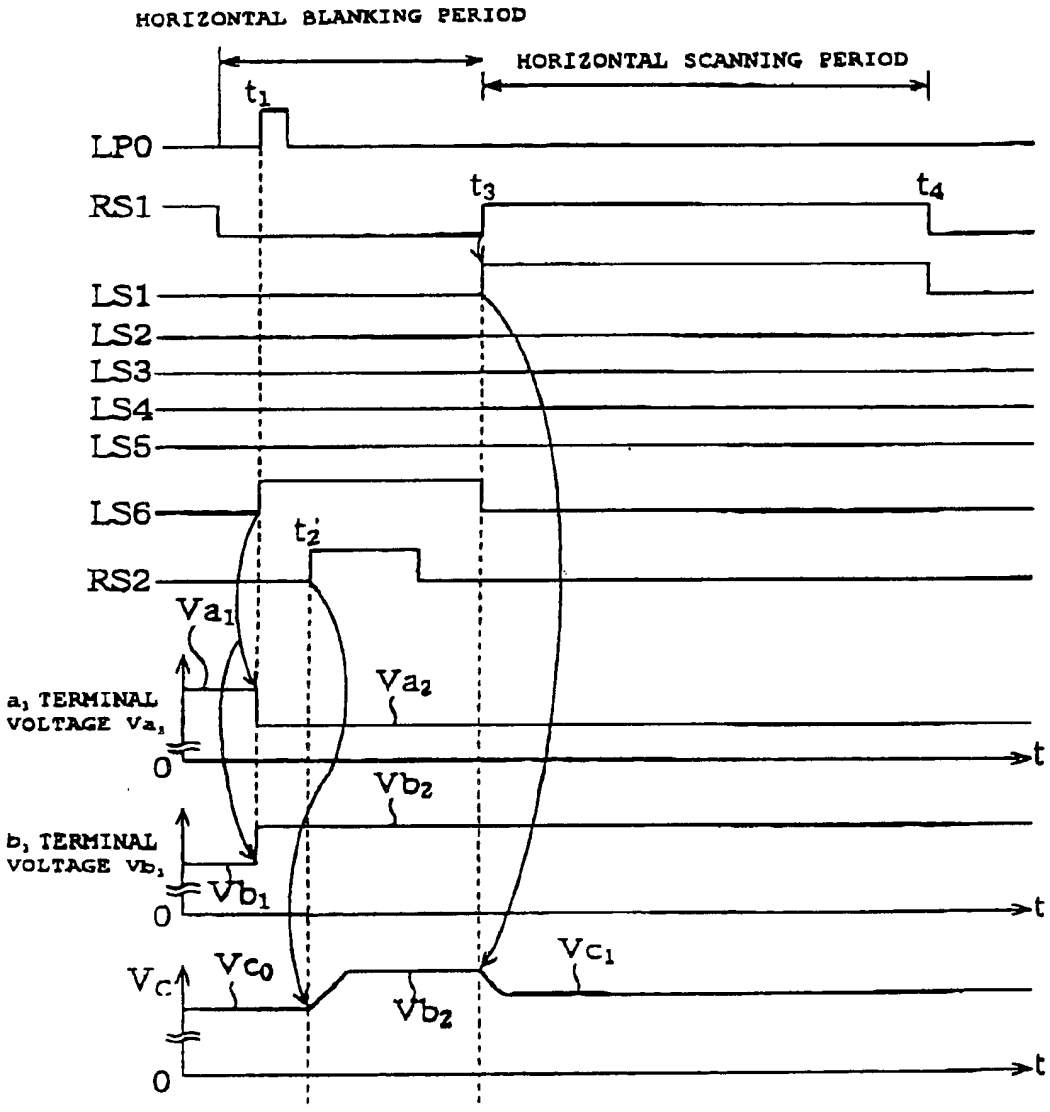

HORIZONTAL BLANKING PERIOD
HORIZONTAL SCANNING PERIOD
t1
t3
t4
t2'
LP0
RS1
LS1
LS2
LS3
LS4
LS5
LS6
RS2
Va1
Va2
a1 TERMINAL VOLTAGE Va1
Vb2
b1 TERMINAL VOLTAGE Vb1
Vb1
Vc0
Vc1
Vc
Vb2
0
t

FIG. 8

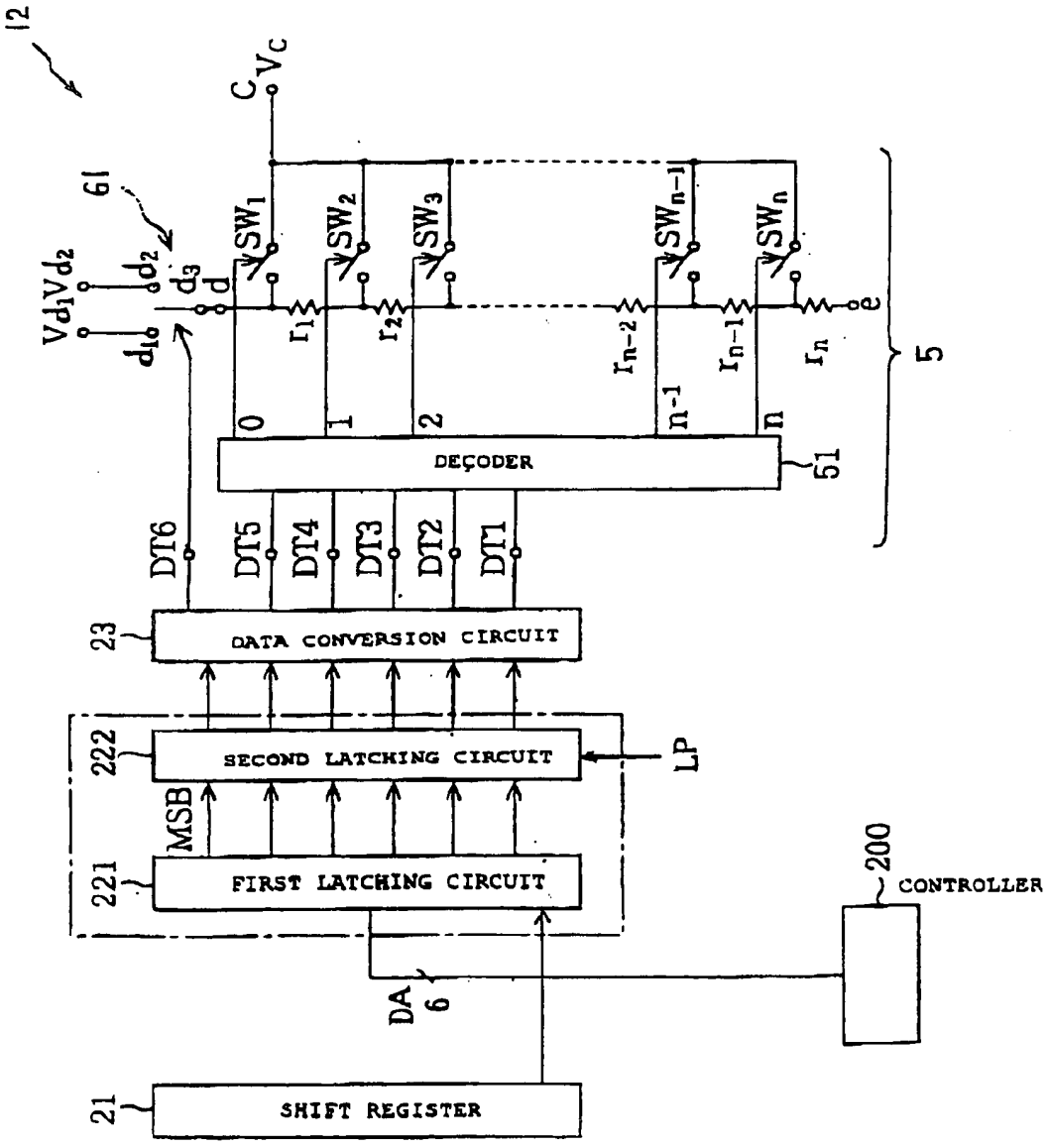

12
C
Vc
61
SW1
SW2
SW3
SWn-1
SWn
Vd1
Vd2
d2
d3
d
d1
r1
r2
rn-2
rn-1
rn
e
5
0
1
2
n-1
n
DECODER
51
DT6
DT5
DT4
DT3
DT2
DT1
23
DATA CONVERSION CIRCUIT
222
SECOND LATCHING CIRCUIT
LP
MSB
221
FIRST LATCHING CIRCUIT
200
CONTROLLER
DA
6
21
SHIFT REGISTER

FIG. 9

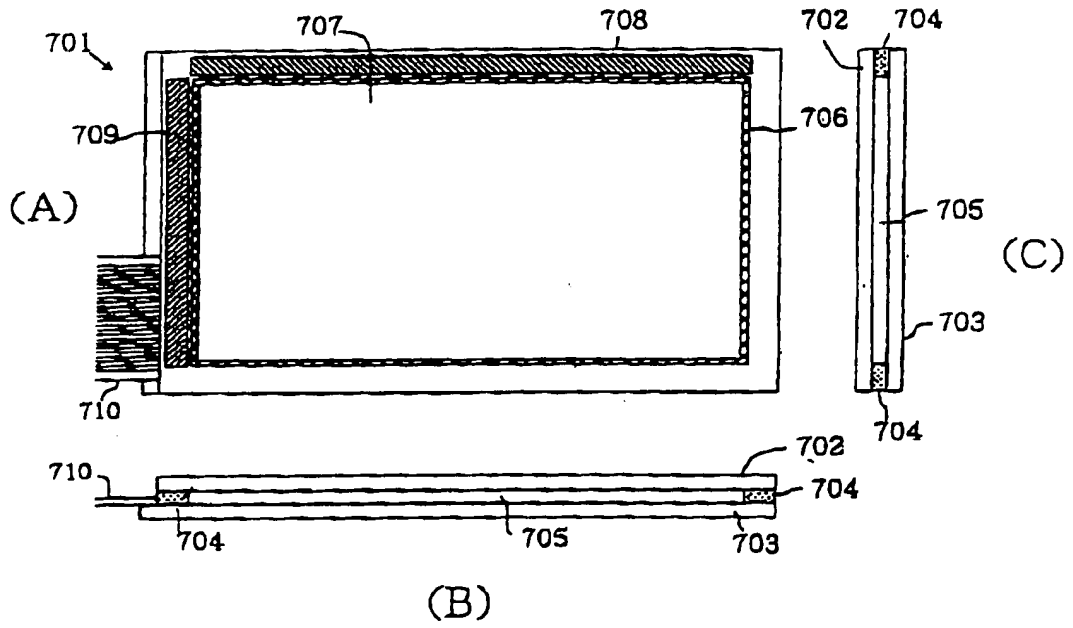

701
707
708
702
704
709
706
(A)
705
(C)
703
710
704
710
702
704
704
705
703
(B)

FIG. 10

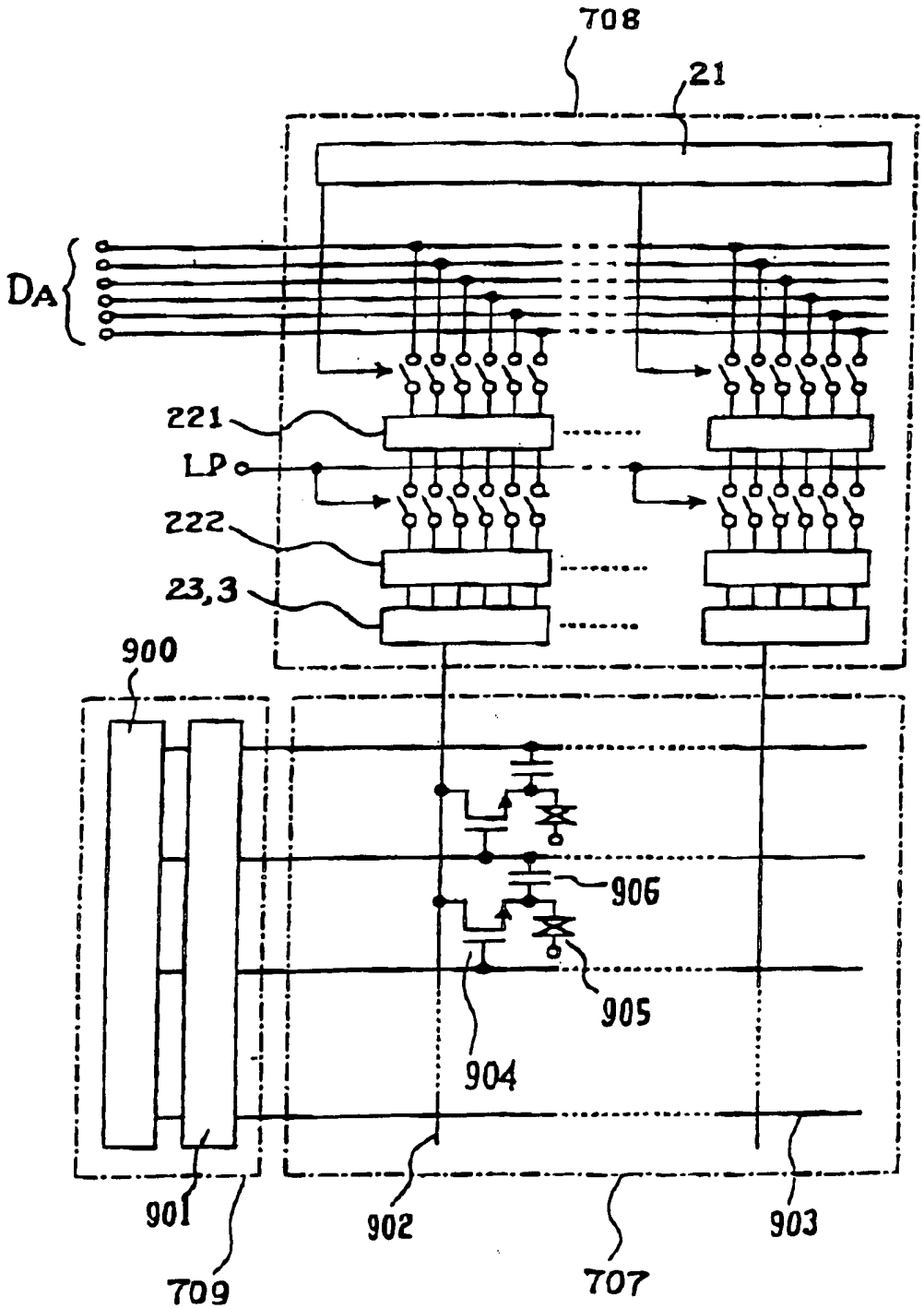


FIG. 11

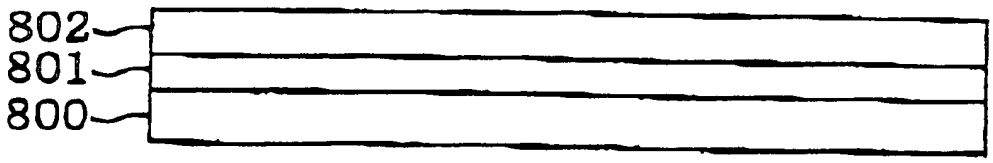


FIG. 12

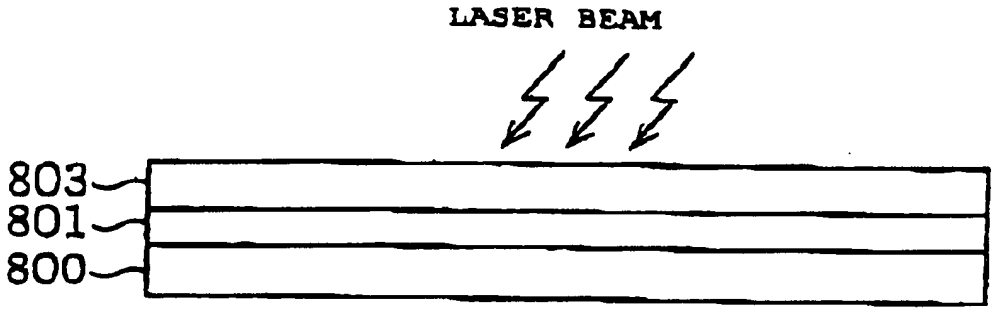


FIG. 13

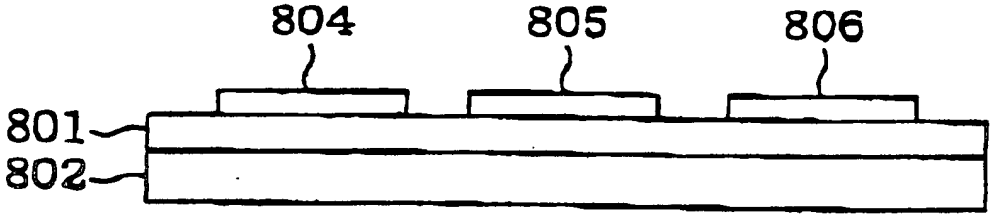


FIG. 14

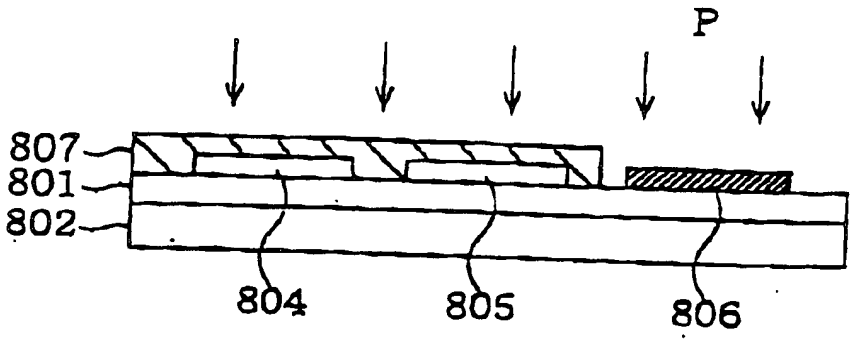


FIG. 15

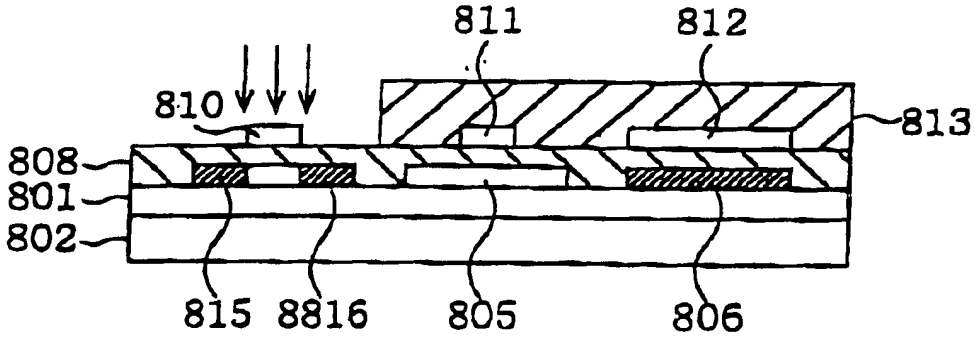


FIG. 16

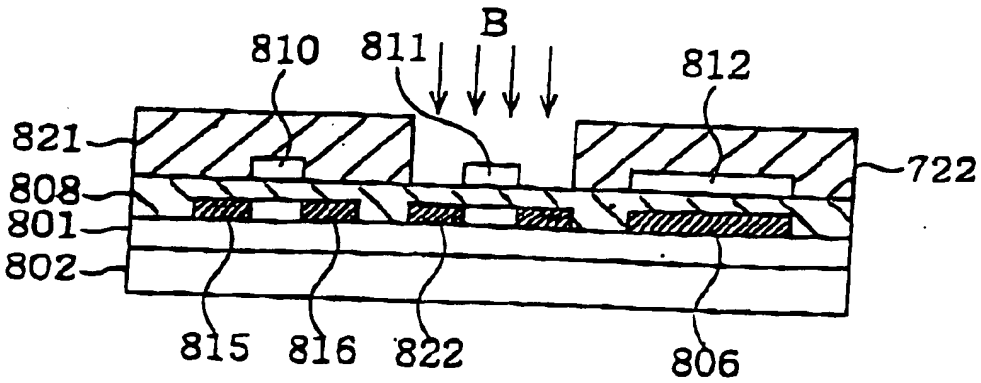
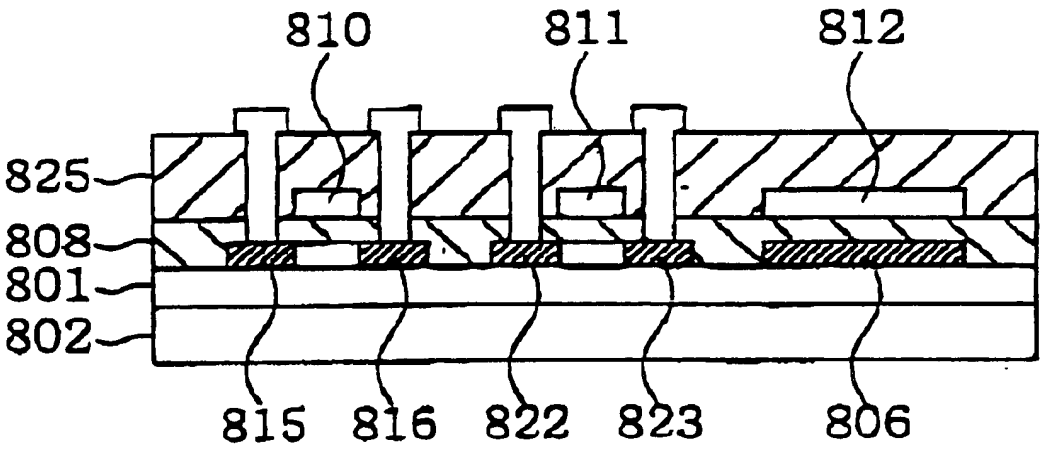


FIG. 17



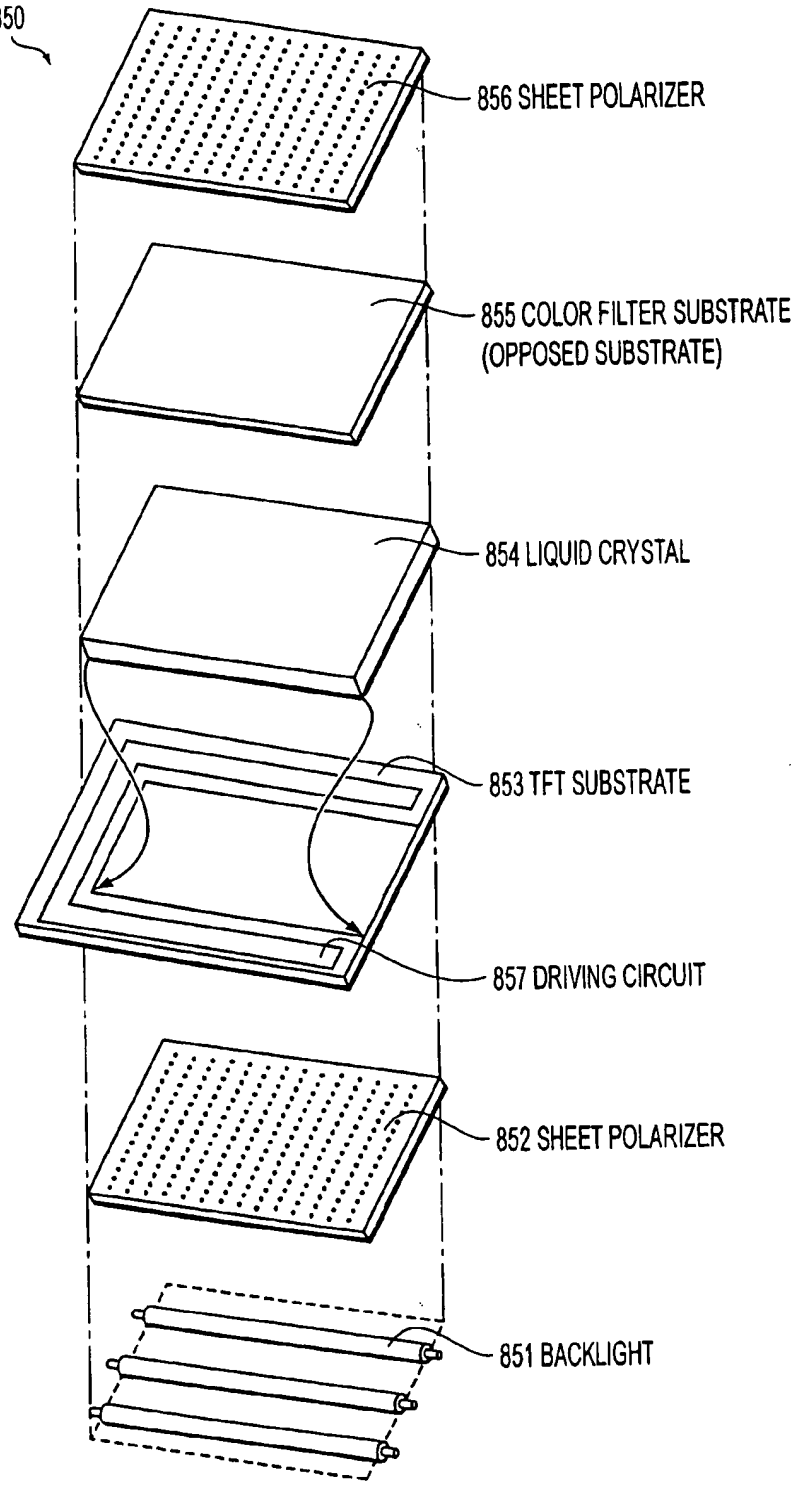

850
856 SHEET POLARIZER
855 COLOR FILTER SUBSTRATE
(OPPOSED SUBSTRATE)
854 LIQUID CRYSTAL
853 TFT SUBSTRATE
857 DRIVING CIRCUIT
852 SHEET POLARIZER
851 BACKLIGHT

FIG. 18

FIG. 19

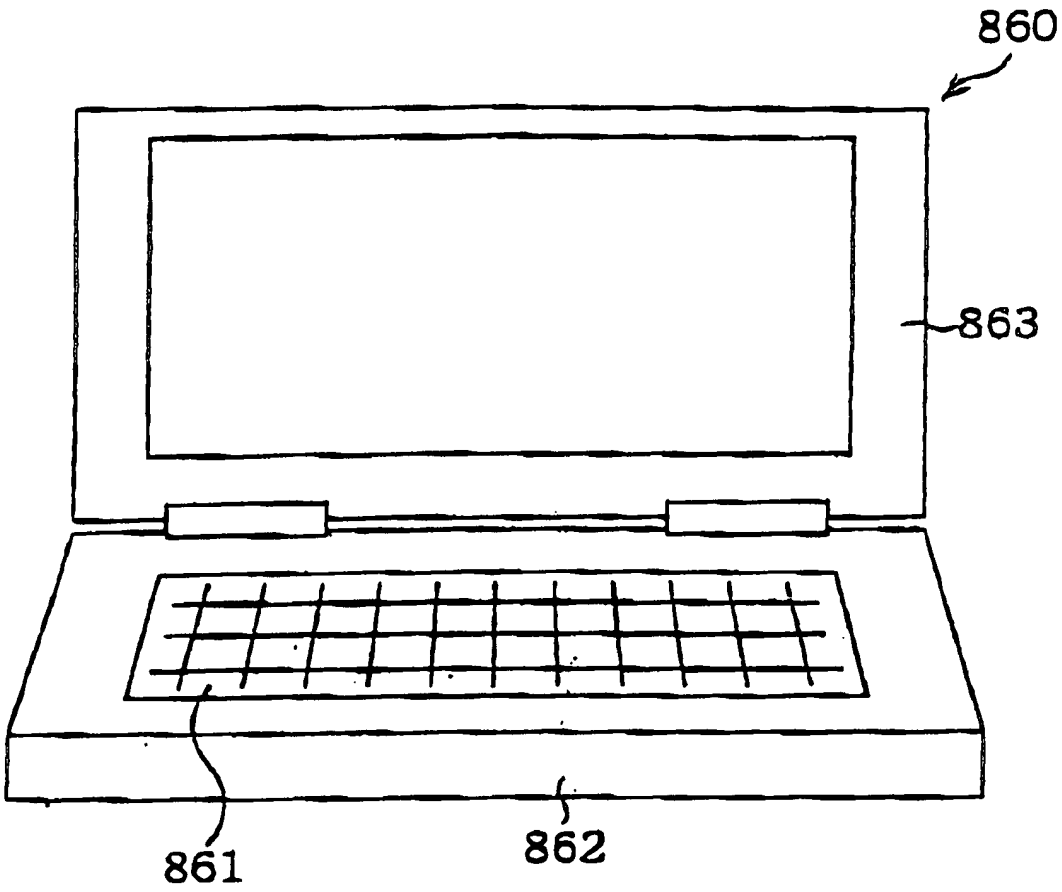


FIG. 20

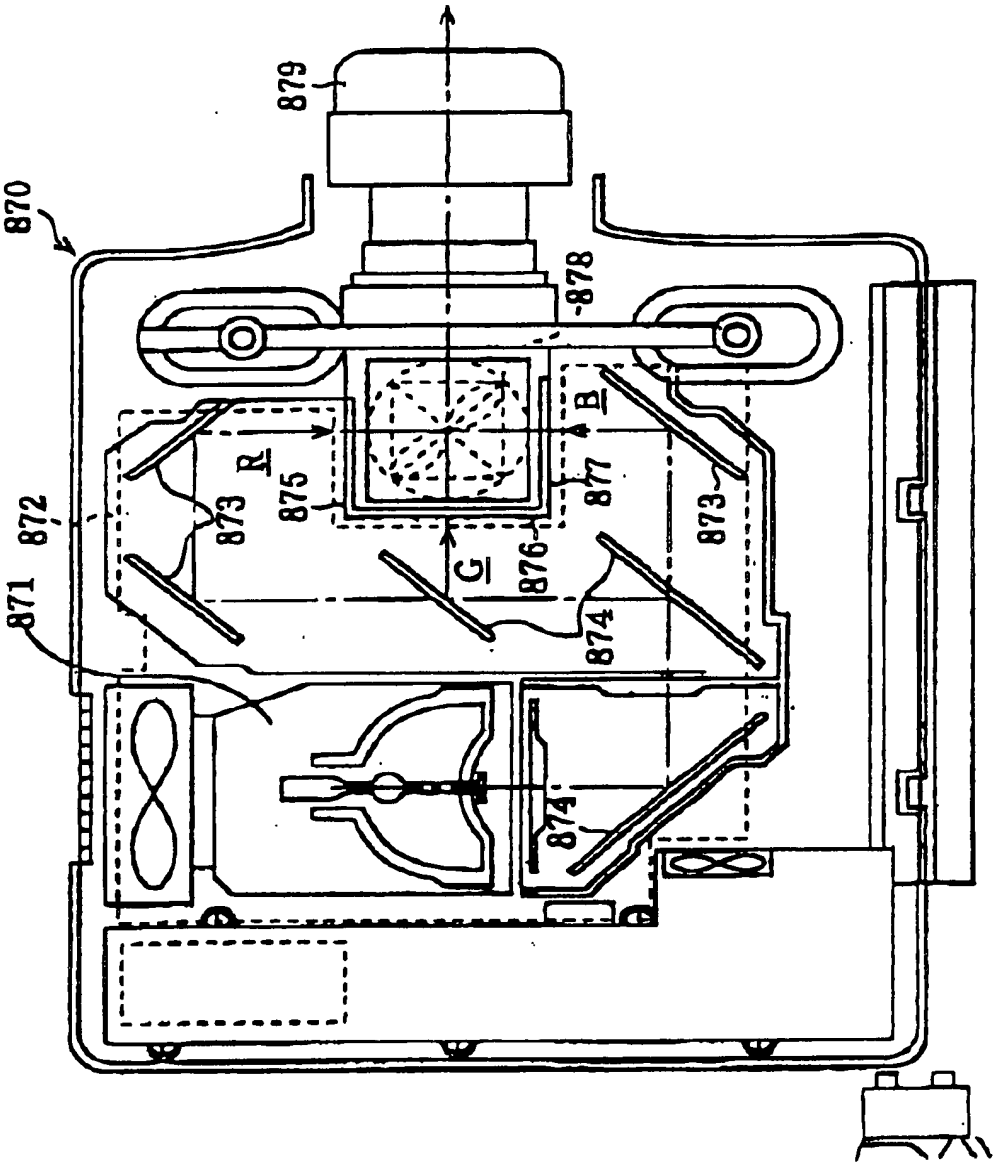
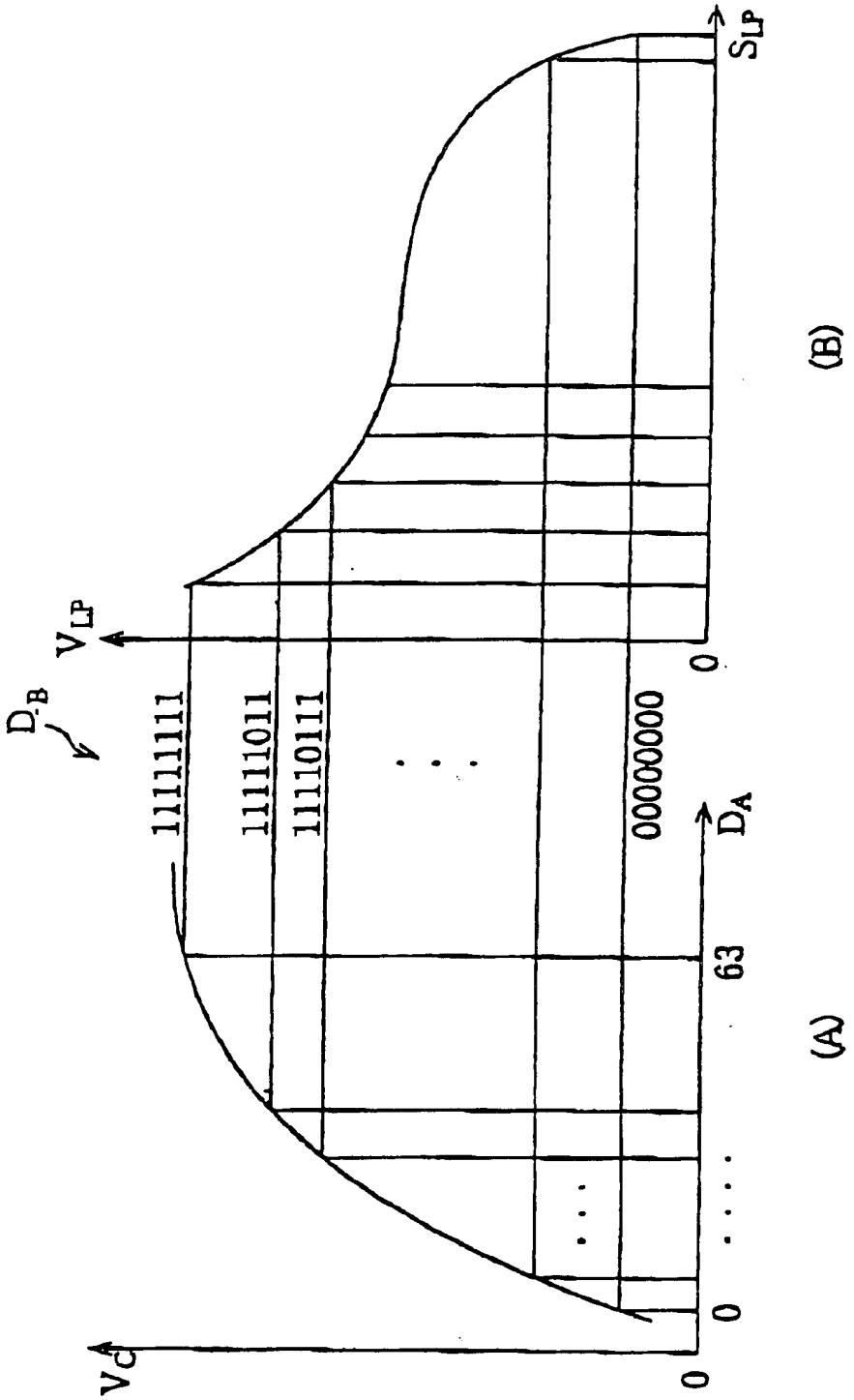


FIG. 21



DRIVING CIRCUIT OF ELECTRO-OPTICAL DEVICE, DRIVING METHOD FOR ELECTRO-OPTICAL DEVICE, AND ELECTRO-OPTICAL DEVICE AND ELECTRONIC EQUIPMENT EMPLOYING THE ELECTRO-OPTICAL DEVICE

BACKGROUND OF THE INVENTION

1. Field of Invention

The present invention relates to a technical field of a driving circuit and a driving method for driving an electro-optical device such as a liquid crystal device, the electro-optical device, and electronic equipment employing the electro-optical device and, more particularly, to a driving circuit and a driving method of an electro-optical device that receives a digital image signal and has a DA (Digital to Analog) converting function and a γ correcting function for an electro-optical device, the electro-optical device, and electronic equipment using the electro-optical device.

2. Description of Related Art

Hitherto, as a driving circuit for driving a liquid crystal device, which is an example of one type of electro-optical device, there is available, for example, a so-called digital driving circuit configured to receive digital image data indicating an arbitrary step of gray scale among a plurality of steps of gray scale, generate analog image data having a driving voltage corresponding to the step of gray scale, and supply the generated analog image data to a signal line of the liquid crystal device. Such a driving circuit is usually provided with a digital-to-analog converter (hereinafter referred to as "DA converter" or "DAC" as necessary) for converting digital image data to analog image data; it is configured to latch the digital image data, which has been input via a digital interface, by a latching circuit, then subject it to analog conversion through a switched capacitor type DA converter (hereinafter referred to as "SC-DAC" (Switched Capacitor—DAC: switch control capacity type DAC) as necessary), a DAC composed of a resistance ladder circuit or the like.

In a liquid crystal device or the like, the changes in optical characteristics (transmittance, optical density, luminance or the like) with respect to the changes in the driving voltage (or a voltage applied to the liquid crystal) are generally nonlinear according to the saturation characteristic or threshold value characteristic that the liquid crystal or the like has and they exhibit a so-called "γ characteristic." Hence, this type of driving circuit is normally provided with γ correcting means for making a correction on digital image data in a stage preceding the latching circuit.

The γ correcting means, for example, carries out γ correction on 6-bit digital image data D_A by referring to a table stored in RAM or ROM so as to convert it into 8-bit digital image data D_B ($D\gamma1, D\gamma2, \ldots, D\gamma8$). The processing by the γ correcting means is implemented, considering the input/output characteristics of the DAC and the characteristic of the transmittance of liquid crystal pixels with respect to the voltage applied to a signal line (characteristics of transmittance vs. the voltage applied to liquid crystal). The transmittance characteristic of the liquid crystal pixels refers to the characteristic of changes in the transmittance of light obtained by transmitting through a liquid crystal layer with respect to the voltage applied to the liquid crystal layer held between a pair of substrates (transmitting through polarizer if they are disposed outside the substrates as necessary).

On the other hand, the aforesaid SC-DAC is constituted by a plurality of capacitive elements disposed in parallel.

The respective capacitive elements have binary ratios of, for example, 2^0C, $2C$, 2^2C, 2^4C and so on. Using these capacitive elements, a pair of reference voltages are subjected to voltage division or the like (charge share) thereby to output analog image data having a driving voltage that changes according to the changes in the gray scale of image data D_B. The DAC such as the SC-DAC configured as described above is connected to a signal line of a liquid crystal device or the like; a buffer circuit or the like is provided between the output terminal of the DAC and the signal line so as to protect the output voltage from the influences of the parasitic capacitance of the signal line.

As set forth above, the driving circuit causes a voltage corresponding to the digital image data D_B to be applied to the respective signal lines of a liquid crystal device or the like.

Graph (A) on the left in FIG. 21 shows the relationship between the decimal values of image data D_A and output voltage Vc of the DAC; graph (B) on the right in FIG. 21 shows the relationship between transmittance S_{LP} of liquid crystal pixels and voltage V_{LP} applied to the signal line (the axis of the transmittance is based on the logarithm). At the center in FIG. 21, the binary values of 8-bit digital image data D_B are given between the two graphs (A) and (B).

In graph (B) on the right in FIG. 21, 2^6 pieces of 8-bit data capable of distinguishably representing the transmittance characteristic of the liquid crystal pixels are selected among 2^8 pieces of 8-bit data obtained from the 8-bit input data to make the γ correction and the selected pieces of data are tabulated. And when 6-bit image data D_A is input, the γ correcting means converts it into 8-bit data D_B according to the table and outputs it to the DAC. More specifically, image data D_A is represented in 64-step gray scale; therefore, the foregoing conversion is carried out so that the data D_A for 64 steps of gray scale may be specified among the 256 steps of gray scale that can be represented by image data D_B in order to provide even changing ratio of the transmittance in the liquid crystal when image data D_A expressed in the 64-step gray scale is changed.

Thus, FIG. 21 illustrates the correspondence relationship between the 6-bit image data D_A and the 8-bit image data D_B and output voltage Vc (equivalent to V_{LP}) of the DAC.

SUMMARY OF THE INVENTION

The foregoing conventional driving circuit, however, requires γ correcting means and RAM or ROM or the like for storing the conversion table for the γ correction which are provided in the stage preceding the latching circuit in order to make γ correction. These components, therefore, provide obstacles in an attempt to reduce the size of the driving circuit. It would be possible to make up the DAC by using many amplifiers so as to provide it with the γ correcting function without using the aforesaid SC-DAC. This, however, would pose such a problem as a more complicated circuit. In addition, forming operational amplifiers on a glass substrate tends to cause more variations in operating characteristics to occur.

Accordingly, it is an object of the present invention to provide a driving circuit of an electro-optical device that is compatible with digital image signals and has a relatively simple and small-scale circuit configuration to provide a DA converting function and a γ correcting function (or an auxiliary function for making a γ correction), the electro-optical device, and electronic equipment employing the electro-optical device.

To this end, according to one aspect of the present invention, there is provided a driving circuit of an electro-

optical device that supplies an analog image signal, which has a driving voltage corresponding to an arbitrary step of gray scale among 2^N (where N is a natural number) steps of gray scale, to a signal line of an electro-optical device in which the changes in the optical characteristics with respect to the changes in the driving voltage are nonlinear; the driving circuit of the electro-optical device being provided with: an input interface to which an N-bit digital image signal indicative of the arbitrary step of gray scale is applied; and a digital-to-analog converter that generates a voltage within a range of a pair of first reference voltages according to the bit value of the foregoing digital image signal to produce the driving voltage within a first driving voltage range corresponding to the step of gray scale of the digital image signal so that the changes in the driving voltage with respect to the changes in the step of gray scale of the digital image signal are nonlinear if the applied digital image signal indicates a step of gray scale from a first to m−1th (where "m" is a natural number and $1<m\leqq 2^N$), and generates a voltage within a range of a pair of second reference voltages according to the bit value of the foregoing digital image signal to produce the driving voltage that corresponds to the step of gray scale of the digital image signal and also lies within a second driving voltage range adjacent to the first driving voltage range so that the changes in the driving voltage with respect to the changes in the gray scale of the digital image signal are nonlinear if the digital image signal indicates a step of gray scale from an m-th to 2^N-th gray scale, and supplies the analog image signal having the generated driving voltage to the signal line.

According to another aspect of the present invention, there is provided a driving method of an electro-optical device having a digital-to-analog converter that supplies an analog image signal having a driving voltage corresponding to an arbitrary step of gray scale among 2^N (where N is a natural number) steps of gray scale to a signal line of the electro-optical device in which the optical characteristics thereof change nonlinearly with respect to the changes in the driving voltage, the driving method including the steps of:

inputting an N-bit digital image signal indicative of the arbitrary step of gray scale to the digital-to-analog converter;

generating, by the digital-to-analog converter, a voltage within the range of a pair of first reference voltages according to the bit value of the foregoing digital image signal to produce the driving voltage within a first driving voltage range corresponding to the step of gray scale of the digital image signal so that the changes in the driving voltage with respect to the changes in the step of gray scale of the digital image signal are nonlinear if the input digital image signal indicates a step of gray scale from a first to m−1th (where "m" is a natural number and $1<m\leqq 2^N$;

generating, by the digital-to-analog converter, a voltage within the range of a pair of second reference voltages according to the bit value of the foregoing digital image signal to produce the driving voltage that corresponds to the step of gray scale of the digital image signal and also lies within a second driving voltage range adjacent to the first driving voltage range so that the changes in the driving voltage with respect to the changes in the gray scale of the digital image signal are nonlinear if the digital image signal indicates a step of gray scale from the m-th to 2^N-th; and

supplying the analog image signal having the generated driving voltage to the signal line.

According to the driving circuit and driving method of an electro-optical device, the N-bit digital image signal indicating an arbitrary step of gray scale is supplied first via an input interface. Then, if the supplied digital image signal indicates a step of gray scale from the first to the m−1th, a voltage within the range of the pair of first reference voltages is selectively generated according to the bit value of the digital image signal by the digital-to-analog converter so as to produce the driving voltage that lies within the first driving voltage range. On the other hand, if the digital image signal indicates a step of gray scale from the m-th to the 2^N-th, then a voltage within the range of the pair of the second reference voltages is selectively generated according to the bit value of the digital image signal by the digital-to-analog converter so as to produce the driving voltage that lies within the second driving voltage range. And the analog image signal having the driving voltage thus generated is supplied to the signal line to drive the electro-optical device. At this time, the changes in the optical characteristics with respect to the changes in the driving voltage in the electro-optical device are nonlinear, and the changes in the driving voltage with respect to the changes in the gray scale of the digital image signal in the digital-to-analog converter are also nonlinear.

In general, the changes in the driving voltage (output) in response to the step of gray scale (input) in the digital-to-analog converter that divides the reference voltages become almost linear if the step of gray scale is low, whereas they tend to be saturated and exhibit, for example, asymptote-like nonlinearity as the step of gray scale becomes higher because of the parasitic capacitance of the signal line on the output side. On the other hand, there are cases where the changes in the optical characteristics (output) with respect to the driving voltage (input) in the electro-optical device show an S-shaped nonlinearity having its inflection point located at around the center thereof due to the saturation characteristic that most electro-optical devices have, a threshold value characteristic or the like. For instance, in the case of a liquid crystal device, the changes in the transmittance (an example of the optical characteristic) with respect to applied voltage in liquid crystal pixels exhibit the saturation characteristic in the areas in the vicinity of a maximum applied voltage and a minimum applied voltage, respectively; therefore, the changes show the S-shaped nonlinearity having its inflection point located at around the central voltage.

Accordingly, if a single reference voltage is divided in the digital-to-analog converter, it would be difficult to correct the nonlinearity of the optical characteristics (e.g. the S-shaped nonlinearity having its inflection point located at around the center thereof) in the electro-optical device by making use of the nonlinearity of the driving voltage (e.g. asymptote nonlinearity) because of the non-similarity between the two. According to the present invention, however, the nonlinearity of the driving voltage in the first driving voltage range obtained by generating the voltage within the range of the first reference voltage can be combined with the nonlinearity of the driving voltage in the second driving voltage range obtained by generating the voltage within the range of the second reference voltage so as to make the nonlinearity of the driving voltage over the entire first and second driving voltage ranges similar to a certain extent to the nonlinearity of the optical characteristics (in other words, it is possible to provide both nonlinearities with a change trend that is similar to a certain extent). In particular, by setting the voltage so that the polarities of the pair of the first reference voltages and the polarities of the pair of the second reference voltages are

opposite in relation to the digital-to-analog converter, the driving voltage with respect to the gray scale can be inflected at the boundary of the first and second driving voltage ranges.

Thus, it is possible to drive the electro-optical device by using a digital image signal as an input, and to correct the nonlinearity of the optical characteristics of the electro-optical device by making use of the nonlinearity of the driving voltage of the digital-to-analog converter according to the degree of the similarity between these nonlinearities. This means that the γ correction for the electro-optical device can be made by using the digital-to-analog converter.

According to the present invention as set forth above, it is not required to separately provide the γ correcting means in a stage preceding the digital-to-analog converter, which was required in the prior art. As an alternative, however, such a γ correcting means may be separately provided to make a γ correction in a first stage, and a γ correction in a second stage may be made by the foregoing digital-to-analog converter in accordance with the present invention. In this case, a rough γ correction may be made in one of these two stages, then a fine γ correction may be made in the other stage.

In a mode of the driving circuit in accordance with the present invention described above, the voltage polarities of the pair of the first reference voltages and the voltage polarities of the pair of the second reference voltages supplied to the digital-to-analog converter are set to be opposite from each other so that the changes in the driving voltage corresponding to the changes in the gray scale have the inflection points between the first and second driving voltage ranges.

According to this embodiment, the optical characteristics in the electro-optical device exhibit the S-shaped nonlinearity having the inflection point between the first and second driving voltage ranges. Meanwhile, the first and second reference voltages, in which the voltage polarities of the reference voltages are opposite to each other, are supplied to the digital-to-analog converter; hence, the driving voltage in the digital-to-analog converter also exhibits the S-shaped nonlinearity having the inflection point located between the first and second driving voltage ranges. Further, there is the change trend corresponding to the change in the S-shaped nonlinearity of the optical characteristics, thus making it possible to achieve a high level of correction of the nonlinearity of the optical characteristics in the electro-optical device by utilizing the nonlinearity of the driving voltage over the entire first and second driving voltage ranges.

In another embodiment of the driving circuit in accordance with the present invention described above, the value of "m" is equal to 2^{N-1} and lower N−1 bits of the digital image signal are selectively input to the digital-to-analog converter as they are or after being inverted according to the value of the most significant bit of the digital image signal. The digital-to-analog converter generates a voltage in the range of the first reference voltage if the lower N−1 bits are input thereto as they are, and it generates a voltage in the range of the second reference voltage if the lower N−1 bits are inverted before being input thereto.

According to the embodiment, the value of "m" is equal to 2^{N-1} In other words, the first half or the latter half of the 2^N steps of gray scale corresponds to the driving voltage in the first driving voltage range and the other half corresponds to the driving voltage in the second driving voltage range. In this case, lower N−1 bits of the digital image signal are selectively input to the digital-to-analog converter as they are or after being inverted, depending upon the binary value (i.e. depending upon whether the value is "0" or "1") of the most significant bit of the digital image signal. The digital-to-analog converter generates a voltage in the range of the first reference voltage to generate the driving voltage in the first driving voltage range if the lower N−1 bits are input thereto as they are. On the other hand, the digital-to-analog converter generates a voltage in the range of the second reference voltage to generate the driving voltage in the second driving voltage range if the lower N−1 bits are inverted before being input thereto. Hence, only one N−1 bit digital-to-analog converter is required as the digital-to-analog converter for converting N-bit digital image signals, making it extremely advantageous from the viewpoint of the composition of the device.

In this embodiment, a selective inverting circuit for selectively inverting the lower N−1 bits depending upon the value of the most significant bit may be further provided between the interface and the digital-to-analog converter.

In such a configuration, when a digital image signal is input via the interface, the selective inverting circuit selectively inverts the lower N−1 bits according to the value of the most significant bit. And the selectively inverted lower N−1 bits are input to the digital-to-analog converter which generates a voltage in the range of the first or second reference voltage so as to generate a driving voltage in the first or second driving voltage range.

Still another embodiment of the driving circuit in accordance with the present invention is further provided with a selective voltage supply circuit for selectively supplying either the first or second reference voltage to the digital-to-analog converter according to the value of the most significant bit of the digital image signal.

According to this embodiment, depending upon the value of the most significant bit of the digital image signal, the selective voltage supply circuit selectively supplies the first or second reference voltage to the digital-to-analog converter. Then, the digital-to-analog converter generates a voltage in the range of the first or second reference voltage selectively supplied so as to generate a driving voltage in the first or second driving voltage range. Thus, the portion of the digital-to-analog converter for selectively generating a voltage in the range of the first reference voltage can be commonly used as the portion of the digital-to-analog converter for selectively generating a voltage in the range of the second reference voltage, making it advantageous from the viewpoint of the composition of the device.

Yet another embodiment of the driving circuit in accordance with the present invention is further provided with, as the digital-to-analog converter, a switched capacitor type digital-to-analog converter adapted to generate the voltages in the ranges of the first and second reference voltages, respectively, by means of charging a plurality of capacitors.

According to this embodiment, the voltages in the ranges of the first and second reference voltages are generated by the plurality of capacitors of the switched capacitor type digital-to-analog converter. This makes it possible to generate driving voltages by relatively reliable, accurate voltage selection by using a relatively simple composition.

In this embodiment, the first reference voltage may be composed of a pair of voltages that enable a voltage in the first driving voltage range to be selectively generated, and the second reference voltage may be composed of a pair of voltages that enable a voltage in the second driving voltage range to be selectively generated.

Such a composition allows a voltage in the range of a pair of the first reference voltages to be generated by the plurality of capacitors of the switched capacitor type digital-to-analog converter, thereby providing a discrete driving voltage that

lies in the first driving voltage range. On the other hand, a voltage in the range of a pair of the second reference voltages is generated to provide a discrete driving voltage that lies in the second driving voltage range. Hence, desired first and second driving voltage ranges can be obtained according to the setting of the pair of the first reference voltages and the setting of the pair of the second reference voltages, and the gap between these ranges can be also reduced.

In this case, the value of the foregoing "m" is equal to 2^{N-1}, and the composition may be such that the lower N−1 bits of the digital image signal are selectively input to the switched capacitor type digital-to-analog converter as they are or inverted before being input thereto according to the value of the most significant bit of the digital image signal, and the switched capacitor type digital-to-analog converter generates a voltage in the range of the first reference voltage if the lower N−1 bits are input thereto as they are, and it generates a voltage in the range of the second reference voltage if the lower N−1 bits are inverted before being input thereto.

According to the configuration set forth above, the value of "m" is equal to 2^{N-1}, and the first half or the latter half of the 2^N steps of gray scale corresponds to the driving voltage in the first driving voltage range and the other half corresponds to the driving voltage in the second driving voltage range. In this case, lower N−1 bits of the digital image signal are selectively input to the switched capacitor type digital-to-analog converter as they are or after being inverted depending upon the value of the most significant bit of the digital image signal. And the switched capacitor type digital-to-analog converter generates a voltage in the range of the first reference voltage to generate a driving voltage in the first driving voltage range if the lower N−1 bits are input thereto as they are. On the other hand, the switched capacitor type digital-to-analog converter generates a voltage in the range of the second reference voltage to generate a driving voltage in the second driving voltage range if the lower N−1 bits are inverted before being input thereto. Hence, only one N−1 bit switched capacitor type digital-to-analog converter is required as the SC-DAC to convert an N-bit digital image signal, making it extremely advantageous from the viewpoint of the composition of the device.

In this case, the switched capacitor type digital-to-analog converter may be further provided with: a first through N−1th capacitive elements respectively having a pair of opposed electrodes, wherein one of the paired first reference voltages or one of the paired second reference voltages is selectively applied to one of the paired opposed electrodes according to the binary value of the most significant bit; a capacitive element resetting circuit for short-circuiting the pair of opposed electrodes in each of the first through N−1th capacitive elements so as to discharge electric charges; a signal line potential resetting circuit for selectively resetting the voltage of the signal line to the other of the paired first reference voltages or the other of the paired second reference voltages according to the binary value of the most significant bit; and a selective switching circuit including a first through N−1th switches that selectively connect the first through N−1th capacitive elements to the signal lines, respectively, according to the values of the lower N−1 bits after the discharge by the capacitive element resetting circuit and the resetting by the signal line potential resetting circuit.

According to the configuration set forth above, in each of the first through N−1th capacitive elements, one of the paired first reference voltages or one of the paired second reference voltages is selectively applied to one of the paired opposed electrodes according to the binary value of the most significant bit. First, the pair of the opposed electrodes are short-circuited and the electric charges are discharged in each of the first through N−1th capacitive elements by the capacitive element resetting circuit. On the other hand, the voltage of the signal line is selectively reset to the other of the paired first reference voltages or the other of the paired second reference voltages according to the binary value of the most significant bit by the signal line potential resetting circuit. After that, the first through N−1th capacitive elements are selectively connected to the signal lines by the first through N−1th switches of the selective switch circuit in accordance with the values of the lower N−1 bits. As a result, the voltages (positive or negative voltages) charged in the respective capacitive elements are applied as the driving voltages to the signal lines according to the steps of gray scale indicated by a digital image signal. Thus, it is possible to generate a driving voltage, which has been selected within the ranges of the reference voltages relatively reliably and accurately, by using a relatively simple composition.

Especially in this case, each of the capacitive elements constituting the switched capacitor type digital-to-analog converter are directly connected to the signal lines and the minimum electric charges required for charging the parasitic capacitance of the signal lines can be directly supplied from each of the capacitive elements. This is extremely advantageous in reducing the power consumed by the digital-to-analog converter and the driving circuit. In particular, the power consumption can be markedly reduced in comparison with the conventional case where a buffer circuit or the like is installed between the output terminal of the switched capacitor type digital-to-analog converter and the signal line to correct the nonlinearity of the driving voltage attributable to the parasitic capacitance of the signal line.

In this case, the capacitances of the first through N−1th capacitive elements may be set to $C\times 2^{i-1}$ (C: Predetermined unit capacitance; i=1, 2, . . . , N−1).

This configuration makes it possible to change a driving voltage, which is obtained by selective voltage generation, at predetermined intervals so as to enable the optical characteristics in the electro-optical device to be changed at the predetermined intervals. Hence, stable multi-step gray scale can be indicated over the entire gray scale range.

In another embodiment of the driving circuit in accordance with the present invention set forth above, the values of the first and second reference voltages are set so that the difference between the driving voltage corresponding to the m−1th step of gray scale and the driving voltage corresponding to the m-th step of gray scale is smaller than a predetermined value.

According to this embodiment, the difference between the driving voltage corresponding to the m−1th step of gray scale, i.e. a driving voltage that lies within the first driving voltage range and that is closest to the second driving voltage range at the same time, and the driving voltage corresponding to the m-th step of gray scale, i.e. a driving voltage that lies within the second driving voltage range and that is closest to the first driving voltage range at the same time, is smaller than the predetermined value. Therefore, by setting the predetermined value to a value that has been experimentally established in advance, e.g. to a value corresponding to a difference in gray scale that cannot be recognized by human, it becomes possible to prevent a practically discontinuous change in the gray scale at the gap between the first and second driving voltage ranges (i.e. the boundary of the two ranges).

In this embodiment, the values of the first and second reference voltages may be set so that the ratio of the optical

characteristics in the case where the electro-optical device is driven by the driving voltage corresponding to the m−1th step of gray scale and the case where the electro-optical device is driven by the driving voltage corresponding to the m-th step of gray scale is equal to one step of gray scale obtained by dividing the variation range of the optical characteristics by (2^N-1).

According to such a composition, the driving voltage obtained by selective voltage generation can be changed at predetermined intervals even before and after the boundary of the first and second driving voltage ranges, so that the optical characteristics in the electro-optical device can be changed at predetermined intervals. This means that highly stable multi-step gray scale display can be achieved over the entire gray scale range including the gray scale range corresponding to the boundary.

In a further embodiment of the driving circuit in accordance with the present invention described above, the digital-to-analog converter is provided with a resistance ladder that divides the first and second reference voltages, respectively, by a plurality of resistors connected in series.

According to this embodiment, the plurality of resistors of the resistance ladder generate the voltages in the ranges of the first and second reference voltages by dividing the voltages. Thus, the driving voltages can be generated relatively reliably and accurately by dividing voltages by using a relatively simple composition.

This embodiment may be further provided with a selective voltage supply circuit for selectively supplying either the first or the second reference voltage to the digital-to-analog converter according to the value of the most significant bit of the digital image signal. The digital-to-analog converter may be further provided with a decoder that decodes the lower N−1 bits of the digital image signal and outputs decoded signals through 2^{N-1} output terminals, and 2^{N-1} switches, one terminal of each of which is connected to each of a plurality of taps drawn out among the plurality of resistors and the other terminal thereof is connected to each of the signal lines and the 2^{N-1} switches being respectively operated according to the decoded signals output through the 2^{N-1} output terminals.

In this case, the selective voltage supply circuit selectively supplies either the first or the second reference voltage to the digital-to-analog converter according to the binary value of the most significant bit of the digital image signal. Then, in the digital-to-analog converter, the decoder decodes the lower N−1 bits of the digital image signal and outputs binary decoded signals respectively through the 2^{N-1} output terminals. Then, when the 2^{N-1} switches respectively connected between the plurality of taps respectively drawn out among the plurality of resistors and the signal lines are operated according to the decoded signals output through the 2^{N-1} output terminals, the first and second reference voltages are divided according to the gray scale indicated by the digital image signal. As a result, the voltages obtained by the voltage division by the respective resistors are applied as the driving voltages to the signal lines according to the gray scale indicated by the digital image signal. Thus, it becomes possible to generate a driving voltage by relatively reliable and accurate voltage division by using a relatively simple configuration.

Dividing the voltage by using the resistance ladder is especially advantageous because it eliminates the possibility of the reverse change of the driving voltage with respect to the change in the gray scale via the gap (boundary) of the first and second driving voltage ranges.

In another embodiment of the driving circuit in accordance with the present invention set forth above, the signal lines are provided with predetermined capacitors in addition to the parasitic capacitance of the signal lines.

According to this embodiment, the changes in the driving voltage (output) with respect to the changes in the gray scale (input) in the digital-to-analog converter generating voltages in the ranges of the reference voltages as previously described exhibit, for example, asymptoteshaped nonlinearity due to the parasitic capacitance of the signal lines located on the output side; therefore, adding the predetermined capacitance as mentioned above makes it possible to bring the nonlinearity of the driving voltage to a desired one or somewhat close to a desired one. The specific value of the predetermined capacitance for obtaining such desired nonlinearity may be set by carrying out experiments, simulations, or the like. Thus, the nonlinearity of the driving voltages in the first and second driving voltage ranges can be matched to each other by the nonlinearity of the optical characteristics by adjusting the additional capacitance of the signal lines in addition to the selective voltage generation carried out based on the two different reference voltages (namely, the first and second reference voltages). As a result, the nonlinearity of the optical characteristics can be corrected by making use of the nonlinearity of the driving voltage that is more similar thereto.

In a further embodiment of the driving circuit in accordance with the present invention described above, the electro-optical device is a liquid crystal device composed of liquid crystal held between a pair of substrates, and the driving circuit is formed on one of the paired substrates.

According to this embodiment, a digital image signal can be directly input, and the gray scale display on the liquid crystal device can be accomplished at relatively low power consumption by using a relatively simple configuration. Furthermore, the γ correction of the liquid crystal device can be also made.

In this embodiment, each of the first and second reference voltages may be supplied to the digital-to-analog converter with the voltage polarity with respect to a predetermined reference potential being inverted for each horizontal scanning period.

According to the configuration described above, each of the voltage polarity of the first reference voltage and that of the second reference voltage is switched for each horizontal scanning period when supplying the reference voltages to allow the liquid crystal device to be driven by a scanning line reversing drive (so-called "1H reversing drive") system, wherein the driving voltage is inverted for each scanning line, or a pixel reversing drive (so-called "dot inverting drive") system. This prevents the flickers on a display screen and also prevents other problems such as a deterioration in liquid crystal due to the application of DC voltage. The predetermined potential providing the reference for the polarity inversion in this case is approximately equal to the opposed potential applied to one electrode of a liquid crystal pixel, to which the driving voltage supplied from the driving circuit is applied, and the other electrode opposed to the foregoing electrode via a liquid crystal layer. However, in the case of a configuration where the voltages are applied to liquid crystal pixels via switching elements such as transistors or nonlinear elements, the foregoing predetermined potential is biased with respect to the opposed potential, considering a drop in the applied voltage attributable to the parasitic capacitance of the switching elements, or the like.

To solve the technical problems described above, an electro-optical device in accordance with the present invention is provided with the driving circuit described above in accordance with the present invention, so that it permits

direct input of a digital image signal, enabling an electro-optical device to be achieved that is capable of providing high-quality gray scale display at relatively low power consumption by using a relatively simple configuration.

To solve the technical problems described above, electronic equipment in accordance with the present invention is provided with the electro-optical device in accordance with the present invention described above, so that it makes it possible to accomplish various types of electronic equipment that has a relatively simple composition, consumes relatively low power, and is capable of providing high-quality gray scale display.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a circuit diagram showing an embodiment of a driving circuit employing an SC-DAC in accordance with the present invention.

FIG. **2** is a diagram illustrative of a method whereby two voltages corresponding to the minimum value and the maximum value of transmittance are determined from a transmittance characteristic curve of liquid crystal pixels.

FIG. **3**(A) is a diagram showing the changes in the output characteristic of the DAC observed when reference voltages are changed.

FIG. **3**(B) is a diagram showing the changes in the output characteristic of the DAC observed when the total capacitance of capacitive elements is changed.

FIG. **4** is a diagram showing the changes in the input/output characteristic of the DAC in the driving circuit of FIG. **1**; graph (A) on the left indicates the output voltage of the DAC with respect to image data, while graph (B) on the right indicates the voltage applied to liquid crystal pixel electrodes with respect to the transmittance of liquid crystal pixels.

FIG. **5** is a graph showing the relationship between the transmittance of the liquid crystal pixels and the voltage applied to the liquid crystal pixel electrodes in three cases (I through III).

FIG. **6** is a circuit diagram showing a detailed configuration of a first embodiment.

FIG. **7** is a timing chart illustrating the operation of the embodiment of FIG. **6**.

FIG. **8** is a circuit diagram showing a second embodiment of a driving circuit employing a resistance ladder type DAC in accordance with the present invention.

FIG. **9**(A) is a top plan view of an embodiment of a liquid crystal device in accordance with the present invention.

FIG. **9**(B) is a cross-sectional view of the liquid crystal device of FIG. **9**(A).

FIG. **9**(C) is a longitudinal sectional view of the liquid crystal device of FIG. **9**(A).

FIG. **10** is a circuit diagram of the liquid crystal device of FIG. **9**.

FIG. **11** is a schematic representation illustrative of a first step of the manufacturing process of the liquid crystal device shown in FIG. **9**.

FIG. **12** is a schematic representation illustrative of a second step of the manufacturing process of the liquid crystal device shown in FIG. **9**.

FIG. **13** is a schematic representation illustrative of a third step of the manufacturing process of the liquid crystal device shown in FIG. **9**.

FIG. **14** is a schematic representation illustrative of a fourth step of the manufacturing process of the liquid crystal device shown in FIG. **9**.

FIG. **15** is a schematic representation illustrative of a fifth step of the manufacturing process of the liquid crystal device shown in FIG. **9**.

FIG. **16** is a schematic representation illustrative of a sixth step of the manufacturing process of the liquid crystal device shown in FIG. **9**.

FIG. **17** is a schematic representation illustrative of a seventh step of the manufacturing process of the liquid crystal device shown in FIG. **9**.

FIG. **18** is a schematic exploded view of another embodiment of the liquid crystal device in accordance with the present invention.

FIG. **19** is a schematic representation showing an embodiment (portable computer) of electronic equipment in accordance with the present invention.

FIG. **20** is a schematic representation showing another embodiment (projector) of the electronic equipment in accordance with the present invention.

FIG. **21** is a diagram illustrative of the input/output characteristics of a DAC used for a conventional driving circuit; graph (A) on the left shows the output voltage of the DAC with respect to image data, while graph (B) on the right shows the voltage applied to a liquid crystal pixel electrode with respect to the transmittance of a liquid crystal pixel.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The following will describe embodiments of the best modes for embodying the present invention in conjunction with the accompanying drawings.

(First Embodiment)

FIG. **1** is a circuit diagram showing an embodiment of a driving circuit of a liquid crystal device in accordance with the present invention when the liquid crystal device, which is an example of an electro-optical device, is driven in a normally white mode. In FIG. **1**, the driving circuit is adapted to perform 6-bit digital image processing, and it is constituted by a shift register **21**, a latching device **22** composed of a first latching circuit **221** and a second latching circuit **222**, a data conversion circuit **23** provided in the following stage, and a DAC **3** provided in the following stage, and a selective circuit **4**.

A controller **200** provided outside the driving circuit sends out 6-bit image data D_A (D1, D2, . . . , D6) in parallel to the driving circuit. The image data D_A is digital image data indicative of an arbitrary step of gray scale among 2^6 steps of gray scale. The latching device **22** constitutes an example of a digital interface; the first latching circuit **221** captures the bits D1, D2, . . . , D6 at a clock CL from the shift register **21** and sends them out to the second latching circuit **222** at a timing LP. The second latching circuit **222** sends out accumulated data to the data conversion circuit **23**.

In FIG. **1**, there is shown a unit circuit of the driving circuit for supplying a data signal voltage to one of the data signal lines of the liquid crystal device. Actually, as many shift registers **21** as the stages for supplying as many outputs as the data signal lines to the liquid crystal device are required. Likewise, as many latching devices **22** as the data signal lines are required. The same number of pieces of 6-bit image data as the number of horizontal pixels are sent out in parallel from the controller **200**, and the shift register **21** gives outputs in sequence according to the sending-out timing. Upon receipt of each of the outputs of the shift register **21**, the first latching circuit **221** of the driving circuit unit associated with each of the data signal lines latches the 6-bit image data in parallel at the same time. After the image

data for the horizontal pixels has been latched at the first latching circuit **221**, the image data for one line is transferred from the first latching circuit **221** to be simultaneously latched together at the second latching circuit by a latch pulse LP. From the moment the second latching circuit **222** latches the image data for one line, the DAC **3** begins DA conversion. Further, when image data for one line is latched at the second latching circuit **222**, the image data of the horizontal pixels for the next line is sent out in sequence from the controller **200**, and the first latching circuit **221** continues latching in sequence upon receipt of an output from the shift register **21** in the same manner as previously mentioned.

In response to the latch pulse LP, the image data for one horizontal pixel, one pixel being composed of 6-bit image data, is latched at the second latching circuit **222**, and the image data for the one horizontal pixel is sent out at the same time to the data conversion circuit **23** of each driving circuit unit.

In this embodiment, if the value of a most significant bit D6 of the 6-bit image data DA is "0," then the data conversion circuit **23** sends out remaining lower bits D1 through D5 of the image data DA as they are to the DAC 3; if the value of the most significant bit D6 is "1," then it inverts the bits D1 through D5 before sending them out to the DAC **3**. In this specification, the image data (the data composed of the lower bits D1 through D5 or inverted bits thereof) sent out by the data conversion circuit **23** to the DAC **3** will be denoted by D_B, and the inverted bits of the bits D1 through D5 will be accompanied by * and denoted as D1* through D5*.

The DAC **3** is a so-called "SC-DAC" and it is composed of a plurality of transistor switches and capacitors. Five, namely, first through fifth capacitive elements **311** through **315**, are disposed in parallel. A capacitor C0 denoted as a signal line capacitor **310** is parasitically present in an output signal line **39** of the DAC **3**. The output signal line **39** is connected to capacitive elements **311** through **315** via each of bit selective switches **341** through **345** making up a bit selective switching circuit **34**. The DAC **3** further includes a capacitive element resetting device **32** and a signal line potential resetting device **33**. The capacitive element resetting device **32** is composed of five switches **321** through **325**. The respective switches **321** through **325** are provided among terminals of the respective capacitive elements **311** through **315**; they allow the electric charges of the capacitive elements **311** through **315** to be discharged when they are turned ON at the same time. The signal line potential resetting device **33** is constituted by a switch **331** for selectively connecting or disconnecting a connecting terminal b_3 of a selective circuit **42**, which will be discussed later, and the output signal line **39**. When the switch **331** is ON, the potential of the output signal line **39** can be reset by reference voltage V_{b1} or V_{b2} which will be discussed later.

In FIG. **1**, the signal line capacitor **310** provides the parasitic capacitance to the output signal line **39**, the terminal potential (common potential) on the opposite side from the signal line being denoted by V0. The signal line **39** is wired toward a pixel area as the data signal line of the liquid crystal device. The signal line capacitor **310** provides the parasitic capacitance to the output signal line **39** and the data signal line of the pixel area joined thereto as previously mentioned. These signal lines have a capacitor formed between themselves and the electrode of a substrate opposed thereto via liquid crystal. In the pixel area of an active matrix liquid crystal panel, data signal lines and scanning signal lines cross each other or pixel electrodes are adjacently disposed, so that a parasitic capacitor is also formed between the data signal lines, the scanning signal lines, and the pixel electrodes. Alternatively, as it will be discussed later, the wiring width of the output signal line **39** may be increased around the pixel area to adjust the output characteristic curve of the DAC **3** and capacitance may be intentionally formed between the electrodes of the substrates opposed to each other with liquid crystal therebetween. The signal line capacitor C0 represents the total parasitic capacitance. In the drawing, the potential at the other end of the signal line capacitor **310** is shown as the electrode potential (common electrode potential) of the opposed substrate; it is indicated as the potential that contributes most as the potential at the other end of the capacitor when the value of the capacitance generated with the common electrode opposed to the output signal line **39** reaches a maximum value. The potential is not limited to the common electrode potential; as long as it is a potential that enables charging the signal line capacitor C0 in the relationship between the reference voltages V_{b1} and V_{b2}, the capacitor may be formed between itself and other potential, and the potential may be defined as the potential at the other end.

The DAC **3** has first and second reference voltage input terminals "a" and "b." An output terminal (a connecting terminal a3) of the selective circuit **41** is connected to the first reference voltage input terminal "a," and an output terminal (a connecting terminal b3) of a selective circuit **42** is connected to the second reference voltage input terminal "b."

The selective circuits **41** and **42** have two terminals each as the input terminals, namely, a1, a2 and b1, b2, respectively. Voltages V_{a1} and V_{a2} are input to the input terminals a1 and a2 of the selective circuit **41**. A switch **420** of the selective circuit 41 connects the connecting terminal a3 to a1 when the value of the most significant bit D6 (indicated by MSB in FIG. 1) of the input data D_A is "0," while it connects the connecting terminal a3 to the input terminal a2 when the value of the most significant bit D6 is "1."

Further, voltages V_{b1} and V_{b2} are input to the input terminals b1 and b2 of the selective circuit **42**. The switch **430** connects the connecting terminal b3 to the input terminal b1 when the value of the most significant bit D6 of the input data D_A is "0," while it connects the connecting terminal b3 to b2 when the value of the most significant bit D6 is "1."

Thus, in this embodiment, the pair of the first reference voltages are comprised of the voltages V_{a1} and V_{b1}, and the pair of the second reference voltages are comprised of voltages V_{a2} and V_{b2}.

The bit selective switching circuit **34** is comprised of the switches **341** through **345** for selectively connecting or disconnecting the respective capacitive elements **311** through **315** and the output signal line **39**; the switches are turned ON or OFF according to the values of the noninverted signals D1 through D5 or the inverted signals D1* through D5* from the data conversion circuit **23**. The capacitances of the capacitive elements **311** through **315** are set by binary ratios and they are C, 2×C, 4×C, 8×C, and 16×C, respectively; total capacitance C_T of the capacitive elements **311** through **315** connected in parallel is 31×C. According to a general formula, the capacitance of the capacitive elements **311** through **315** is $Cx2^{j-1}$ (where: C denotes a predetermined unit capacitance; j=1, 2, . . . , N−1).

How each of the values of the two pairs of reference voltages V_{a1} and V_{b1} and V_{a2} and V_{b2} are determined in the driving circuit of this embodiment will now be described. In this embodiment, it is assumed that $V_{a1}>V_{b1}$ and $V_{a2}<V_{b2}$.

First, a transmittance variation range T is decided from a transmittance characteristic Y of a liquid crystal pixel that is indicated by an applied voltage V_{LP} to the liquid crystal of a pixel taken on the abscissa and transmittance S_{LP} of the pixel taken on the ordinate as shown in FIG. **2**. Then, two voltages corresponding to the minimum value and the maximum value of the transmittance are determined from the transmittance characteristic curve of the liquid crystal pixel. In this case, the two voltages are denoted as V_{a1} and V_{a2} ($V_{a1}>V_{a2}$).

In this embodiment, the liquid crystal will be driven in the normally white mode; hence, when the transmittance reaches its maximum, the image data D_A will be "000000." At this time, the lower five bits D1 through D5 ("00000") of the image data D_A will be input directly to the data input terminals DT1 through DT5 of the DAC **3** shown in FIG. **1**. Hence, all the bit selective switches **341** through **345** will be OFF. The most significant bit of the image data D_A is "0," so that the switch **430** of the selective circuit **42** connects b3 to b1, and V_{b1} appears at the reference voltage input terminal "b" of the DAC **3**. This causes V_{b1} to appear at the output signal line **39**.

On the other hand, when the transmittance reaches its minimum, the image data D_A is "111111." At this time, the inverted bits D1* through D5* "00000" are input to the data input terminals of the DAC **3**. Hence, the bit selective switches **341** through **345** are all turned OFF in this case also. Further, the most significant bit of the image data D_A is "1," so that the switch **430** of the selector circuit **42** connects b3 to b2 and V_{b2} appears at the reference voltage input terminal "b" of the DAC **3**. Thus, the output of the DAC **3** that corresponds to the maximum value of the transmittance of the transmittance variation range T is V_{b1} and the output of the DAC **3** that corresponds to the minimum value of the transmittance is V_{b2}.

Further, if the image data D_A is "011111," that is, if the value of the image data D_A is set to a decimal value $2^{N-1}-1$, then the lower bits D1 through D5 "11111" are input as they are to the data input terminal of the DAC **3** shown in FIG. **1**. In this case, the most significant bit of the image data D_A is "0," so that the switch **420** of the selective circuit **41** connects the terminal a3 to the terminal a1, and V_{a1} appears at the reference voltage input terminal "a" of the DAC **3**. Also, the switch **430** of the selective circuit **42** connects the terminal b3 to the terminal b1, and V_{b1} appears at the reference voltage input terminal "b" of the DAC **3**. Then, on one hand, the switch **331** of the signal line potential resetting device **33** is turned ON once and then turned OFF to reset the signal line potential of the signal line **39** to V_{b1}. On the other hand, the five switches **321** through **325** of the capacitive element resetting device **32** are all turned ON once and then turned OFF to reset the voltages at both terminals of each capacitive element to V_{a1}. Under this condition, when the bit selective switch **34** is selectively turned ON (in this case, since the bits D1 through D5 are "11111," the bit selective switches **341** through **345** are all turned ON), the following voltage appears at the output signal line **39**:

$$V_1=V_{a1}+\{(V_{b1}-V_{a1})\times 31C/(C0+31C)\} \quad (1)$$

Furthermore, if the image data D_A is "100000," that is, if the value of the image data D_A is set to a decimal value 2^{N-1}, then the inverted bits D1* through D5* "11111" are input to the data input terminal of the DAC **3** shown in FIG. **1**. First, the most significant bit of the image data D_A is "1," so that the switch **420** of the selective circuit **41** connects the terminal a3 to the terminal a2, and V_{a2} appears at the reference voltage input terminal "a" of the DAC **3**. Also, the switch **430** of the selective circuit **42** connects the terminal b3 to the terminal b2, and V_{b2} appears at the reference voltage input terminal "b" of the DAC **3**. Then, on one hand, the switch **331** of the signal line potential resetting device **33** is turned ON once and then turned OFF to reset the signal line potential of the signal line **39** to V_{b2}. On the other hand, the five switches **321** through **325** of the capacitive element resetting device **32** are all turned ON once and then turned OFF to reset the voltages at both terminals of each capacitive element to V_{a2}. Under this condition, when the bit selective switch **34** is selectively turned ON (in this case, since the bits D1* through D5* are "11111," the bit selective switches **341** through **345** are all turned ON), the following voltage appears at the output signal line **39**:

$$V_2=V_{a2}+\{(V_{b2}-V_{a2})\times 31C/(C0+31C)\} \quad (2)$$

Thus, as shown in FIG. **2**, by appropriately selecting the value of $\Delta V=V_2-V_1$, the difference between the transmittance of the liquid crystal pixel obtained by the voltage (the output voltage of the DAC **3**) appearing at the output signal line **39** when the image data D_A is "011111" and the transmittance of the liquid crystal pixel obtained by the voltage appearing at the output signal line **39** when the image data D_A is "100000" can be set to one step of gray scale of the transmittance variation range T (one step of gray scale on the logarithm axis).

The condition for the gray scale not to be reversed over the range of "011111" to "100000" is $\Delta V>0$, that is;

$$(31C/C_T)\times(V_{a1}-V_{a2})<V_{b2}-V_{b1}$$

In general, the following formula applies:

$$\Sigma Ci/C_T\times(V_{a1}-V_{a2})<V_{b2}-V_{b1}$$

(where the computation of Σ is carried out on i=1 to i=N−1)

The above inequality formula holds if a voltage of the positive polarity is output from the driving circuit to the output signal line **39** when driving the liquid crystal of the pixels by AC. For this reason, it should be noted that all signs of inequality in the above inequality formula are reversed when a voltage of the negative polarity is output.

As it is obvious from the formulas (1) and (2) given above, if $V_{b1}-V_{b2}$ and $V_{a2}-V_{a1}$ remain constant, then the value of ΔV does not change. Hence, if, for example, V_{b1} and V_{b2} are set to fixed values, $V_{a2}-V_{a1}$ is set to a constant value, and the values of V_{a2} and V_{a1} are shifted in the positive or negative direction, then the center of the gray scale of the output characteristic curve of the DAC **3** with respect to the image data D_A can be moved toward higher or lower transmittance.

FIG. **3**(A) shows the output characteristic (image data value D_A-Output voltage Vc of DAC) of the DAC **3** in a case (G1) where the voltage difference of $V_{a2}-V_{a1}$ is increased and a case (G2) where it is decreased while the voltage difference of $V_{b1}-V_{b2}$ is held constant, and the output characteristic before the change being denoted by **G0**.

As it is seen from formula (2) above, by appropriately setting the total capacitance C_T of the capacitive elements **311** through **315** and the capacitance C0 of the signal line capacitor **310**, the change in the gradient of the output characteristic curve of the DAC **3** with respect to the image data D_A can be changed. More specifically, increasing C_T with respect to C0 permits the change in the gradient of the output characteristic curve to increase, and decreasing C_T with respect to C0 permits the output characteristic curve to be close to a straight line.

FIG. **3**(B) shows the output characteristic (image data value D_A-Output voltage Vc of DAC) of the DAC **3** in a

case (G3) where C_T is increased with respect to C0 and a case (G4) where it is decreased while V_{a1}, V_{a2}, V_{b1}, and V_{b2} are held constant, and the output characteristic before the change being denoted by G0.

To bring the output characteristic curve further close to a straight line, a capacitor of a predetermined capacitance may be connected in parallel to the signal line **39** to increase the capacitance C0 of the signal line capacitor **310**. More specifically, by this configuration, the change in the driving voltage with respect to the change in the gray scale in the DAC **3** can be brought close to a straight line due to the increased capacitance of the signal line **39** as mentioned above; therefore, even when the γ characteristic is more linear, it can be handled by using the output characteristic curve of the DAC **3**.

The operation of the DAC **3** when the two pairs of reference voltages V_{a1}, V_{b1} and V_{a2}, V_{b2} have been set and the total capacitance C_T of the capacitive elements **311** through **315** has been set as set forth above will now be described in detail.

First, the most significant bit D6 of the image data D_A input to the data conversion circuit **23** is input to a data input terminal DT6 of the DAC 3. If the value of the most significant bit D6 is "0," then the switch **420** of the selective circuit **41** connects the connecting terminal a3 to the terminal a1 and the switch **430** of the selective circuit **42** connects the connecting terminal b3 to the terminal b1. If the value of the most significant bit D6 is "1," then the switch **420** of the selective circuit **41** connects the connecting terminal a3 to the terminal a2 and the switch **430** of the selective circuit **42** connects the connecting terminal b3 to the terminal b2. At this time, the switches **321** through **325** of the capacitive element resetting device **32** and the switch **331** of the signal line potential resetting device **33** are both ON, while the switches **341** through **345** of the bit selective switching circuit **34** are OFF. This causes the capacitive elements **311** through **315** to discharge and both terminals of each thereof to be reset to the reset voltage V_{a1} or V_{a2} and the terminal of the signal line capacitor **310** (i.e. the output signal line **39**) to be reset to V_{b1} or V_{b2}.

Under this condition, the switches **321** through **325** and the switch **331** are turned OFF, then the switches **341** through **345** of the bit selective switching circuit **34** that had been OFF until then are selectively turned ON according to the values of the first bit D1 to the fifth bit D5 of the image data D_A. At this time, as previously mentioned, if the value of the most significant bit D6 of the image data D_A input to the data conversion circuit **23** is "0," then the noninverted signals D1 through D5 of the lower five bits are input to the data input terminals DT1 through DT5 of the DAC **3**, or if the value of the most significant bit D6 is "1," then the inverted signals D1* through D5* of the lower five bits are input thereto.

Therefore, if, for example, the image data D_A is "000001," then 0, 0, 0, 0, 1 are respectively input to the five terminals DT1 through DT5 of the DAC **3**, causing only the switch **341** among the switches of the bit selective switching circuit **34** to be turned ON. Likewise, if the image data D_A is "111110," then 0, 0, 0, 0, 1 are respectively input to the five terminals DT1 through DT5 of the DAC 3, causing only the switch **341** among the switches of the bit selective switching circuit **34** to be turned ON also in this case.

Thus, a capacitive element of **311** to **315** connected to a switch that is ON among the switches **321** through **325** is connected to the signal line capacitor **310**, and the voltage based on this connection appears at the output signal line **39**.

For instance, if the image data D_A is "000001," then the signal line capacitor **310** (capacitance C0) is charged by the voltages V_{b1} and V0 at both terminals. The capacitive element **311** (capacitance C) connected to the signal line **39** via the switch **341** after all the switches **321** through **325** of the capacitive element resetting device **32** are turned OFF is charged by the reference voltages V_{a1} and V_{b1} (on the other hand, the capacitive elements **312** through **315** are not charged by the reference voltages V_{a1} and V_{b1} because the switches **342** through **345** remain OFF). Hence, the capacitive element **311** (capacitance C) and the signal line capacitor **310** (capacitance C0) cause a voltage, which looks as if it were obtained by substantially dividing the pair of reference voltages V_{a1} and V_{b1} (i.e. $V_{b1}-V_{a1}$), to appear at the output signal line **39**.

Further, if the image data D_A is "111110," then the signal line capacitor **310** (capacitance C0) is charged by the voltages V_{b2} and V0 at both terminals. The capacitive element **311** (capacitance C) connected to the signal line **39** via the switch **341** after all the switches **321** through **325** of the capacitive element resetting device **32** are turned OFF is charged by the reference voltages V_{a2} and V_{b2} (on the other hand, the capacitive elements **312** through **315** are not charged by the reference voltages V_{a2} and V_{b2} because the switches **342** through **345** remain OFF). Hence, the capacitive element **311** (capacitance C) and the signal line capacitor **310** (capacitance C0) cause a voltage, which looks as if it were obtained by substantially dividing the pair of reference voltages V_{a2} and V_{b2} (i.e. voltages $V_{b2}-V_{a2}$), to appear at the output signal line **39**.

In FIG. **4**, graph (A) on the left shows the output voltage Vc of the DAC **3** with respect to the image data D_A (expressed in 64 steps of gray scale), and graph (B) on the right shows the relationship between a transmittance S_{LP} (axis: logarithm) of a liquid crystal pixel and a voltage V_{LP} (corresponding to the output voltage Vc of the DAC 3) applied to a liquid crystal pixel electrode, the transmittance S_{LP} being indicated on the abscissa and the applied voltage V_{LP} being indicated on the ordinate. "111111" to "000000" of the image data D_A are binary codes of the image data indicative of 64 steps of gray scale. As it becomes apparent by referring to graphs (A) and (B) in FIG. **4** in contrast to graphs (A) and (B) in FIG. **21**, the DAC **3** in accordance with the present invention makes a γ correction while carrying out D/A conversion at the same time.

Shifting all the reference voltages V_{a1}, V_{a2}, V_{b1}, and V_{b2} to the high voltage side or the low voltage side makes it possible to shift the overall luminance (transmittance) in the pixels to the low side or the high side. Furthermore, by setting the voltage difference $V_{b1}-V_{b2}$ to a large value beforehand, the contrast ratio can be increased, or by setting it to a small value, the contrast ratio can be decreased.

FIG. **5** gives a graph indicative of the relationship between the transmittance of liquid crystal pixels and the voltage applied to the liquid crystal pixel electrodes in three cases (indicated by cases I through III) where actual measurement has been performed in this embodiment. In FIG. **5**, the voltages of the positive and negative polarities of V_{a1}, V_{a2}, V_{b1}, and V_{b2} are respectively applied in the respective cases I through III. This is because there are cases where a voltage of the positive polarity is output and cases where a voltage of the negative polarity is output with respect to the reference voltage (**0V** in the case of FIG. **5**) to the data signal line to drive the liquid crystal of the pixels in the AC mode. If V_{a1}, V_{a2}, V_{b1}, and V_{b2} are positive voltages, then the voltage of the positive polarity is applied to the pixel liquid crystal, or if they are negative voltages, then the voltage of the negative polarity is applied thereto.

Accordingly, in the driving circuit of FIG. **1**, in actual use, as V_{a1}, V_{a2}, V_{b1}, and V_{b2}, respectively, the reference voltage

for applying the voltage of the positive polarity and the reference voltage for applying the voltage of the negative polarity are switched at a regular cycle and applied.

Regarding the switching cycle of the voltages V_{a1}, V_{a2}, V_{b1}, and V_{b2}, if the driving method of the liquid crystal device is such that the polarity of the voltage applied to the liquid crystal is inverted at every vertical scanning period (1 field or 1 frame), then the switching of the voltages is performed at every vertical scanning period; if the polarity is inverted at every horizontal scanning period (so-called "line inverting drive"), then the switching of the voltages is performed at every horizontal scanning period. Further, if the polarity is inverted at every column line (so-called "source line inversion") or if the polarity is inverted at every pixel (so-called "dot inverting drive"), then the polarities of the voltages applied as V_{a1}, V_{a2}, V_{b1}, and V_{b2} with respect to the reference voltages are different alternately for every adjacent unit driving circuit. More specifically, the reference voltage applied as V_{a1} is for the positive polarity in the unit driving circuit of a first data signal line, while the reference voltage applied as V_{a1} is for the negative polarity in the unit driving circuit of a second data signal line; thus the voltages are different. The reference voltage for each unit driving circuit is switched for every vertical scanning period in the case of the source line inversion, or for every horizontal scanning period in the case of the dot inversion.

In the first embodiment set forth above and other embodiments to be described below, the description is given, the relationship between the image data D1 through D6 and the terminals DT1 through DT6 may be reversed so that "111111" denotes white and "000000" denotes black. Further, in this embodiment, the same apparently applies to even the orientation of liquid crystal molecules and the setting of the axis of polarization are changed (to the normally black mode) so that the transmittance is high when the output voltage of the DAC is low, while the transmittance is low when the output voltage thereof is high.

More detailed configuration and operation of the driving circuit of the first embodiment will now be described with reference to FIG. **6** and FIG. **7**. FIG. **6** is a detailed circuit diagram of the driving circuit of the embodiment, and FIG. **7** is a timing chart thereof. In FIG. **7**, like constituent parts as those shown in FIG. **1** are assigned like reference numerals and the description thereof will be omitted as necessary.

In FIG. **6**, six latching elements **211** through **216** of a first latching circuit **221** are respectively driven by the output pulses of a shift register **7**; they are adapted to latch 6-bit image data for one pixel on a data line at the same time. Only one unit of driving circuit is shown for the first latching circuit **221**; however, a similar first latching circuit is configured also for the unit driving circuit adjoining the latching circuit. In the first latching circuit **221**, however, the latching is controlled by a different output of the shift register **7** for each unit driving circuit.

A second latching circuit **222** is configured so that it captures all bits D1, D2, . . . , D6 retained at the first latching circuit **221** into each of latching elements **271** through **276** by a latch pulse LP0 and outputs them to the data conversion circuit **23**. Like the first latching circuit **221**, the second latching circuit **222** is provided at each unit driving circuit; however, the second latching circuit **222** of each unit driving circuit is different from the first latching circuit **221** in that it latches at the same time by the same latch pulse LP0.

The data conversion circuit **23** is made up of five sets of gate circuits **311** through **315**, each of which is composed of an EX-OR gate, a NAND gate, and a NOT gate, and a latching gate **316**.

Each of the EX-OR gate of the gate circuits **311** through **315** inputs the respective bit values D1 through D5 of the image data D_A from the latching elements **271** through **276**, and the latching gate **316** inputs the value of the most significant bit D6. Each EX-OR gate is configured so that, if the value of the most significant bit D6 is "1," then it inverts the values of the lower bits D1 through D5 before it outputs them to the NAND gate in the following stage, or if the value of the most significant bit D6 is "0," then it outputs the values of the lower bits D1 through D5 to the NAND gate in the following stage without inverting them.

Level shifting circuits **81** through **86** are the circuits for shifting, for example, a binary voltage level from 0 V and 5 V to 0 V and 12 V; each of them has two output terminals for a noninverted output and an inverted output. The outputs of these two output terminals are sent out to the DAC **3** in the following stage. In FIG. **6**, the noninverted output signals of the level shifting circuits **81** through **86** are denoted by LS1 through LS6.

In this embodiment, the respective capacitive elements **311** through **315** are constituted by patterns. Regarding each of the capacitive elements **312** through **315**, the capacitive element **312** is constituted by connecting in parallel two capacitors of the same capacitance as that of the capacitance C of the capacitive element **311**, the capacitive element **313** is constituted by connecting in parallel four capacitors of the same capacitance as that of the capacitance C of the capacitive element **311**, the capacitive element **314** is constituted by connecting in parallel eight capacitors of the same capacitance as that of the capacitance C of the capacitive element **311**, and the capacitive element **315** is constituted by connecting in parallel sixteen capacitors of the same capacitance as that of the capacitance C of the capacitive element **311**. The reference voltages of the voltages V_{a1}, V_{a2}, V_{b1}, and V_{b2} are of AC (the voltage polarity is inverted, for example, for every scanning line, field, or frame); hence, each of the switches **341** through **345** is composed of a CMOS transistor having two control terminals to enable operation regardless of whether the polarity of a signal to be controlled is positive or negative. More specifically, the noninverted output signals LS1 through LS5 from the level shifting circuits **81** through **86** are adapted to actuate each of the switches **341** through **345** when the capacitive element resetting voltages V_{a1}, V_{a2} and the signal line potential resetting voltages V_{b1}, V_{b2} are positive, while the inverted output signals from the level shifting circuits **81** through **86** are adapted to actuate each of the switches **341** through **345** when the capacitive element resetting voltages V_{a1}, V_{a2} and the signal line potential resetting voltages V_{b1}, V_{b2} are negative.

The operating of the driving circuit configured as illustrated in FIG. **6** will now be described with reference to the timing chart given in FIG. **7**.

In FIG. **7**, first, during a previous horizontal scanning period, the first latching circuit **221** sequentially latches the image data for the number of the horizontal pixels for each unit driving circuit according to a transfer signal issued in sequence from the shift register **7**. Then, when the image data for one horizontal pixel has been latched and when the latch pulse LP0 is generated at time t1 in a horizontal blanking period, the second latching circuit **222** captures each of the bits D1, D2, . . . , D6 held at the first latching circuit **221** into each of the latching elements **271** through **276** and outputs them to the data conversion circuit **23**.

Next, when a reset signal RS1 is input to the respective NAND gates of the data conversion circuit **23**, the outputs of the EX-OR gates are output to the level shifting circuits

81 through 85 via the NOT gates during a period from t_3 to t_4 (i.e. the horizontal scanning period) during which the reset signal RS1 stays at the H level. When the latch pulse LP0 is input, the most significant bit D6 is output to the level shifting circuit 86 from the latching gate 316.

In this embodiment, the value of the most significant bit D6 is "1" and therefore, a noninverted output LS6 of the most significant bit D6 from the level shifting circuit 86 is switched to the high level at time t1 which is the timing at which the latch pulse LP0 is generated. And the actuation of the switch 420 causes the resetting voltage V_{a2} to appear at a selected terminal a_3 at time t1. Also, the actuation of the switch 430 causes a signal line potential resetting voltage V_{b2} to appear at a selected terminal b_3 at time t1.

Then, when a reset signal RS2 or its inverted signal (this inverted signal is denoted by RS2* in FIG. 6) is generated at time t2, the switches 321 through 325 of the capacitive element resetting device and the switch 331 of the signal line potential resetting device are turned ON. At this time, the period during which the reset signal RS2 is at the high level is later than the timing at which the latch pulse LP0 is generated but earlier than time t3 at which the reset signal RS1 rises.

Subsequently, when a reset signal RS3 is generated at time t3 under a condition where the switch 331 of the signal line resetting device is OFF, the potential of the signal line is V_{b2}, the switches 321 through 325 of the capacitive element resetting device are OFF, and the capacitive elements 311 through 315 are chargeable, the switches 341 through 345 of the bit selective switching circuit are selectively turned ON in accordance with the values of the outputs of the level shifting circuits 81 through 85. In this embodiment, only LS1 among the outputs LS1 through LS5 of the level shifting circuits 81 through 85 is switched to the H level; therefore, the voltage (the output voltage Vc of the DAC 3), which is generated by the connection between the capacitive element 311 and the signal line capacitor 310, will appear at the output signal line 39, and the output voltage Vc is applied to the signal line in the horizontal scanning period.

As described in detailed above, according to the first embodiment, the output voltage in accordance with the step of gray scale indicated by the bits of the digital image data D_A can be supplied to the respective signal lines of the liquid crystal device and the γ correction can be made at the same time.

(Second Embodiment)

A second embodiment of the driving circuit of a liquid crystal device in accordance with the present invention will now be described with reference to FIG. 8.

FIG. 8 shows the second embodiment that employs a resistance ladder type DAC in place of the SC-DAC shown in FIG. 1. In FIG. 8, a driving circuit 12 is comprised of a shift register 21, a latching device 22 composed of a first latching circuit 221 and a second latching circuit 222, a data conversion circuit 23, and a DAC 5. The configurations and functions of the shift register 21, the latching device 22, and the data conversion circuit 23 are the same as those of the first embodiment. In FIG. 8, the same constituent elements as those shown in FIG. 1 are given the same reference numerals and the description thereof will be omitted as necessary. In the second embodiment also, the detailed configuration (the shift register, the latching means, and the data conversion circuit) up to the stage preceding the DAC is identical to that of the first embodiment shown in FIG. 6.

As in the case of the driving circuit shown in FIG. 1, when a controller 200 sends out 6-bit image data D_A to the driving circuit 12, the latching device 22 sends out the six bits D1 through D6 of the image data D_A to the data conversion circuit 23. The data conversion circuit 23 sends out the most significant bit D6 and the lower bits D1 through D5 without inverting them to the input terminal of the DAC 5 if the value of the most significant bit D6 is "0." If the value of the most significant bit D6 is "1," then the data conversion circuit 23 inverts the values of the lower bits D1 through D5 and sends the inverted bits as well as the most significant bit D6 to the input terminal of the DAC 5.

The DAC 5 is comprised of a decoder 51, 25 resistors r_1 through r_n ($n=2^5$) connected in series, and an "n" number of switches SW_1, through SW_n ($n=2^5$). In this case, the value of each "r" of the resistors r_1 through r_n is set so that the voltage Vc output according to the value of the combined resistance of the resistors connected in series that are selected among the resistors r_1 through r_n by the image data D_A changes as shown in FIG. 4(A) except for the last resistor r_n that is set to $r_n \approx r_{n-1}/2$. Setting to $r_n \approx r_{n-1}/2$ makes it possible to set the difference between the transmittance of the liquid crystal pixel obtained by the output voltage Vc of the DAC 5 when D_A is "011111" and the transmittance obtained by the output voltage Vc of the DAC 5 when D_A is "100000" to approximately one step of gray scale (one step of gray scale in logarithm) of a transmittance variation range T of the liquid crystal pixel.

First and second reference input terminals "d" and "e" are connected to both ends of the series connection circuit of the resistors r_1 through r_n. One end of the switch SW_1 is connected to a reference voltage input terminal "d" of the DAC 5 (the end on the side of r_1 of the series connection circuit of the resistors r_1 through r_n), and one end of each of the switches SW_2 through SW_n is connected to the connection (tap) of r_1 through r_n of the series connection circuit, while the other end of each of the switches SW_1 through SW_n is connected to the output terminal Vc of the DAC 5.

A selective circuit 61 is connected to the reference voltage input terminal "d" of the DAC 5. The selective circuit 61 has two input terminals d_1 and d_2 and one connection terminal d_3, voltages Vd_1 and Vd_2 being input to these terminals. A reference voltage input terminal "e" is fixed at a midpoint potential Ve. In this embodiment, Vd_1 and Ve make up a pair of first reference voltages, and Vd_2 and Ve make up a pair of second reference voltages. There is an established relationship $Vd_1 > Ve > Vd_2$ between the voltages Vd_1, Vd_2, and Ve.

The selective circuit 61 connects a connection terminal d_3 to an input terminal d_2 when the value of the most significant bit D6 of input data D_A is "0" or it connects the connection terminal d_3 to an input terminal d_1 when the value of the most significant bit D6 is "1."

In the driving circuit 12 of FIG. 8, if, for example, the image data D_A is "000001," then the most significant bit D6 is "0"; therefore, the data conversion circuit 23 outputs the lower bits D1 through D5 to the decoder 51 without inverting them. The selective circuit 61 connects the connection terminal d_3 to the input terminal d_2. Further, 0, 0, 0, 0, 1 are input to five terminals DT1 through DT5 of the decoder 51 (the decode value at this time is "1"), and only the switch SW_2 corresponding to a decode value "1" among the switches SW_1 through SW_n will be turned ON. Accordingly, the voltage Vc as shown below will appear at the output terminal C of the DAC 5:

$$Vc = Vd_2 + (Ve - Vd_2) \times [r_1/(r_1 + r_2 + \ldots + r_n)]$$

If, for example, image data D_A is "111110," then the most significant bit D6 is "1"; therefore, the data conversion circuit 23 inverts the lower bits D1 through D5 before it

outputs them to the decoder **51**. The selective circuit **61** connects the connection terminal d_3 to the input terminal d_1. Further, 0, 0, 0, 0, 1 are input to each of the five terminals DT1 through DT5 of the decoder **51** (the decode value at this time is "1"), and only the switch SW_1 corresponding to the decode value "1" among the switches SW_1 through SW_n will be turned ON. Accordingly, the voltage Vc as shown below will appear at the output terminal C of the DAC 5:

$$Vc=Vd_1-(Vd_1-Ve)\times[r_1/(r_1+r_2+\ldots+r_n)]$$

As in the case of the first embodiment, as the voltages Vd_1, Vd_2, and Ve, the reference voltage used when a voltage of the positive polarity is applied to the pixels and the reference voltage used when a voltage of the negative polarity is applied to the pixels are periodically switched to carry out the scanning line reversing drive or the like and are supplied to each of them. The switching timing is the same as that explained in the case of the first embodiment.

The configuration of the DAC used for the present invention is not limited to the one in the first or second embodiment shown in FIG. **1** or FIG. **8** as long as the changes occur from a large gradient to a small gradient in the small area/large area of input data value, whereas the changes occur from small gradient to a large gradient in the large area/small area of the input data value. Various types of the DAC may be employed.

In the embodiments set forth above, the description has been given to the cases where the 6-bit digital image data is processed. The present invention, however, is not limited thereto; it is obvious that the invention may be applied to perform the processing of a variety of digital image data of 4 bits, 5 bits, 7 bits, or more.

Likewise, in the above embodiments, the values of the first through fifth bits have been inverted when the value of the most significant bit of the image data D_A was "1"; alternatively, however, the configuration may be such that the values of the first through fifth bits are inverted (they are output as they are when the value of the most significant bit is "1")when the value of the most significant bit of the image data D_A is "0".

Further in this embodiment, the normally white mode has been used; however, the same can be embodied even if the normally black mode is used.

(Third Embodiment)

An embodiment of a liquid crystal device which is an example of the electro-optical device in accordance with the present invention will be described with reference to FIG. **9** through FIG. **17**.

The driving circuits in each of the embodiments set forth above are employed to drive a liquid crystal device **701** shown, for example, in a top plan view (A), a cross-sectional view (B), and a longitudinal sectional view (C) of FIG. **9**.

In FIG. **9**, liquid crystal **705** is charged between an active matrix substrate **702** and an opposed substrate (a color filter substrate) **703**; it is sealed by a sealant **704** on the peripheries of each of the substrates. A light-shielding pattern **706** is formed along the periphery of the active matrix substrate **702** excluding the peripheral edge portion. Formed inside the light-shielding pattern **706** is an active matrix section **707** composed of pixel electrodes, output signal lines (data lines), scanning lines or the like. Provided in the foregoing peripheral edge portion are a driver **708** in which as many driving circuits in each of the above embodiments as pixel array columns are formed, and a scanning line driver **709**. Further, a mount terminal member **710** is provided on the outer side of the scanning driver **709** in the peripheral edge portion.

The circuit diagram of the above active matrix type liquid crystal device is shown in FIG. **10**.

In FIG. **10**, pixels are formed in a matrix pattern in the active matrix section **707**. In the active matrix section **707**, a data signal line **902** is driven by the signal line driver **708** in which the unit driving circuits described in the first or second embodiment are disposed to match data signal lines, and the scanning line **903** is driven by the scanning line driver **709**. Each pixel is comprised of: a thin film transistor (TFT) **904** having its gate connected to the scanning line **903**, its source connected to the data signal line **902**, and its drain connected to a pixel electrode (not shown); liquid crystal **905** disposed between the pixel electrode and a common electrode (not shown); and a charge accumulating capacitor **906** formed between the pixel electrode and its adjacent scanning line. The scanning line driver **709** is constituted by a shift register **900** that sequentially provides outputs during every horizontal scanning period to decide the timing for selecting a scanning line, and a level shifter **901** that receives the outputs of the shift register **900** and outputs a scanning signal of the voltage level that turns the TFT **904** ON to the scanning line **903**.

The signal line driver **708** is provided with a shift register **21**, a first latching circuit **221**, a second latching circuit, a data conversion circuit **23**, a DAC **3** or the like as previously mentioned.

A process (process employing a low temperature polysilicon technique) for forming the driving circuits (the driver **708**), the active matrix section **707** or the like on the aforesaid active matrix substrate **702** will now be described step by step with reference to FIGS. **11** through **15**.

Step 1: First, as shown in FIG. **11**, a buffer layer **801** is formed on an active matrix substrate **800**, and an amorphous silicon layer **802** is formed over the buffer layer **801**.

Step 2: Then, the whole surface of the amorphous silicon layer **802** of FIG. **11** is subjected to laser annealing to make the amorphous silicon layer polycrystalline so as to form a polycrystalline silicon layer **803** as shown in FIG. **12**.

Step 3: Next, the polycrystalline silicon layer **803** is patterned to form island regions **804**, **805**, and **806** as shown in FIG. **13**. The island regions **804** and **805** are the layers where the active regions (sources and drains) of MOS transistors employed as each of the switches shown in the embodiments are formed. The island region **806** is the layer that provides one pole of the thin film capacitor of the capacitive element shown in the embodiments.

Step 4: Next, as shown in FIG. **14**, a mask layer **807** is formed, and phosphorous (P) ions are implanted only in the island region **806** that provides one pole of the thin film capacitor of the capacitive element so that the island region **806** has lower resistance.

Step 5: Next, as shown in FIG. **15**, a gate insulating film **808** is formed, and TaN layers **810**, **811**, and **812** are formed on the gate insulating film **808**. The TaN layers **810** and **811** are the layers that provide the gates of the MOS transistors employed as various switches, while the TaN layer **812** is the layer that provides the other pole of the thin film capacitor. After producing these TaN layers, a mask layer **813** is formed, and phosphorous (P) ions are implanted in self-alignment by using the gate TaN layer **810** as the mask to form an n-type source layer **815** and drain layer **816**.

Step 6: Next, as shown in FIG. **16**, mask layers **821** and **822** are formed, boron (B) ions are implanted in self-alignment by using the gate TaN layer **811** as the mask to form a p-type source layer **821** and drain layer **822**.

Step 7: Next, as shown in FIG. **17**, an interlayer insulating film **825** is formed and contact holes are formed in the

interlayer insulating film, then electrode layers **826**, **827**, **828**, and **829** composed of ITO or Al are formed. Electrodes are connected also to the TaN layers **810**, **811** and **812**, and the polycrystalline silicon layer **806** via the contact holes although they are not shown in FIG. **17**. Thus, an n-channel TFT and a p-channel TFT employed as each of the switches of the driving circuit, and a MOS capacitor used as the capacitive element also of the driving circuit are produced.

Using the steps **1** through **7** set forth above permits easier manufacture of the liquid crystal device including the driver circuitry and also enables reduced cost to be achieved. The polysilicon provides significantly higher mobility of carriers than amorphous silicon, so that it permits high-speed operation, which is advantageous in achieving higher performance of the circuit.

A process employing amorphous silicon may be used in place of the manufacturing process set forth above.

The driving circuits of the liquid crystal devices of the embodiments described above may be constituted by thin film transistors, resistive elements and capacitive elements formed by silicon thin film layers or metal layers on a glass substrate made of quartz glass, non-alkali glass or the like, or they may be formed on other substrates (e.g. synthetic resin substrates and semiconductor substrates) other than the glass substrates. In the case of a semiconductor substrate, metallic reflector electrodes are used for pixel electrodes, the transistor elements, resistive elements, and capacitive elements are formed on the surface of the semiconductor substrate or the surface of the substrate, and a glass substrate is used for the opposed substrate, thereby to accomplish a reflective type liquid crystal device having liquid crystal held between the semiconductor substrate and the glass substrate. When forming the driving circuits on the glass substrate having a lower melting point, it is preferable to use the manufacturing process employing the low temperature polysilicon technique (TFT process) to improve reliability.

The liquid crystal devices in the embodiments described above are of the active matrix type; however, there are no restrictions on the type of the liquid crystal device, and other types than the active matrix type can be used. Further, various types of DAC may be used; when forming the circuits on the glass substrate, however, it is preferable to employ the SC type DAC or the resistance ladder type DAC to achieve reduced variations in the operating characteristics and improved reliability. In the embodiments set forth above, the present invention has been applied to the liquid crystal device as an example of the electro-optical device; however, the same or similar advantages can be expected by applying the present invention as long as the electro-optical device exhibits nonlinear optical characteristic with respect to driving voltage.

In particular, when forming the driving circuits in each of the embodiments on silicon substrates, it is preferable to use the resistance ladder type DAC which makes it easy to produce high resistance in a relatively small area and to minimize variations. Likewise, when using the silicon semiconductor substrate, it is preferable to configure a reflective type liquid crystal panel. Conversely, when forming the driving circuits on the glass substrate, the use of the SC-DAC makes it possible to configure the device by using elements of relatively small areas, so that the area of the whole circuitry can be made smaller, providing advantages.

In particular, even when the driving circuits are formed on the glass substrate by the manufacturing process employing the low temperature polysilicon technique, the SC-DAC or the resistance ladder type DAC can be used as the DAC, enabling smaller driving circuits to be accomplished without complicating the circuit configuration.

Diverse embodiments of the liquid crystal device driven by the aforesaid driving circuits manufactured using the active matrix substrate described above and electronic equipment such as a portable computer and a liquid crystal projector having the liquid crystal device will now be described.

(Fifth Embodiment)

As illustrated in FIG. **18**, a liquid crystal device **850** is constructed by a backlight **851**, a polarizer **852**, a TFT substrate **853**, liquid crystal **854**, an opposed substrate (a color filter substrate) **855**, and a polarizer **856** that are assembled in the order in which they are listed. In this embodiment, a driving circuit **857** is formed on the TFT substrate **853** as described above.

(Sixth Embodiment)

As shown in FIG. **19**, a portable computer **860** has a main unit **862** provided with a keyboard **861**, and a liquid crystal display screen **863**.

(Seventh Embodiment)

As shown in FIG. **20**, a liquid crystal projector **870** is a projector employing a transmissive type liquid crystal panel as a light valve; it uses, for example, a 3-panel prism type optical system. In the projector **870** shown in FIG. **20**, the projection light emitted from a lamp unit **871**, which is a white light source, is separated into three primary colors, namely, R, G, and B, through a plurality of mirrors **873** and two dichroic mirrors **874** in a light guide **872** and the three color light beams are guided to three liquid crystal panels **875**, **876**, and **877** that display the images of the respective colors. The light beams that have been modulated by the respective liquid crystal panels **875**, **876**, and **877** are incident upon a dichroic prism **878** from three directions. The light beams of R (red) and B (blue) are bent by 90 degrees through the dichroic prism **878**, whereas the light beam of G (green) goes straight therethrough, so that the images of the respective colors are synthesized thereby to project a color image on a screen or the like through a projection lens **879**.

Electronic equipment to which the present invention can be applied includes an engineering workstation, a pager or a portable telephone, a word processor, a TV set, a viewfinder type or monitor viewing type video camera, an electronic pocketbook, an electronic desktop calculator, a car navigation device, a POS terminal, and a variety of devices provided with touch panels.

As described above, according to each of the embodiments, it is possible to achieve a reliable driving circuit of a liquid crystal device that is compatible to digital image signals, provides stable operating characteristics with controlled variations, and provides the DA converting function and the γ correcting function (or an auxiliary function for the γ correction) by a relatively simple and a small-scale circuit configuration, and a liquid crystal device and a variety of electronic equipment employing the driving circuit.

INDUSTRIAL APPLICABILITY

The driving circuit of an electro-optical device in accordance with the present invention can be used as the driving circuit for driving a transmissive or reflective type liquid crystal device, and further, it can be used as the driving circuit for driving diverse electro-optical devices that exhibit nonlinear changes in optical characteristics with respect to the changes in driving voltage while correcting the nonlinearity at the same time. Moreover, the driving circuit of the electro-optical device in accordance with the present invention can be used for a variety of electro-optical devices

constructed using such a driving circuit and also for electronic equipment or the like constituted using such electro-optical devices.

What is claimed is:

1. A driving circuit of an electro-optical device that supplies an analog image signal, which has a driving voltage corresponding to an arbitrary gray scale level among 2^N (where N is a natural number) steps of gray scale, to a signal line of an electro-optical device in which changes in an optical characteristic thereof with respect to changes in said driving voltage are nonlinear; said driving circuit of an electro-optical device comprising:

an input interface to which an N-bit digital image signal indicative of said arbitrary gray scale level is applied; and

a digital-to-analog converter that generates a driving voltage within a first driving voltage range defined by a first pair of reference voltages or within a second driving voltage range defined by a second pair of reference voltages according to a bit value of said digital image signal and corresponding to the gray scale level of said digital image signal so that changes in said driving voltage with respect to changes in the gray scale level of said digital image signal are nonlinear; the digital-to-analog converter generates a voltage within the range of the first pair of reference voltages if said applied digital image signal indicates a gray scale level from a first to m−1th value (where "m" is a natural number and $1 < m \leqq 2^N$), and generates a voltage within the range of the second pair of reference voltages adjacent to said first driving voltage range if said digital image signal indicates a gray scale level from an m-th to 2^N-th value, and supplies said analog image signal including said generated driving voltage to said signal line.

2. The driving circuit of an electro-optical device according to claim 1, wherein a first reference voltage of said first pair of reference voltages is greater than the second reference voltage of said first pair of reference voltages; and

a first reference voltage of said second pair of reference voltages is less than the second reference voltage of said second pair of reference voltages, a change in said driving voltage corresponding to a change in the gray scale having an inflection point within ranges defined by said first pair of reference voltages and said second pair of voltages respectively.

3. The driving circuit of an electro-optical device according to claim 1, wherein:

the value of said "m" is equal to 2^{N-1};

lower N−1 bits of said digital image signal are selectively applied to said digital-to-analog converter either inverted or non-inverted according to a value of a most significant bit of said digital image signal; and

said digital-to-analog converter generates a voltage in the range of said first reference voltages if said lower N−1 bits are applied non-inverted, and generates a voltage in the range of said second reference voltages if said lower N−1 bits are inverted before being applied thereto.

4. The driving circuit of an electro-optical device according to claim 3, further comprising a selective inverting circuit for selectively inverting said lower N−1 bits depending upon the value of said most significant bit, said selective inverting circuit being provided between said interface and said digital-to-analog converter.

5. The driving circuit of an electro-optical device according to claim 1, further comprising a selective voltage supply circuit for selectively supplying either said first or second reference voltages to said digital-to-analog converter according to a value of a most significant bit of said digital image signal.

6. The driving circuit of an electro-optical device according to claim 1, wherein said digital-to-analog converter comprises a switched capacitor type digital-to-analog converter that generates driving voltages in the ranges of said first and second reference voltages, respectively, by means of charging a plurality of capacitors.

7. The driving circuit of an electro-optical device according to claim 6, wherein said first reference voltages include a pair of voltages that enable a voltage in said first driving voltage range to be selectively generated, and said second reference voltages include a pair of voltages that enable a voltage in said second driving voltage range to be selectively generated.

8. The driving circuit of an electro-optical device according to claim 7, wherein:

the value of said "m" is equal to 2^{N-1};

the lower N−1 bits of said digital image signal are selectively applied to said switched capacitor type digital-to-analog converter either inverted or non-inverted before being applied thereto according to a value of a most significant bit of said digital image signal; and

said switched capacitor type digital-to-analog converter generates a voltage in the range of said first reference voltages if said lower N−1 bits are applied non-inverted, and generates a voltage in the range of said second reference voltages if said lower N−1 bits are inverted before being applied thereto.

9. The driving circuit of an electro-optical device according to claim 6, wherein said switched capacitor type digital-to-analog converter comprises:

a first through an N−1th capacitive elements, each capacitive element respectively having a pair of opposed electrodes, wherein one of said first reference voltages or one of said second reference voltages is selectively applied to one of said opposed electrodes according to a value of a most significant bit of the digital image signal;

a capacitive element resetting circuit for short-circuiting said pair of opposed electrodes in each of said first through N−1th capacitive elements so as to discharge electric charges therein;

a signal line potential resetting circuit for selectively resetting a potential of said signal line to the other of said pair of first reference voltages or the other of said pair of second reference voltages according to the value of said most significant bit; and

a selective switching circuit including a first through N−1th switches that selectively connect said first through N−1th capacitive elements to said signal lines, respectively, according to values of lower N−1 bits after the discharge by said capacitive element resetting circuit and the resetting by said signal line potential resetting circuit.

10. The driving circuit of an electro-optical device according to claim 9, wherein:

the capacitance of said first through N−1th capacitive elements is set to $Cx2^{i-1}$ where C is a predetermined unit capacitance, and i is a positive integer between 1 and N−1.

11. The driving circuit of an electro-optical device according to claim 1, wherein the values of said first and second

reference voltages are set so that a difference between said driving voltage corresponding to the m−1th gray scale level and said driving voltage corresponding to the m-th gray scale level is smaller than a predetermined value.

12. The driving circuit of an electro-optical device according to claim **11**, wherein the values of said first and second reference voltages are set so that a ratio of said optical characteristic where said electro-optical device is driven by said driving voltage corresponding to the m−1th gray scale level to said optical characteristic where said electro-optical device is driven by said driving voltage corresponding to the m-th gray scale level is equivalent to one gray scale level obtained by dividing a variation range of said optical characteristic by (2^N-1).

13. The driving circuit of an electro-optical device according to claim **1**, wherein said digital-to-analog converter comprises a resistance ladder that divides said first and second reference voltages, respectively, by a plurality of resistors connected in series.

14. The driving circuit of an electro-optical device according to claim **13**, further comprising a selective voltage supply circuit for selectively supplying either said first or second reference voltages to said digital-to-analog converter according to a value of a most significant bit of said digital image signal, and

said digital-to-analog converter further comprising:

a decoder that decodes lower N−1 bits of said digital image signal and outputs decoded signals through 2^{N-1} output terminals, and

2^{N-1} switches, one terminal of each of said 2^{N-1} switches connected to each of a plurality of taps from said plurality of resistors and another terminal thereof connected to each of said signal lines, each 2^{N-1} switch respectively operated according to the decoded signals output through said 2^{N-1} output terminals.

15. The driving circuit of an electro-optical device according to claim **1**, wherein said signal lines are provided with predetermined capacitors in addition to a parasitic capacitance of said signal lines.

16. The driving circuit of an electro-optical device according to claim **1**, wherein said electro-optical device is a liquid crystal device comprising a liquid crystal held between a pair of substrates, and said driving circuit is formed on one of said substrates.

17. The driving circuit of an electro-optical device according to claim **16**, wherein said first and second reference voltages are respectively supplied to said digital-to-analog converter with a voltage polarity with respect to a predetermined reference potential being inverted for each horizontal scanning period.

18. An electro-optical device comprising the driving circuit according to claim **1**.

19. Electronic equipment comprising the electro-optical device according to claim **18**.

20. The driving circuit of an electro-optical device according to claim **2**, wherein at least one pair among a pair of terminals for the first reference voltages and a pair of terminals for the second reference voltages are disposed so that a pair of terminals can be connected to an identical connecting terminal.

21. A driving method of an electro-optical device having a digital-to-analog converter that supplies an analog image signal, which has a driving voltage corresponding to an arbitrary gray scale level among 2^N (where N is a natural number) gray scale level, to a signal line of the electro-optical device in which changes in an optical characteristic with respect to changes in said driving voltage are nonlinear, said driving method comprising the steps of:

supplying an N-bit digital image signal indicative of said arbitrary gray scale level to said digital-to-analog converter;

generating a voltage within a range of a first pair of reference voltages or a second pair of reference voltages according to a bit value of said digital image signal to produce said driving voltage corresponding to the gray scale level of said digital image signal so that the changes in said driving voltage with respect to the changes in the gray scale of said digital image signal are nonlinear, wherein the voltage is generated within the range of the pair of first reference voltages if said applied digital image signal indicates a first to m−1th gray scale level (where "m" is a natural number and $1<m\leqq 2^N$) and the voltage is generated within the range of the pair of second reference voltages if said digital image signal indicates an m-th to 2^N-th gray scale level; and

supplying said analog image signal having said generated driving voltage to said signal line.

22. A driving circuit for an electro-optical device, comprising:

an in put interface that receives an input N-bit digital image signal representing a gray scale value in a range of 2^N gray scale values (N is a natural number); and

a digital-to-analog converter that generates an analog driving voltage corresponding to the input digital image signal, and that supplies the analog driving voltage to a signal line, the digital-to-analog converter simultaneously generating the analog driving voltage for, and performing gamma correction with respect to, the input digital image signal, wherein the digital-to-analog converter generates the analog driving voltage in a first driving voltage range defined by a first pair of reference voltages if the input digital image signal represents a gray scale value from a first to an $m-1^{th}$ value (where m is a natural number and $1<m\leqq 2^N$), and generates the analog driving voltage in a second driving voltage range defined by a second pair of reference voltages if the input digital image signal value represents a gray scale value from an m^{th} to a 2^{Nth} value.

23. The driving circuit of an electro-optical device according to claim **22**, wherein a voltage polarity of said first pair of reference voltages and a voltage polarity of said second pair of reference voltages supplied to said digital-to-analog converter are set to be opposite from each other so that a change in said driving voltage corresponding to a change in the gray scale has an inflection point between said first and second driving voltage ranges.

24. The driving circuit of an electro-optical device according to claim **22**, wherein:

the value of said "m" is equal to 2^{N-1};

lower N−1 bits of said digital image signal are selectively applied to said digital-to-analog converter either inverted or non-inverted according to a value of a most significant bit of said digital image signal; and

said digital-to-analog converter generates a voltage in the range of said first reference voltage if said lower N−1 bits are non-inverted, and generates a voltage in the range of said second reference voltage if said lower N−1 bits are inverted.

25. The driving circuit of an electro-optical device according to claim **24**, further comprising a selective inverting circuit for selectively inverting said lower N−1 bits depend-

ing upon the value of said most significant bit, said selective inverting circuit being provided between said interface and said digital-to-analog converter.

26. The driving circuit of an electro-optical device according to claim **22**, further comprising a selective voltage supply circuit for selectively supplying either said first or second reference voltages to said digital-to-analog converter according to a value of a most significant bit of said digital image signal.

27. The driving circuit of an electro-optical device according to claim **22**, wherein said digital-to-analog converter comprises a switched capacitor type digital-to-analog converter adapted to generate voltages in the ranges of said first and second reference voltages, respectively, by means of charging a plurality of capacitors.

28. The driving circuit of an electro-optical device according to claim **27**, wherein said first reference voltages include a pair of voltages that enable a voltage in said first driving voltage range to be selectively generated, and said second reference voltages include a pair of voltages that enable a voltage in said second driving voltage range to be selectively generated.

29. The driving circuit of an electro-optical device according to claim **28**, wherein:

the value of said "m" is equal to 2^{N-1};

the lower N−1 bits of said digital image signal are selectively applied to said switched capacitor type digital-to-analog converter either inverted or non-inverted before being applied thereto according to a value of a most significant bit of said digital image signal; and

said switched capacitor type digital-to-analog converter generates a voltage in the range of said first reference voltages if said lower N−1 bits are applied non-inverted, and generates a voltage in the range of said second reference voltages if said lower N−1 bits are inverted.

30. The driving circuit of an electro-optical device according to claim **27**, wherein said switched capacitor type digital-to-analog converter comprises:

a first through an N−1th capacitive elements, each capacitive element respectively having a pair of opposed electrodes, wherein one of said first reference voltages or one of said second reference voltages is selectively applied to one of said opposed electrodes according to a value of a most significant bit of the digital image signal;

a capacitive element resetting circuit for short-circuiting said pair of opposed electrodes in each of said first through N−1th capacitive elements so as to discharge electric charges therein;

a signal line potential resetting circuit for selectively resetting a potential of said signal line to the other of said first reference voltages or the other of said second reference voltages according to the value of said most significant bit; and

a selective switching circuit including a first through N−1th switches that selectively connect said first through N−1th capacitive elements to said signal lines, respectively, according to values of lower N−1 bits of the digital image signal after the discharge by said capacitive element resetting circuit and the resetting by said signal line potential resetting circuit.

31. The driving circuit of an electro-optical device according to claim **30**, wherein:

the capacitance of said first through N−1th capacitive elements is set to $C\times 2^{i-1}$

where C is a predetermined unit capacitance, and i is a positive integer between 1 and N−1.

32. The driving circuit of an electro-optical device according to claim **22**, wherein the values of said first and second reference voltages are set so that a difference between said driving voltage corresponding to the m−1th gray scale level and said driving voltage corresponding to the m-th gray scale level is smaller than a predetermined value.

33. The driving circuit of an electro-optical device according to claim **32**, wherein the values of said first and second reference voltages are set so that a ratio of an optical characteristic of said electro-optical device driven by said driving voltage corresponding to the m−1th gray scale level to an optical characteristic of said electro-optical device driven by said driving voltage corresponding to the m-th gray scale level is equivalent to one gray scale level obtained by dividing a variation range of said optical characteristic by (2^{-1}).

* * * * *

US006326958B1

(12) **United States Patent**
Gorny et al.

(10) **Patent No.: US 6,326,958 B1**
(45) **Date of Patent: Dec. 4, 2001**

(54) **POWER PARTITIONED MINIATURE DISPLAY SYSTEM**

(75) Inventors: **Douglas J. Gorny; Douglas J. McKnight; Lowell F. Bohn, Jr.**, all of Boulder, CO (US)

(73) Assignee: **Zight Corporation**, Boulder, CO (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/311,891**

(22) Filed: **May 14, 1999**

(51) **Int. Cl.**[7] **G09G 5/00**

(52) **U.S. Cl.** **345/204**; 345/87; 345/88; 345/206

(58) **Field of Search** 345/199, 204, 345/205, 206, 208, 211, 212, 213, 89, 88, 87, 98, 100, 150, 153, 154, 155

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,769,632 * 9/1988 Work et al. 345/199
5,861,869 * 1/1999 Scheffer et al. 345/89
6,046,716 * 4/2000 McKnight 345/208

FOREIGN PATENT DOCUMENTS

5-216428 8/1993 (JP).
8-161086 6/1996 (JP).
10-253918 9/1998 (JP).

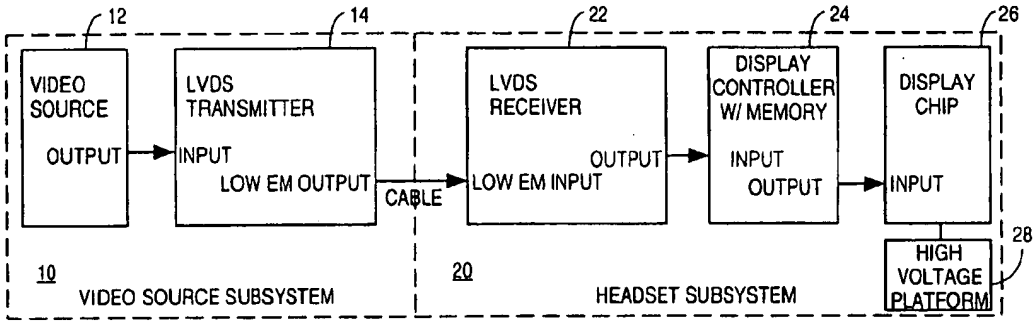
* cited by examiner

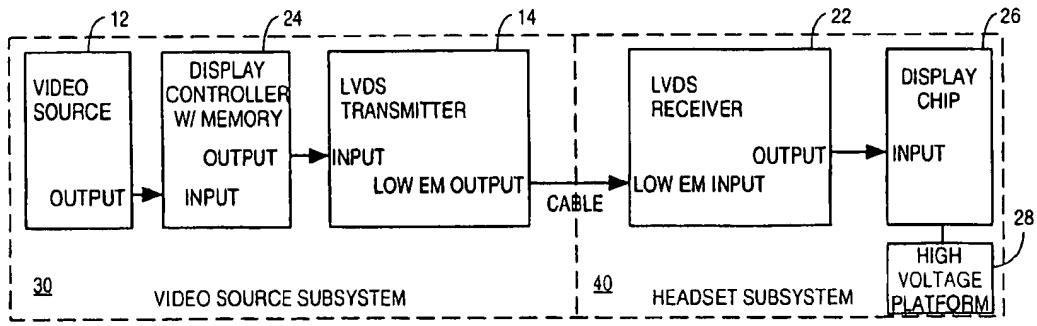
Primary Examiner—Xiao Wu
(74) *Attorney, Agent, or Firm*—Blakely, Sokoloff, Taylor & Zafman

(57) **ABSTRACT**

A system and method to reduce power consumption in a miniature display system. The system is formed on three distinct substrates with different feature sizes and operating in different power zones. The display controller and other high speed logic are formed on one substrate. The display, DACs and LUTs are formed on a second substrate, and high voltage circuitry for driving the LEDs and the cover glass voltage is formed on a third substrate.

13 Claims, 5 Drawing Sheets





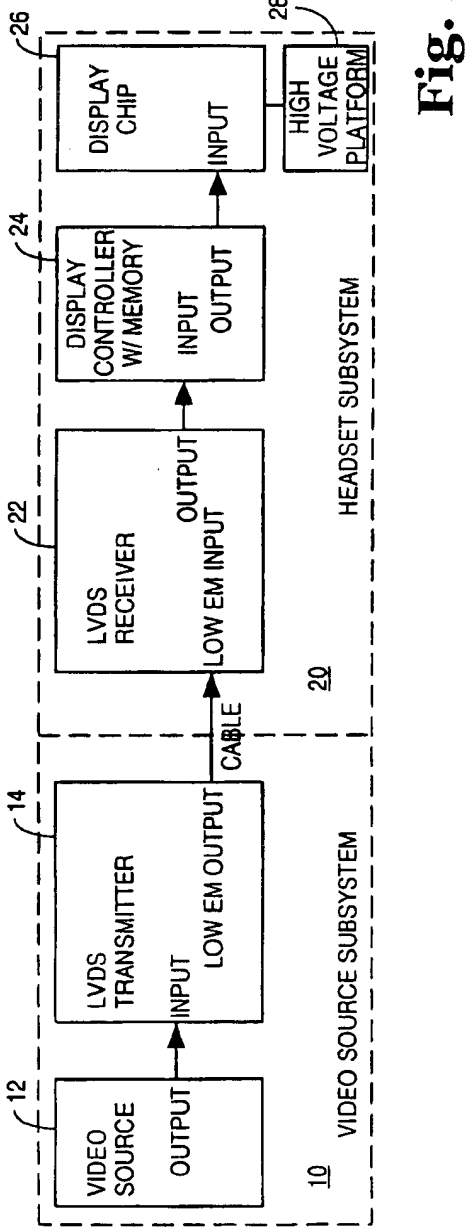

VIDEO SOURCE
OUTPUT
12
LVDS TRANSMITTER
INPUT
LOW EM OUTPUT
14
CABLE
LVDS RECEIVER
OUTPUT
LOW EM INPUT
22
DISPLAY CONTROLLER W/ MEMORY
INPUT
OUTPUT
24
DISPLAY CHIP
INPUT
26
HIGH VOLTAGE PLATFORM
28
VIDEO SOURCE SUBSYSTEM
10
20
HEADSET SUBSYSTEM

Fig. 1a

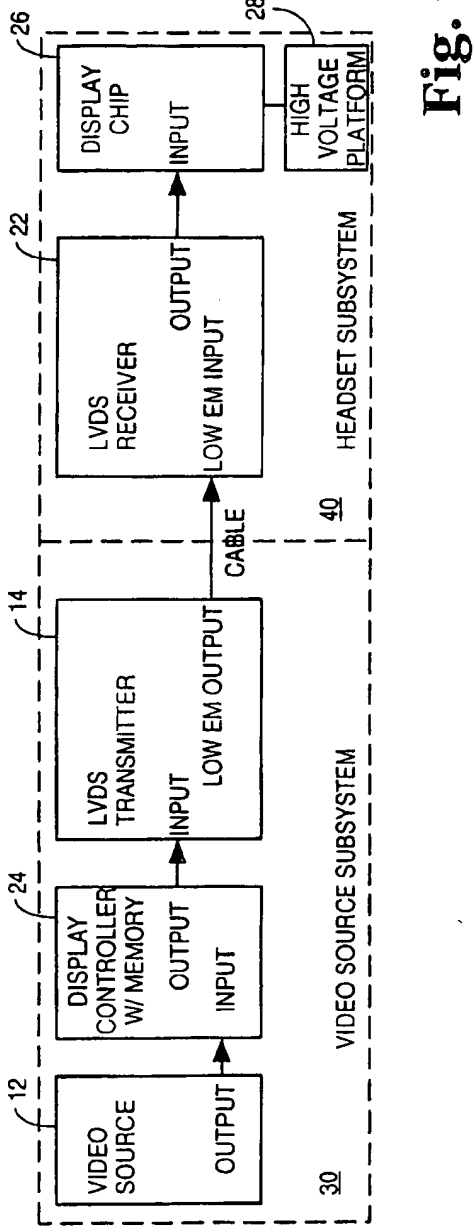

VIDEO SOURCE
OUTPUT
12
DISPLAY CONTROLLER W/ MEMORY
OUTPUT
INPUT
24
LVDS TRANSMITTER
INPUT
LOW EM OUTPUT
14
CABLE
LVDS RECEIVER
OUTPUT
LOW EM INPUT
22
DISPLAY CHIP
INPUT
26
HIGH VOLTAGE PLATFORM
28
VIDEO SOURCE SUBSYSTEM
30
40
HEADSET SUBSYSTEM

Fig. 1b

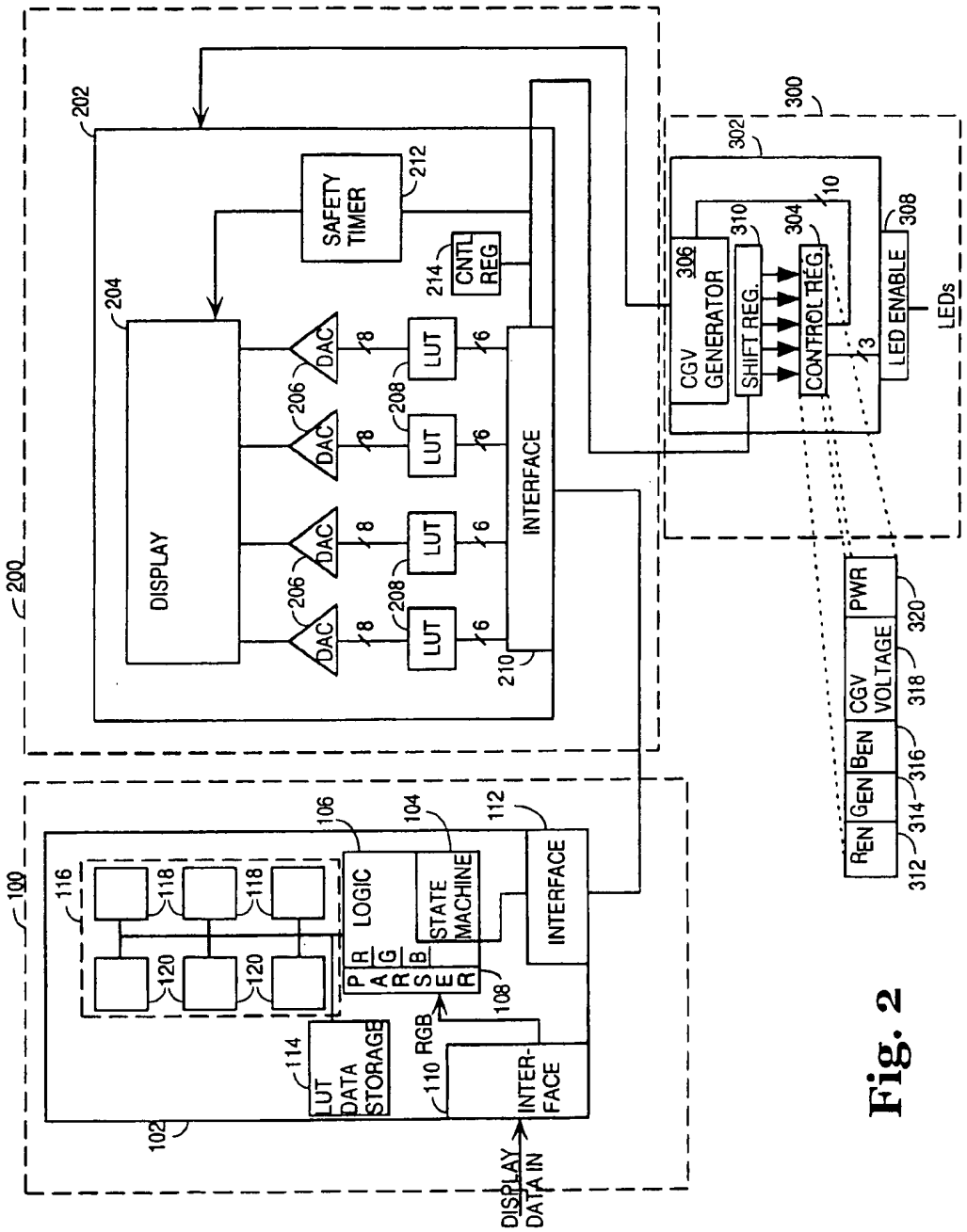

200
202
DISPLAY
204
SAFETY TIMER
212
CNTL REG
214
DAC
206
LUT
208
INTERFACE
210
300
302
CGV GENERATOR
306
SHIFT REG.
310
CONTROL REG.
304
LED ENABLE
308
LEDs
PWR
320
CGV VOLTAGE
318
BEN
316
GEN
314
REN
312
100
102
LOGIC
106
STATE MACHINE
104
INTERFACE
112
PARSER
108
RGB
110
LUT DATA STORAGE
114
INTER-FACE
DISPLAY DATA IN
116
118
120

Fig. 2

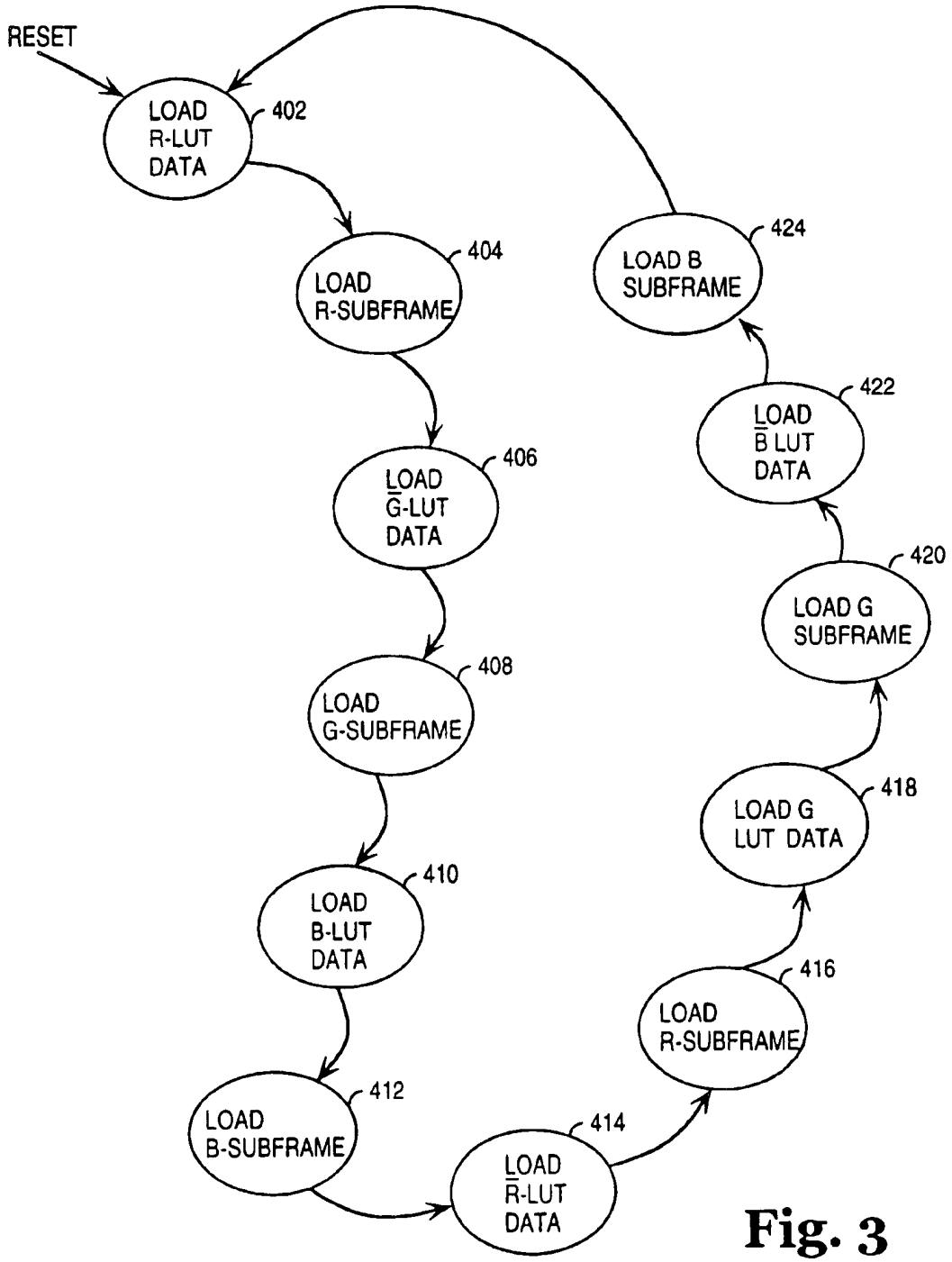

RESET
LOAD R-LUT DATA
402
LOAD R-SUBFRAME
404
LOAD $\bar{G}$-LUT DATA
406
LOAD G-SUBFRAME
408
LOAD B-LUT DATA
410
LOAD B-SUBFRAME
412
LOAD $\bar{R}$-LUT DATA
414
LOAD R-SUBFRAME
416
LOAD G LUT DATA
418
LOAD G SUBFRAME
420
LOAD $\bar{B}$ LUT DATA
422
LOAD B SUBFRAME
424

Fig. 3

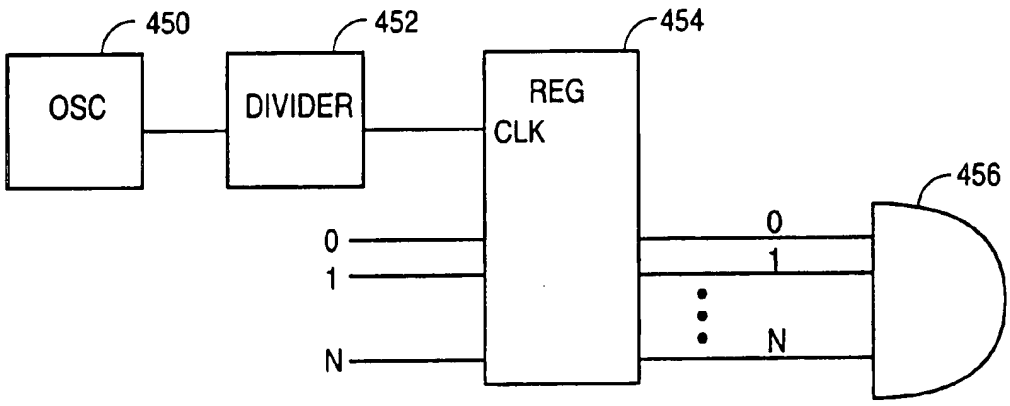


Fig. 4

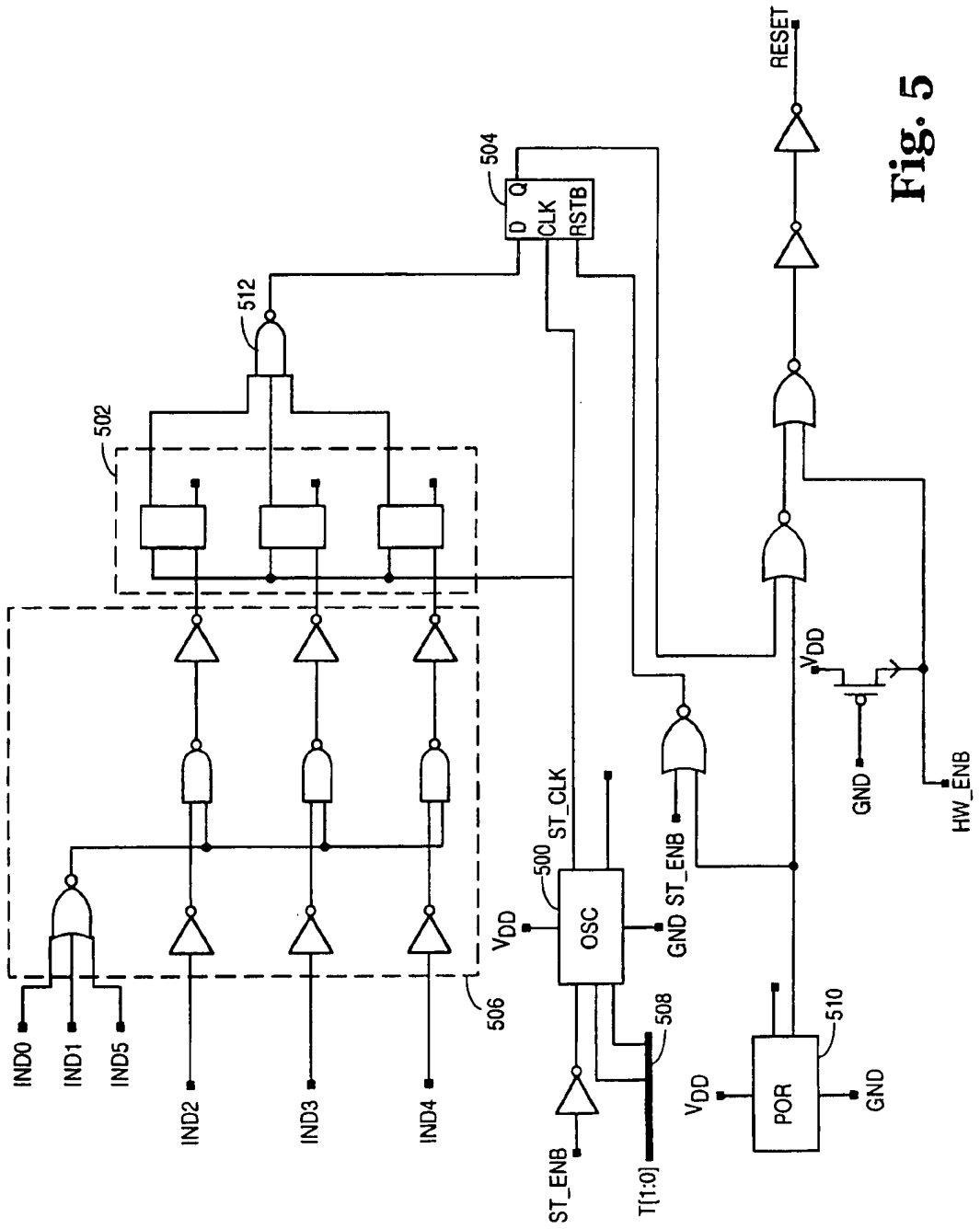

RESET
504
D
Q
CLK
RSTB
512
502
506
IND0
IND1
IND5
IND2
IND3
IND4
ST_CLK
500
OSC
VDD
GND
ST_ENB
508
T[1:0]
ST_ENB
510
POR
VDD
GND
VDD
GND
HW_ENB

Fig. 5

POWER PARTITIONED MINIATURE DISPLAY SYSTEM

BACKGROUND

(1) Field of the Invention

The invention relates to a small power efficient display system. More specifically, the invention relates to partitioning the display system into distinct power zones to minimize power consumption and size.

(2) Background

Liquid crystal displays have been known generally for many years. Initially, liquid crystal displays were formed on amorphous silicon substrates. Amorphous silicon tended to be slow, relatively large, and unsuited for formation of high speed logic and other device types. Liquid crystal displays then evolved into a polysilicon style which still had inadequate speed and logic compatibility characteristics. More recently, crystalline silicon has been employed to manufacture very small liquid crystal on silicon (LCOS) displays. These displays are much faster than the displays which use polysilicon to form display devices and can permit high speed driving of the individual pixels on display. In miniature displays, the challenge is to make the displays as small as possible and to also minimize power consumption, as these displays are increasingly used in a mobile environment with limited power resources.

The use of lookup tables (LUTs) is generally understood in the art. A LUT is effectively a listing of output codes which correspond to the possible input codes. The LUT performs a mapping of the input code to the output code, though the input code and output code may have different ranges. Typically, when LUTs are used in the context of displaying graphical data, three LUTs are employed to carry output codes corresponding to each of the color components (e.g. red, green, and blue) of a pixel. The subsequent three output codes are all simultaneously driven to the display to create the image of the color specified. Using three LUTs per pixel implies non-trivial die space to form the three LUTs, as well as power consumption by all those tables. In the context of miniature displays, it is desirable to minimize both die space and power consumption.

Because driving consecutive positive frames may cause liquid crystal malfunctions, liquid crystal display pixels are invariably driven by an alternating voltage having a positive and negative swing. While this places certain powering constraints on the system, it also necessitates use of frame inversion techniques in which the frame data is inverted to be driven by a negative signal. The required data inversion increases complexity of the display controller as well as power consumption and die are required.

It is also known in the art that liquid crystal displays can be damaged if exposed to DC voltage for a significant period of time. Thus, efforts have been made to reduce the risk of such damage. However, in the case of systems where the display is remote from the display controller, improper cable connections, a crash at the controller, or even a damaged cable can cause large and damaging voltages to be driven to a liquid crystal display. The problem arises how to protect the display from damages as a result of likely faults. Solutions to this problem are largely absent in the existing art.

BRIEF SUMMARY OF THE INVENTION

A system and method to reduce power consumption in a miniature display system is disclosed. The system is formed on three distinct substrates with different feature sizes and operating in different power zones. The display controller and other high speed logic are formed on one substrate. The display, DACs and LUTs are formed on a second substrate, and high voltage circuitry for driving the LEDs and the cover glass voltage is formed on a third substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1***a* and **1***b* are block diagrams of alternative configurations of a display system of one embodiment of the invention.

FIG. **2** is a block diagram of a display system of one embodiment of the invention.

FIG. **3** is an exemplary state diagram of one embodiment of the state machine.

FIG. **4** is a block diagram of a safety timer of one embodiment of the invention.

FIG. **5** is a schematic of a safety timer of one embodiment of the invention.

DETAILED DESCRIPTION

FIGS. **1***a* and **1***b* are block diagrams of alternative configurations of a display system of one embodiment of the invention. In FIG. **1***a*, a video source subsystem **10** includes a video source **12** coupled to a low voltage differential signaling (LVDS) transmitter **14**. LVDS transmitters and receivers are commercially available, and LVDS signaling is generally well-known in the art. A video signal from the video source **12** is converted by the LVDS transmitter and transmitted in a standard manner across a cable to an LVDS receiver **22** in headset subsystem **20**. A display controller with embedded memory **24** receives the output of the LVDS receiver **22** and stores the subframes of the image data in the embedded memory. Subframes are then sent out to display chip **26** which is also within the headset subsystem **20**. A high voltage platform **28** within the headset subsystem **20** is coupled to the display chip **26** and responsible for driving the cover glass voltage (CGV) of the display. In an alternative embodiment, by changing certain design parameters, the CGV may be driven from the display substrate. For example, the CGV range could be restricted to be driven by a voltage range that can be supplied directly from the display substrate such as 0 to 5 volts.

FIG. **1***b* shows a system employing the same components in a slightly different configuration. Specifically, video source subsystem **30** has video source **12** coupled to display controller with memory **24** (possibly embedded) which in turn provides its output to the LVDS transmitter **14** to be cabled to the LVDS receiver **22** in the headset subsystem **40**. The display chip **26** then receives the output of the LVDS receiver **22** and is supplied power in the same manner by high voltage platform **28** as described with reference to FIG. **1***a* above. The flexibility of the display controller and memory **24** to provide or receive LVDS signaling and also the display chip **26** to receive LVDS signaling permits significant flexibility in system design. Co-pending U.S. patent application Ser. No. 09/222,230, filed Dec. 29, 1998, describes an example of a display which may be used with embodiments of the invention, including the systems of FIGS. **1***a* or **1***b*; that application is hereby incorporated by reference.

FIG. **2** is a block diagram of a display system of one embodiment of the invention. In this diagram, LVDS transmitters and receivers are not shown, but it is within the scope and contemplation of the invention to configure the system

of FIG. **2** as shown in **1***a* or **1***b*, or the LVDS components may be omitted entirely. The system is segregated into three distinct power zones, **100**, **200**, **300**. Power zone **200** includes a substrate **202** which has a display **204** formed thereon. In one embodiment, display **204** is a liquid crystal on silicon (LCOS) display. Also formed on substrate **202** are a plurality of digital to analog converters (DACs) **206** which drive display **204**. Coupled to the DACs and also formed on substrate **202** are a plurality of lookup tables (LUTs) **208** in a one-to-one correspondence with the DACs. A set of control registers **214** are formed on substrate **202** and used to control the function of the other devices formed on substrate **202** and also provide control signals to a high-power platform in power zone **300**. A safety timer **212** is formed on a substrate **202**. Safety timer **212** is used to drive the display into a safe state in the event of certain system malfunctions. Safety timer **212** is described in further detail with respect to FIGS. **4** and **5** below. Interface **210** formed on substrate **202** may be a LVDS compliant interface and is responsible for directing incoming data appropriately to the LUTs **208** or the control register space **214**. The control register space includes registers required to manage display functions and registers to hold control information to be sent to substrate **302** (discussed below). Among the control registers are a DAC standby register to power and remove power from the DACs, a start of frame registers to signal the start of a new frame, LED enable register, and a cover glass voltage register. Additional useful registers will occur to one of ordinary skill in the art. Typically, the display **204** occupies 80–90% of the die space of substrate **202**. It operates at a 5 V level and is driven by TTL level outputs. Thus, the formation of the devices on substrate **202** should be formed with a process having a feature size compatible with these needs. It has been found that 0.8 μ feature size is satisfactory. For even lower power consumption, a 0.45 μ feature size could be used for substrate **202**, while still maintaining 5 V operation if desired.

Substrate **202** is coupled to a substrate **302** which resides in power zone **300**. Substrate **302** is manufactured with a much larger feature size because of its voltage requirements. Particularly, the cover glass voltage (CGV) generator **306** generates the voltage for the cover glass of the display **204**. In one embodiment, the cover glass voltage requirements dictate that it be driven between a +6 V and −2 V. Co-pending U.S. patent application Ser. No. 08/801,994, filed Feb. 18, 1997, and U.S. patent application Ser. No. 08/994,033, filed Dec. 18,1997, describe examples of voltages which may be applied to a cover glass in exemplary embodiments, and these applications are hereby incorporated by reference. To supply this range, a larger feature size needs to be employed in the formation of CGV generator **306**. A 3 μ process has been found suitable. Also on substrate **302** is part of an LED driver **308** which enables the red, green and blue LEDs which illuminate the display **204** in a time sequential manner. Because it uses a significantly larger process, operations on substrate **302** occur at a much slower rate than, for example, on substrate **202**. Moreover, for space reasons, it is desirable to keep the circuitry on substrate **302** to a minimum. A simple data interface exists between substrate **202** and substrate **302** consisting of three lines, a data-in line, a clock line, and a load line. The data-in supplies data to a shift register **310** which shifts data into the shift register **310** responsive to the clock. Once the shift register **310** is full, a load signal along the load line causes the data in the shift register **310** to be transferred to control register **304**. Control register **304** is shown exploded out. It contains three LED enables, Red Enable **312**, Green Enable **314**, and Blue Enable **316**. These values are provided to the LED driver **308** and are the basis on which the LED driver **308** drives the corresponding LEDs. CGV **318** is a ten bit value that is provided to the CGV generator **306** from which the CGV generator **306** generates the appropriate voltage for the cover glass over substrate **202**. A final bit of control register **304** is the power bit **320** which causes substrate **302** to be powered or not powered, depending on whether the power bit is active.

Also coupled to the substrate **202** is display controller substrate **102** existing within power zone **100**. A coupling of substrate **102** to substrate **202** may be local or via cable through a pair of LVDS interfaces. Substrate **102** includes a logic unit **104** which functions as a display controller for the display. The logic unit **104** includes a state machine **106** which drives data in a color sequential manner to the display. A parser **108** may also be provided which accepts data in an RGB format and converts it to a parallelization of R, and then G, and then B. A storage unit **116**, which may be embedded dynamic random access memory (DRAM), is also formed on substrate **102**. A storage unit should include at least two logically distinct subunits.

By using two to six logically or physically distinct subunits, each with its own memory interface, a number of advantages are obtained. By way of example, because the display is driven in a time sequential manner with a clock speed of 100 MHz and four pixels are to be supplied to the display for each clock, a data rate of 400 megapixels from the memory to the display is required. This data rate must be maintained for an entire subframe which, for a 480,000 pixel display of one embodiment of the invention, is approximately 1.2 milliseconds. If no parser is provided such that the data is stored in RGB format, three times the data rate between memory and a temporary storage, such as a FIFO, is required. Moreover, the FIFO must be large enough to supply sufficient subframe data while the incoming image frame occupies the memory interface. Additionally, relatively large FIFOs must be supplied on the incoming side to hold the data while the output side (or another subunit of the input side) is being serviced. Even with the parser present such that the data is stored in separate logical storage areas, first red, then green, then blue, the complexity of the memory controller and FIFO is required for each subunit increase in both power usage and die space. In this example, the memory controller would need to handle four data streams (three in, one out) with different clock rates between the streams in and the streams out. By employing six independently accessible memory subunits (two sets of three, one for each subframe of the current frame, and one for each subframe of the next frame), each with their own memory interface, memory access is significantly simplified such that a simpler memory controller may be employed, smaller or no FIFOs may be used, and the memory to outgoing FIFO operational speed can be significantly reduced.

As shown, storage unit **116** is shown composed of six subunits **120** and **118**. Each subunit is presumed to have it own independent memory interface in this embodiment of the invention. Because a frame will be displayed simultaneously with one being loaded, the system ping pongs back and forth between subunits **118** and subunits **120** for loading/displaying. A LUT data storage unit **114** which may be part of storage unit **116** or formed as a separate memory type, such as SRAM, is also provided. LUT data storage **114** retains six LUT data sets, one corresponding to each of R, G, B, $\overline{R}$, $\overline{G}$, $\overline{B}$. This permits the system to use an inverted LUT data set rather than inverting the data itself, providing

greater flexibility in the inverting algorithm. Another embodiment permits the use of only three LUT data sets R, G, and B with inverses generated by logic **106**. In such embodiments, a small amount of storage is saved at a cost of more stringent DAC linearity requirements.

In one embodiment, interfaces **110** and **112** are both LVDS compliant, allowing greater flexibility in the positioning of the controller relative to the display. Interface **110** may optionally provide conversion from a YUV format to RGB format. Additionally, either interface **110** or parser **108** truncates incoming color data by dropping the two least significant bits thereby changing the resolution from eight bits per color to six bits per color, as stored in a storage unit **116**. This permits the controller chip to send four pixels (of six bits each) simultaneously to the display chip using standard LVDS techniques. The lookup table then maps the six bits into eight bits. A set of LUT data is basically a listing of output codes that correspond to each possible input code. Since the shown embodiment uses six bit input code, that implies 64 output codes selected from a 256 possible output codes. This expansion of codes permits the LUT to perform gamma correction, correct for the non-linearity of the system components, and address other human factors. Notably, since the 64 output codes are of eight bits each, moving a LUT data set in the shown embodiment is accomplished by moving 64 bytes of data. This is a trivial percentage of the data moved in a subframe. Moreover, there is a period of time after the subframe data is loaded into the display during which the liquid crystal is permitted to settle. Then there is a period during which the display is illuminated. During these periods, the LUT and the display controller are mostly unused. Thus, the load of the LUT data set can be accomplished during these periods with no impact on system timing.

Though the embodiment above describes a six to eight bit encoding through the LUT, it is within the scope and contemplation of the invention to perform other encodings. For example, a two to eight encoding would permit four colors to be selected from a very large palette and permit extremely high speed pixel throughput as twelve pixels could be processed simultaneously using the current 24 bit data path, assuming the twelve LUTs and twelve DACs are also provided. It is also within the scope and contemplation of the invention that the output coding may be greater than eight bits. Such merely increases the size of the LUT data set and provides a larger palette from which to select output codes.

In the typical course of operation, a first frame is loaded into, for example, subunits **118** as three distinct subframes, e.g. a red subframe, a green subframe, and a blue subframe. A state machine **106** then begins feeding the subframes to the display substrate **202** preceded by an appropriate LUT data set. In addition to the **24** data signals moving between controller substrate **102** and display substrate **202**, there are also a mode signal, a reset signal, a clock signal, and a chipselect signal. The chipselect signal permits the display controller to drive multiple displays by selecting only the one to which the frame should be sent. The mode signal selects between a register mode and a data mode. In data mode, four pixels of data are moved across the 24 lines on each clock. In register mode, the data lines become nine address lines, eight data lines, a read line and a write line (with five lines unused). It is in register mode that LUT writes and register writes occur. It will be recognized that these twenty-eight signals are readily transferred using LVDS techniques.

The LUT is loaded first with an appropriate LUT data set corresponding to the immediately following subframe and provides the necessary mapping of six bit color data to eight bit display data. The LUT data set is selected to accommodate for non-linearities in the DACs **206** and the liquid crystal response to the particular color. LUTs may also be used to perform gamma correction, for example. While to first order, e.g. R and $\overline{R}$ LUT data sets are true inverses of each other, in reality, secondary effects such as the difference in non-linearity of the liquid crystal or the DAC when exposed to a negative voltage may require greater difference between the positive and inversed LUT data set. This ability to compensate for these differences provides improved image quality of standard frame inversion techniques. Because a relatively small amount of data is required for LUTs, moving it from the controller chip to the display chip has a negligible effect on system efficiency. It is also possible to load all four LUTs simultaneously with the same data, thereby increasing the efficiency of the transfer. By loading the LUTs before each subframe, the number of LUTs required on the display chip is reduced. This saves space and reduces power consumption of the overall system.

Subsequently, the color data is applied to the LUTs with one pixel to each LUT, thus, four pixels (in the same monochrome subframe) are processed simultaneously and then driven by the DACs onto the display. An entire subframe is driven to the display after which the display is illuminated by the corresponding LED color. Subsequently, the other two subframes are in turn driven to the display and illuminated. It should be recognized that the particular ordering of the red, green, blue subframes may be arbitrary. Additionally, it is desirable, when driving a liquid crystal display, to toggle between driving a positive subframe and driving an inverse subframe to protect the display from deleterious effects of constant voltage difference conditions. Accordingly, as mentioned above, the LUT data set selected to be driven to the LUT will alternate between a positive data set and an inverse data set.

FIG. **3** shows an exemplary state diagram of one embodiment of state machine **106**. Upon reset, the state machine enters a load R LUT data state. In this state, the LUT data set corresponding to R is loaded into the LUT on substrate **202**. In the case of FIG. **2**, the four LUTs receive the same LUT data for the red subframe in order to drive four separate pixels. Alternatively, when a different number of pixels is being driven (e.g. one pixel), then the substrate **202** would include the same (e.g. one) number of LUTs. A state machine then advances to the load R subframe state **404**. In this state, the R data from the logically distinct R buffer in storage unit **116** is passed through the LUTs and the corresponding values driven to corresponding pixels on the display **204**. The state then advances to the load $\overline{G}$ LUT data state **406**. In this state, the LUTs on substrate **202** are loaded with a data set corresponding to $\overline{G}$. The G subframe is then driven to the LUTs and the corresponding encoding is driven to the display four pixels at a time. Then at state **410**, the LUTs are loaded with a B LUT data set and the state advances to the load B subframe **412**. As with the subframes before it, the B subframe is driven to the display. By rapidly displaying the monochrome subframes, the human eye integrates the subframe to perceive a full color image. The incoming and outgoing subunits of storage unit **116** swap for the next series of states.

The $\overline{R}$ LUT data set is then loaded into the LUTs at state **414** and a next red subframe (in this case, from R subbuffer **120**) is driven through the LUTs and DACs to the display at state **416**. The state advances to state **418** in which the G LUT data set is loaded into the LUTs. The state then advances to **420** and the G subframe from G subbuffer **120**

is driven to the display, and so forth, at states **422** and **424** for the $\overline{B}$ LUT data and the corresponding B subframe. The state machine **104** then returns to state **402** and begins driving R LUT data again, as long as state machine **109** remains in the active displaying mode.

It is within the scope and contemplation of the invention to redisplay the data in the current subbuffer again before swapping subbuffers if the incoming data rate does not match the outgoing data rate one to one. Thus, if the input rate is one half the output rate, each frame would be displayed twice before a swap. Analogous cases exist for greater disparities between input and output rates.

Another embodiment uses only one set of subbuffers in storage unit **116** to hold data to be displayed. In this embodiment, parser **108** allows the subbuffer, e.g. **118**, to be randomly written with new pixel data during the times when the subbuffer is not being accessed to provide data to the display. In this case, the same order as described above with reference to FIG. **3** occurs, but no swap of subbuffers is used. This ordering is repeated over and over, allowing input access during the non-displaying time.

While in the embodiment of FIG. **3**, only six LUT data sets are used and only a single display loop exists within the state machine, it is within the scope and contemplation of the invention to have multiple display loops and an arbitrary large number of groups of data sets. For example, one embodiment of the invention might use one group of LUT data sets R_1, G_1, B_1, $\overline{R}_1$, $\overline{G}_1$, $\overline{B}_1$for temperatures below a certain threshold and a second group R_2, G_2, B_2, $\overline{R}_2$, $\overline{G}_2$, $\overline{B}_2$, for temperatures above the threshold. The corresponding state machine would look like FIG. **3** duplicated with temperature selecting the loop of states through which the state machine transitions. Similar, different groups of data sets may be used for different frame rates or different contrast settings, environmental conditions, liquid crystal, etc. Other bases for using multiple groups of data sets are also within the scope and contemplation of the invention. For example, for an LED display (rather than a liquid crystal display), the LUT data sets may require R, G, B and no inverted sets.

Detection of fault conditions in a display is important to avoid damage to the display. As used herein, fault means anything affecting the status of the circuitry or software driving the display or the display itself. A number of problems may occur that cause the display to become hung up with a constant CGV and a DC voltage across the liquid crystal. Even with small voltage differences between the cover glass and the underlying pixels, damage may occur to the liquid crystal. Examples of fault that my occur include a crash of the display controller or the host video source that causes the display controller to leave its display state machine with the subframe unfinished. Hot plugging the cable or improperly coupling the cable may also cause the system to hang. The safety timer as described below can be used to drive the display into a safe state in the event of potentially damaging faults. Because a pathological condition that causes the power to the display to be wholly disrupted is also a "safe state" for the display, the safety timer need only address the conditions during which power is supplied to the display chip substrate.

FIG. **4** shows a block diagram of a safety timer of one embodiment of the invention. An oscillator **450** independent of the clock that drives the remainder of the display chip is employed to provide the safety timer clock. A clock divider **452** may optionally be employed to expand the period during which indicators of proper function will be collected from the fundamental frequency of the oscillator. An arbitrarily large number of indicators (0–N) may be collected during the period and stored in a register **454** or series of flip flops. Individual register positions are then effectively ANDed together or an expected set of indicators may be compared with a set of indicators actually received. Other methods of determining if all indicators have been received are within the scope and contemplation of the invention. If all the indicators are received during the specified period, the system is then deemed to be working properly. If all the indicators were not received during the specified period, a result at the AND **456** is false and the timer drives the display into a safe state. A safe state is defined in one embodiment as having a CGV of zero volts and all the pixels driven to zero volts. Reset, the safe state, is maintained until all the indicators are collected during an appropriate time period. Thus, if the deficiency is a permanent condition, the reset will be permanently maintained until the system is fixed. If the failure to receive an indicator is transient, possibly on the next oscillator cycle, the reset will be released. Significantly, it is important during reset to allow the interface **210** on substrate **202** to continue to receive signals, otherwise, a timer will never come out of reset.

FIG. **5** shows a schematic of a safety timer of one embodiment of the invention. A plurality of indicators, IND0 through IND5, are fed into combinational logic **506**. The indicators may be signals available in raw form on the display chip or signals derived from additional combinational logic (not shown) that is also formed on the display chip. The results of combinational logic **506** are retained in flip flops **502** and combined by NAND gate **512** for storage of a single signal in flip flop **504**. The independent oscillator **500** provides all clocking for the safety timer circuit. Oscillator **500** includes a divider circuit which is driven by T signals **508**. The T signal is a two bit signal which provides four possible clock periods from oscillator **500**. The T signal may be provided by a register in the register space. The power on reset (POR) circuit **510** is also provided to ensure that the safety timer provides a reset at power on and allows the system to stabilize before releasing the reset or safety mode. In one embodiment, on reset, all register values on the display chip return to default values when the timer comes out of reset. This is desirable because it is assumed that a pathological condition usually causes the timer to force the chip into safe mode, or reset. Thus, it is reasonable to presume that there may have been some corruption of register values during that pathological condition. By returning the registers to default values, any corrupted values are overwritten. A hard wired enable (HW_ENB) is supplied so that the timer can be permanently disabled if desired for a particular application or system. Safety timer enable (ST_ENB) may be used to temporarily disable the safety timer when such is desired, as is certain test cases.

The particular indicators selected may vary between different designs. However, the selection of indicators will affect the combinational logic **506** required. In the shown embodiment, IND**0**, IND**1**, and IND**5**, collectively, indicate whether a write to any register in the control register space of the display chip has occurred. IND2, IND3, and IND4 reflect whether a write to specific registers in the control register block has occurred. For example, IND2 may indicate whether the load register for the high voltage platform has been written to, IND3 might indicate whether a frame start register has been written to, and IND4 might indicate whether a standby register has been written. The standby register causes the DACs to power down when not physically driving data to the display. This is desirable because the

DACs consume a significant amount of power and also running constantly may exhibit undesirable heat characteristics. All three of the above-noted indicators occur every frame for normal operation. For example, every frame must be started by a write to the frame start register, and it is necessary to load the high power platform to cause illumination of the array via the LED drivers, as well as to adjust the CGV. Thus, if the clock period of safety timer clock (ST_CLK) is equal to the frame rate, it is necessarily the case that all indicators should be received during the ST_CLK period.

In addition to selecting signals which would necessarily occur within a frame, in one embodiment of the invention, indicators are selected so that at least one indicator is provided along each channel of the LVDS cable. This has the advantage of permitting identification of errors related to damage to a single channel, for example, as a result of kinking of the cable. The above-described embodiment relies on register writes as the basis for operation of the safety timer. Other suitable indicators include pixel clock activity, LUT writes, selected data wires, and even cover glass switching. It is, of course, possible in principle to examine every incoming signal to ensure that all expected signals are received during each frame. However, that becomes unjustifiably overhead intensive with corresponding circuit size and power costs. Thus, by selecting a subset of indicators reflective of the faults of most concern to the system, a safety timer can be effectively implemented which protects the display subsystem from permanent damage as a result of those faults. Notably, the timer does not merely identify the existence of a fault condition and report, e.g. to the display controller, for corrective action. Rather, the safety timer drives the reset signal that places the display in a safe state.

In the foregoing specification, the invention has been described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes can be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense. Therefore, the scope of the invention should be limited only by the appended claims.

What is claimed is:

1. A system comprising:

a memory unit and a display controller formed on a first substrate;

a display, a digital to analog converter (DAC), and a lookup table (LUT) formed on a second substrate, the second substrate coupled to the first substrate; and

a cover glass voltage (CGV) driver and LED driver disposed on a third substrate, the third substrate coupled to the second substrate, wherein the first, second, and third substrates operate at three different voltage levels.

2. The system of claim 1 wherein the three substrates are manufactured using three different feature sizes.

3. The system of claim 2 wherein the first substrate is made using a feature size of less than 0.35μ, the second substrate is made using a feature size of between 0.25μ, and 0.8μ, and the third substrate is made using a greater than 0.8μ feature size.

4. The system of claim 1 wherein the first substrate and the second substrate are coupled together through a low voltage differential signaling (LVDS) interface.

5. The system of claim 1 wherein the display is a liquid crystal on silicon (LCOS) display.

6. The system of claim 1 wherein the memory unit comprises a plurality of subunits each with an independent memory interface.

7. The system of claim 6 wherein the plurality is equal to twice the number of subframes of an image to be displayed.

8. A method comprising:

receiving an input image data stream including frames of an image in a band interleaved format at a first substrate;

segregating individual bands of the band interleaved format to expose a plurality of monochrome subframes of a first frame;

storing the subframes in distinct storage subunits; and

concurrently with the receiving, driving subframes of a previously received frame to a lookup table (LUT) coupled to a display wherein both the LUT and the display are formed on a second substrate.

9. The method of claim 8 further comprising:

truncating each datum of the subframes prior to storing the subframes.

10. The method of claim 8 wherein the first substrate and the second substrate operate at different voltage levels.

11. The method of claim 10 further comprising:

driving a cover glass voltage for the display from a third substrate, the third substrate operating a higher voltage than either the first or second substrate.

12. The method of claim 8 wherein each distinct storage subunit has an independent memory interface.

13. An apparatus comprising:

a memory unit and a display controller formed on a first substrate;

a display, a digital to analog converter (DAC), a lookup table (LUT) and a cover glass voltage driver formed on a second substrate, the second substrate coupled to the first substrate; and

wherein the first and second substrates operate at different voltage levels.

* * * * *

US005589847A

United States Patent [19]

Lewis

[11] Patent Number: 5,589,847

[45] Date of Patent: Dec. 31, 1996

[54] **SWITCHED CAPACITOR ANALOG CIRCUITS USING POLYSILICON THIN FILM TECHNOLOGY**

[75] Inventor: **Alan G. Lewis**, Sunnyvale, Calif.

[73] Assignee: **Xerox Corporation**, Stamford, Conn.

[21] Appl. No.: **764,292**

[22] Filed: **Sep. 23, 1991**

[51] **Int. Cl.**[6] **G09G 3/36**

[52] **U.S. Cl.** **345/98**; 345/87

[58] **Field of Search** 257/310; 437/20, 437/57, 919; 340/718, 784; 345/98, 100, 87, 92

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,466,719	9/1969	Sharif et al.	437/919 X
3,988,824	11/1976	Bodway	437/919 X
4,169,746	10/1979	Ipri et al. .	
4,276,688	7/1981	Hsu .	
4,689,116	8/1987	Coissard et al. .	
4,694,314	9/1987	Terada et al. .	
4,720,467	1/1988	Muggli et al.	437/919 X
4,772,099	9/1988	Kato et al. .	
4,783,146	11/1988	Stephany et al. .	
4,814,289	3/1989	Baeuerle	437/919 X
4,872,002	10/1989	Stewart et al. .	
4,878,151	10/1989	Gallichio .	
4,918,454	4/1990	Early et al. .	
4,988,952	1/1991	Sevastopoulos et al. .	
5,042,916	8/1991	Ukai et al. .	

FOREIGN PATENT DOCUMENTS

0145606	6/1985	European Pat. Off. .
0263287	4/1988	European Pat. Off. .
59-182569	10/1984	Japan .
61-13665	1/1986	Japan .
2117970	10/1983	United Kingdom .
2138207	10/1984	United Kingdom .
WO86/02489	4/1986	WIPO .

OTHER PUBLICATIONS

Allan, R., "Thin-film Devices on Silicon Chip Withstand up to 500° C", *Electronics*, vol. 53, No. 1, (1980), pp. 39–40.

Wu, et al., "Retardation of Nucleation Rate for Grain Size Enhancement by Deep Silicon Ion Implantation of Low-Pressure Chemical Vapor Deposited Amorphous Silicon Films", *J. Appl. Phys.* 65(10) May 1989, pp. 4036–4039.

Lewis et al, IEEE International Solid-State Circuits Conference, pp. 222–223 (Feb. 16, 1990).

Lee et al, IEEE ISSCC Digest, pp. 220–221, (Feb. 16, 1990).

Stewart et al, SID Technical Digest, pp. 319–322 (1990).

Yamauchi et al, IEDM, pp. 353–356 (1989).

Kim et al, SID Technical Digest, pp. 304–306 (1990).

Nakazawa et al, SID Technical Digest, pp. 311–314 (1990).

Ono et al, IEDM, pp. 345–348 (1989).

(List continued on next page.)

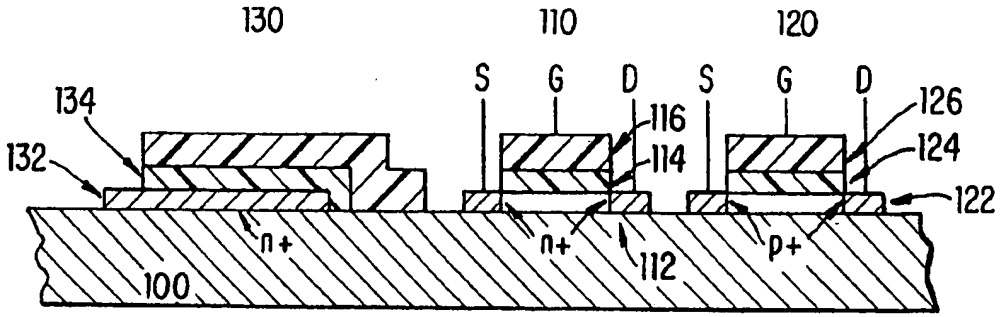
Primary Examiner—Ulysses Weldon

Attorney, Agent, or Firm—Oliff & Berridge

[57] **ABSTRACT**

Switched capacitor analog circuits (such as integrators, amplifiers and digital-to-analog converters) constructed from polysilicon thin film transistors and capacitors are disclosed. The circuits are commonly implemented using conventional single crystal CMOS technologies, but this is the first time they have been realized using polysilicon TFT CMOS. The performance of the circuits is inevitably worse than that of conventional single crystal CMOS devices, but is nevertheless adequate for many large area applications. The circuits can be fabricated on large area substrates and integrated with, for example, flat panel displays, pagewidth optical scan arrays, or pagewidth printheads, offering improvements in the functionality and performance of those devices. Charge redistribution amplifiers and digital-to-analog converters are shown to operate with settling times ranging from a few microseconds to a few tens of microseconds, even with large capacitive loads, despite the relatively poor performance of polysilicon TFTs in comparison to conventional MOSFETS. Better than 8-bit accuracy is also demonstrated for the digital-to-analog converters.

27 Claims, 14 Drawing Sheets



OTHER PUBLICATIONS

Lewis et al, IEDM, pp. 349–352 (1989).
Wu et al, SID Technical Digest, pp. 307–310 (1990).
Matsueda et al, SID Technical Digest, pp. 315–318 (1990).
Lewis et al, IEDM, pp. 261–263 (1988).
Lewis et al, IEDM, pp. 264–267 (1988).
Cho et al, Abstract, "Charge-Sensitive Poly-silicon Amplifiers for A-Si:H Pixel Particle Detectors (1991)".

Borkan, Electronics, pp. 53–60 (Apr. 20, 1964).

Weimer, Proceedings of the IRE, pp. 1462–1469 (Jun. 1962).

Bipolar and Mos Analog Integrated Circuit Designs, Grebene, publisher: John Wiley and Sons, pp. 703–711, 761–764.

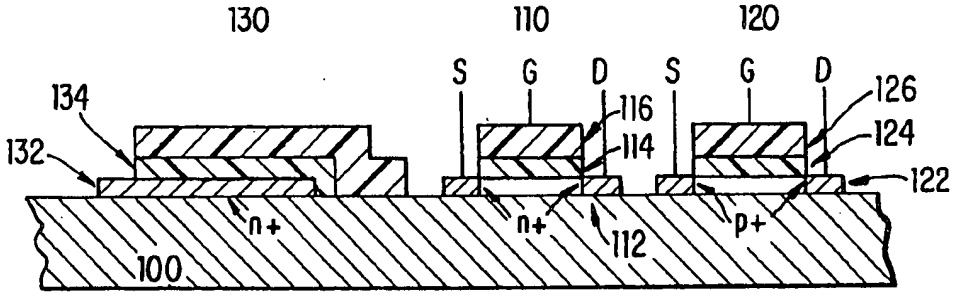


FIG. 1

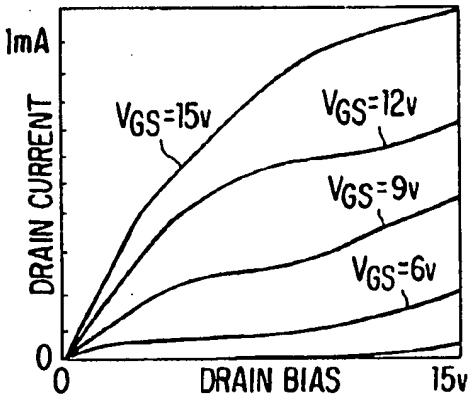


FIG. 2A

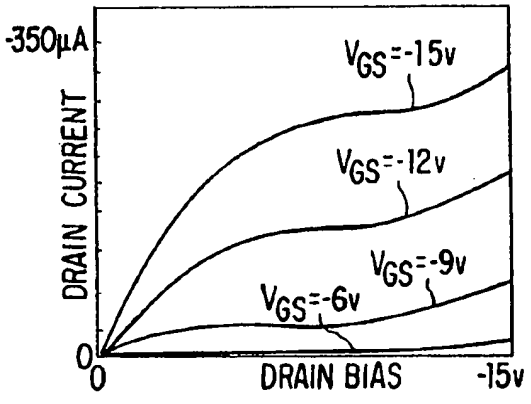
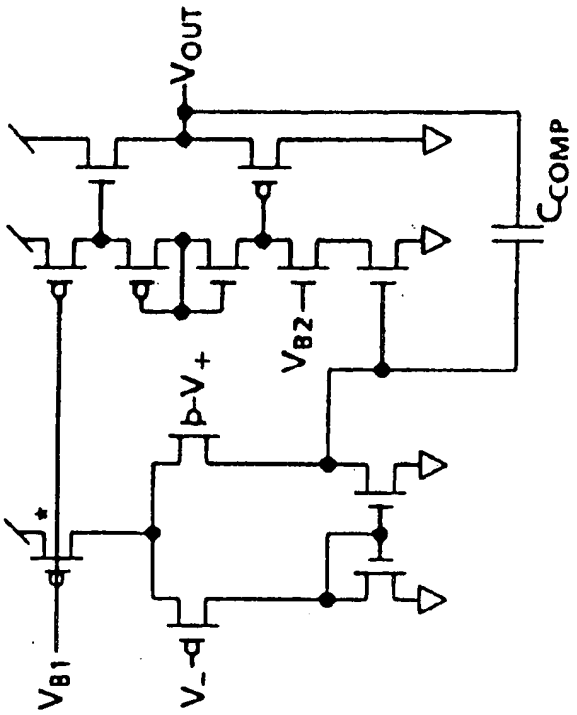
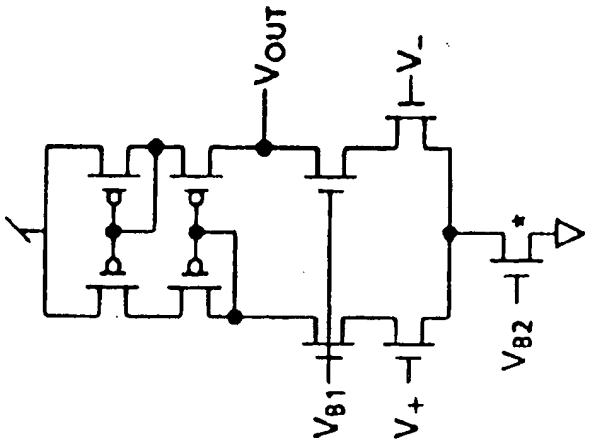


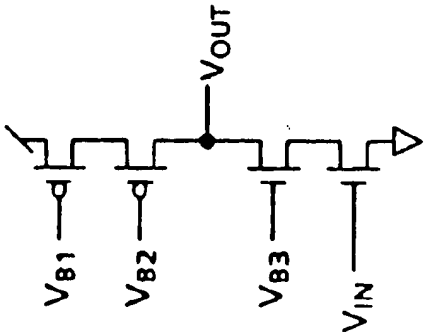
FIG. 2B



Type III FIG. 3C



Type II FIG. 3B



Type I FIG. 3A

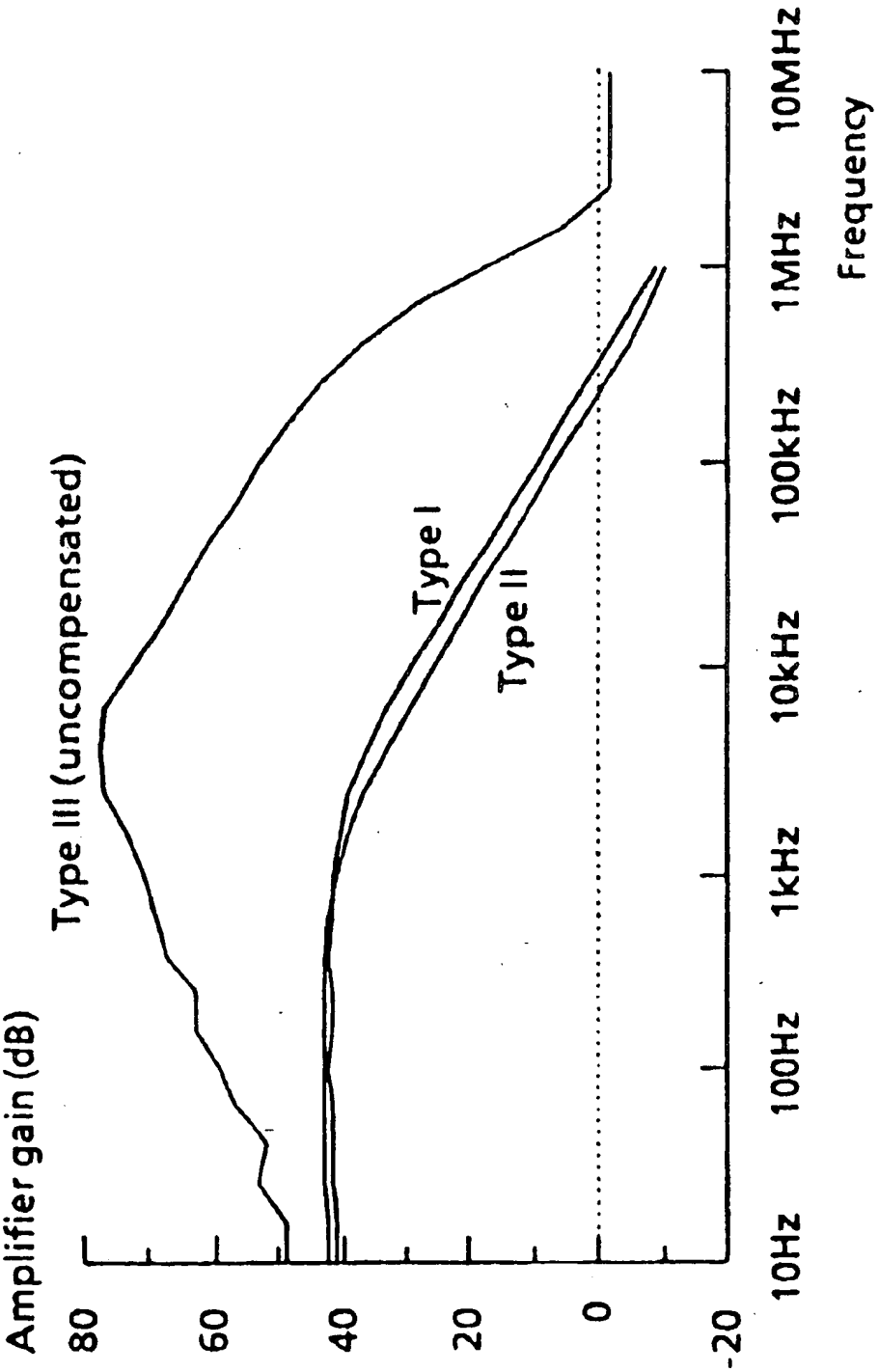

Amplifier gain (dB)
80
60
40
20
0
-20
10Hz
100Hz
1kHz
10kHz
100kHz
1MHz
10MHz
Frequency
Type III (uncompensated)
Type I
Type II

FIG. 4

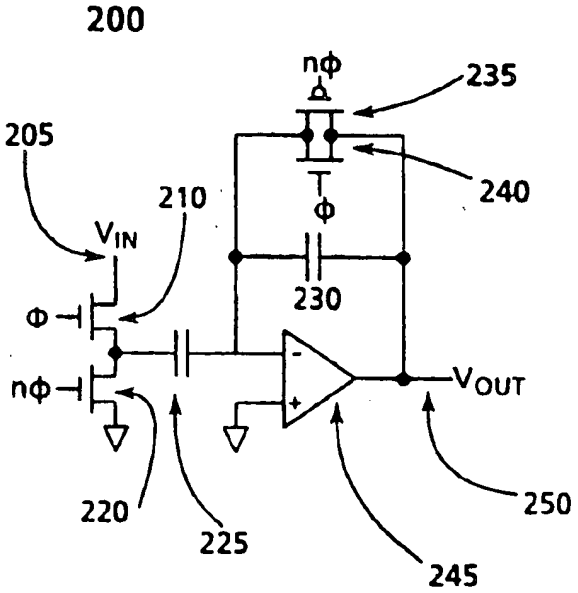

200
nϕ
235
205
240
210
ϕ
VIN
230
ϕ
nϕ
VOUT
220
225
245
250

FIG. 5

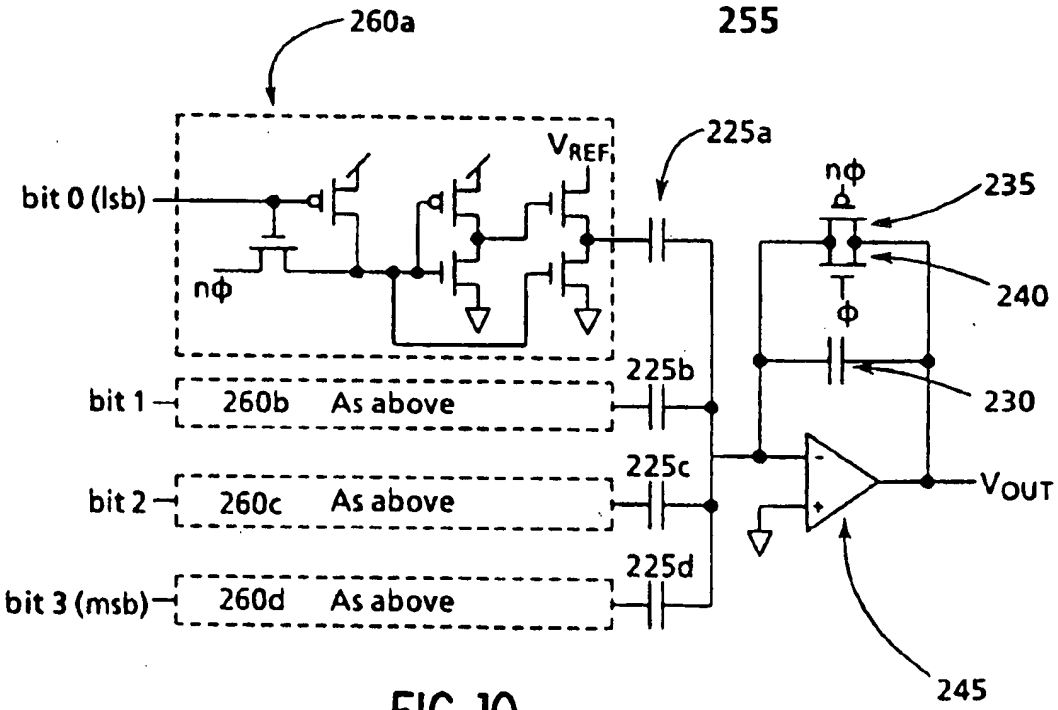

260a
255
VREF
225a
bit 0 (lsb)
nϕ
nϕ
235
240
ϕ
225b
bit 1
260b As above
230
225c
bit 2
260c As above
VOUT
225d
bit 3 (msb)
260d As above
245

FIG. 10

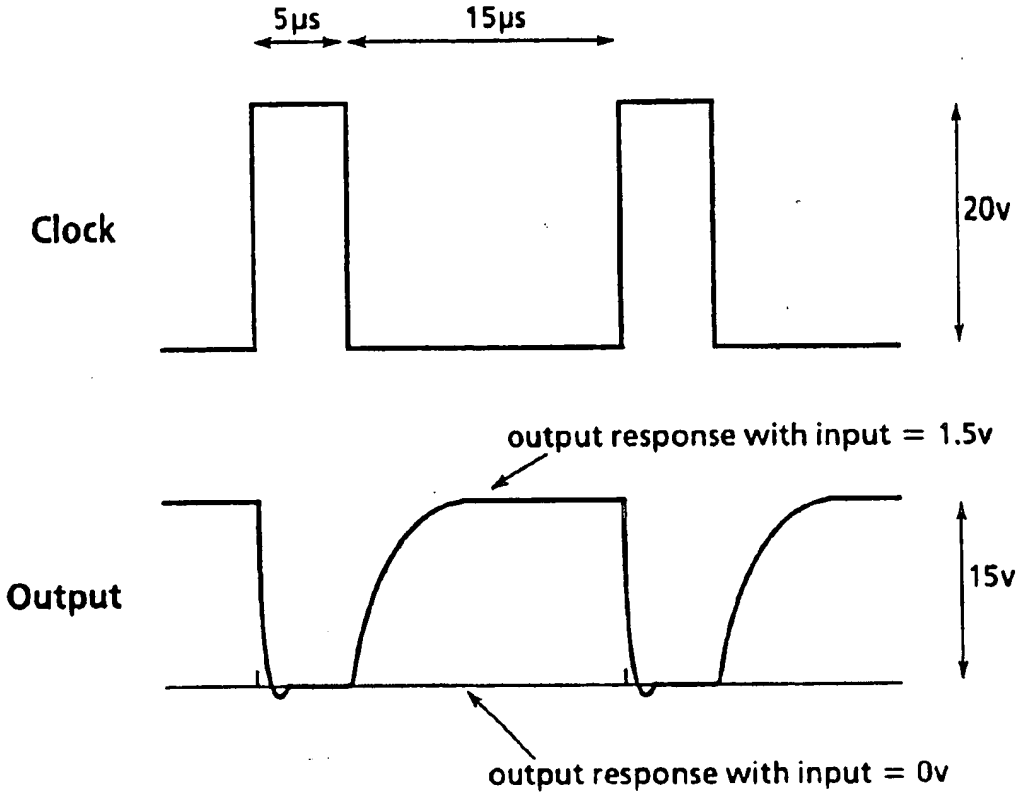

5μs
15μs
Clock
20v
output response with input = 1.5v
Output
15v
output response with input = 0v

FIG. 6

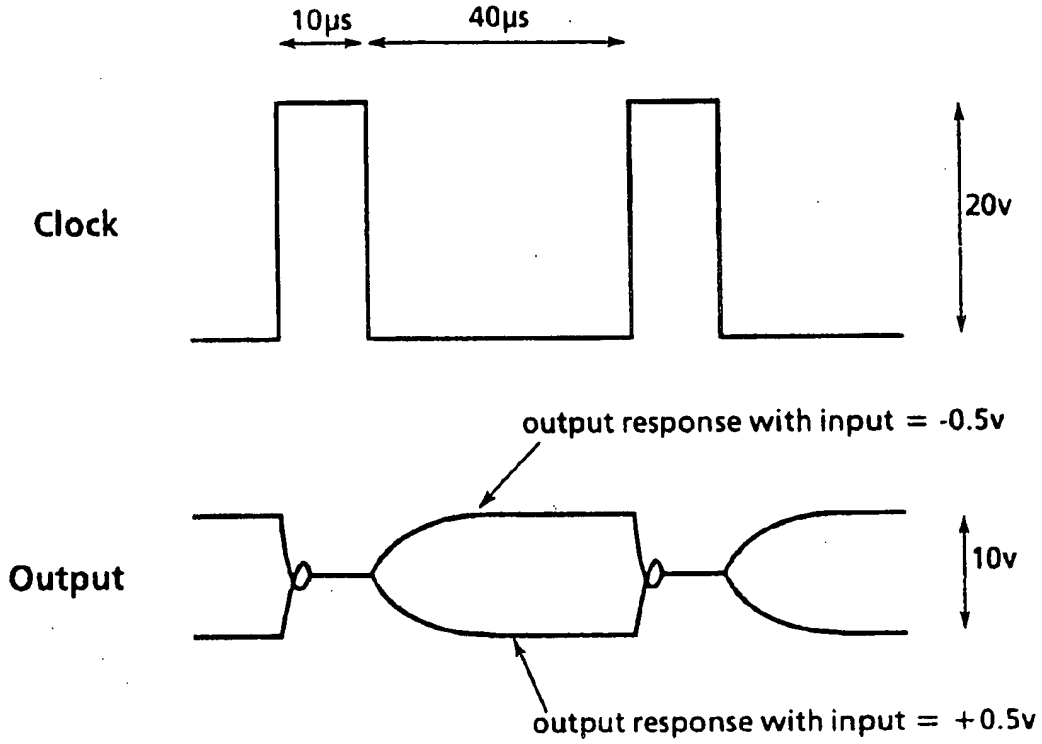

10μs
40μs
Clock
20v
output response with input = -0.5v
Output
10v
output response with input = +0.5v

FIG. 7

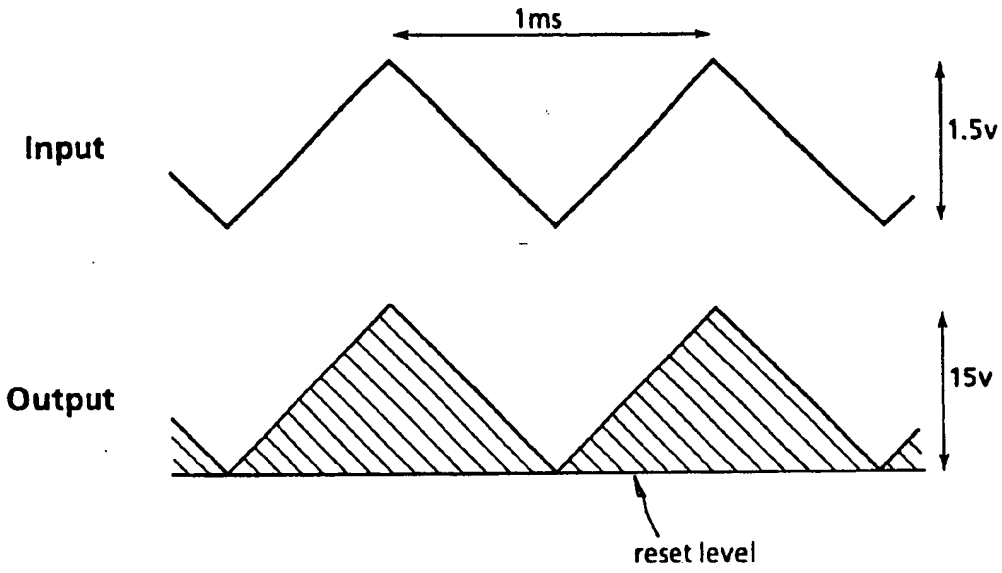


FIG. 8

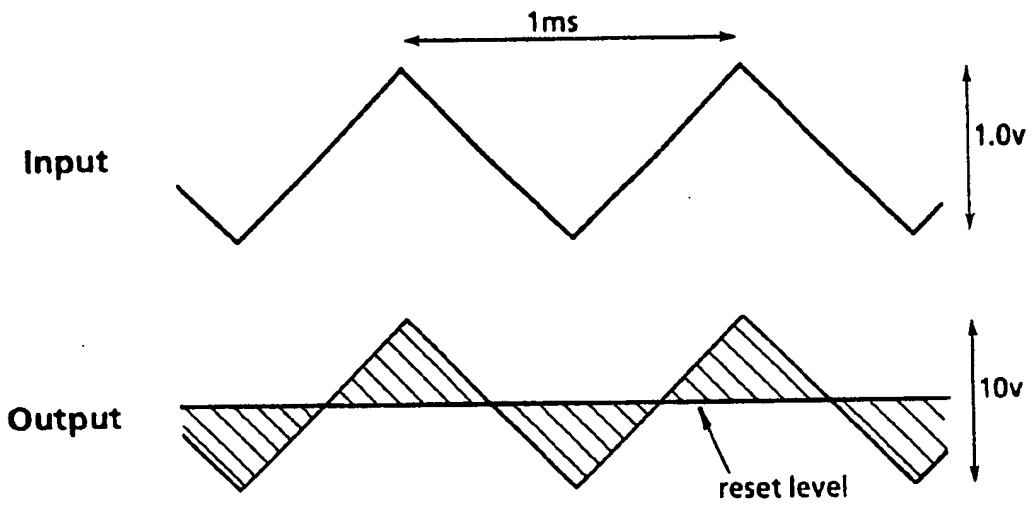


FIG. 9

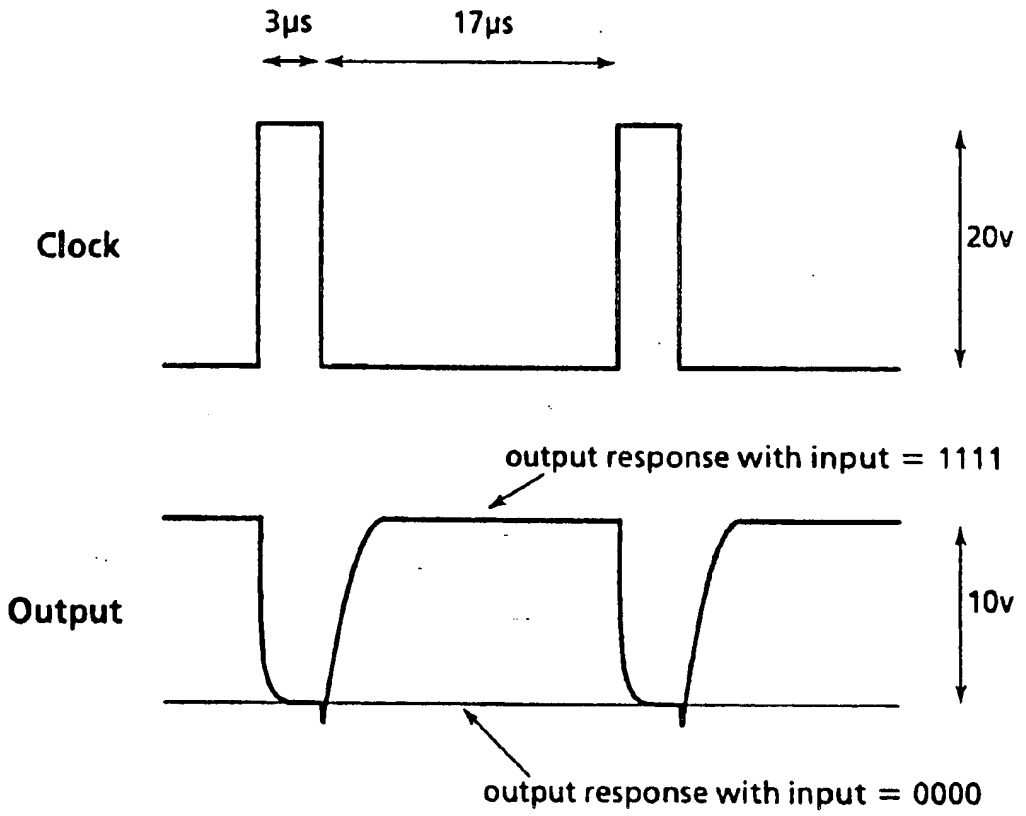

3μs
17μs
Clock
20v
output response with input = 1111
Output
10v
output response with input = 0000

FIG. 11

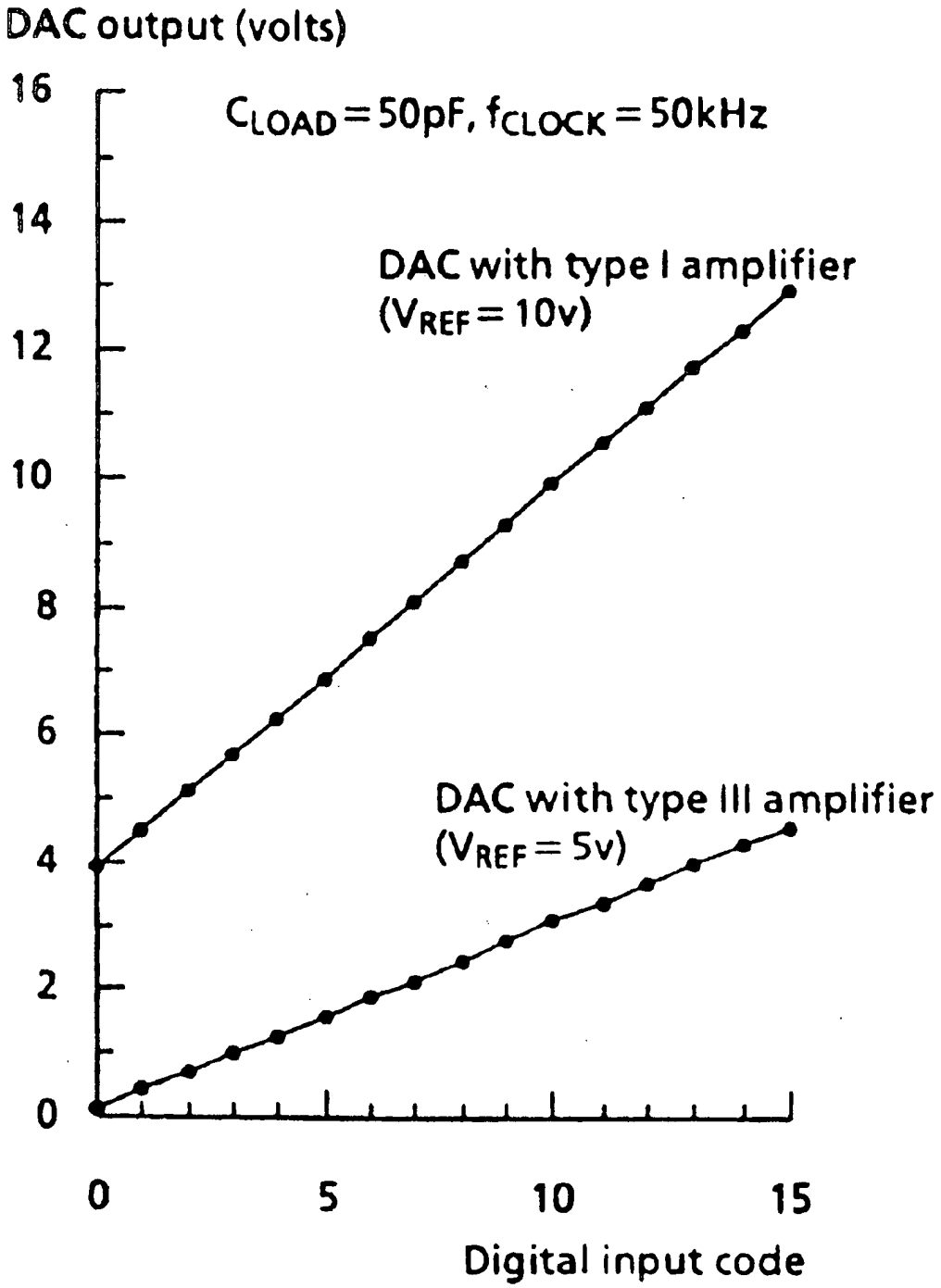

DAC output (volts)
16
14
12
10
8
6
4
2
0
$C_{LOAD} = 50pF$, $f_{CLOCK} = 50kHz$
DAC with type I amplifier
($V_{REF} = 10v$)
DAC with type III amplifier
($V_{REF} = 5v$)
0
5
10
15
Digital input code

FIG. 12

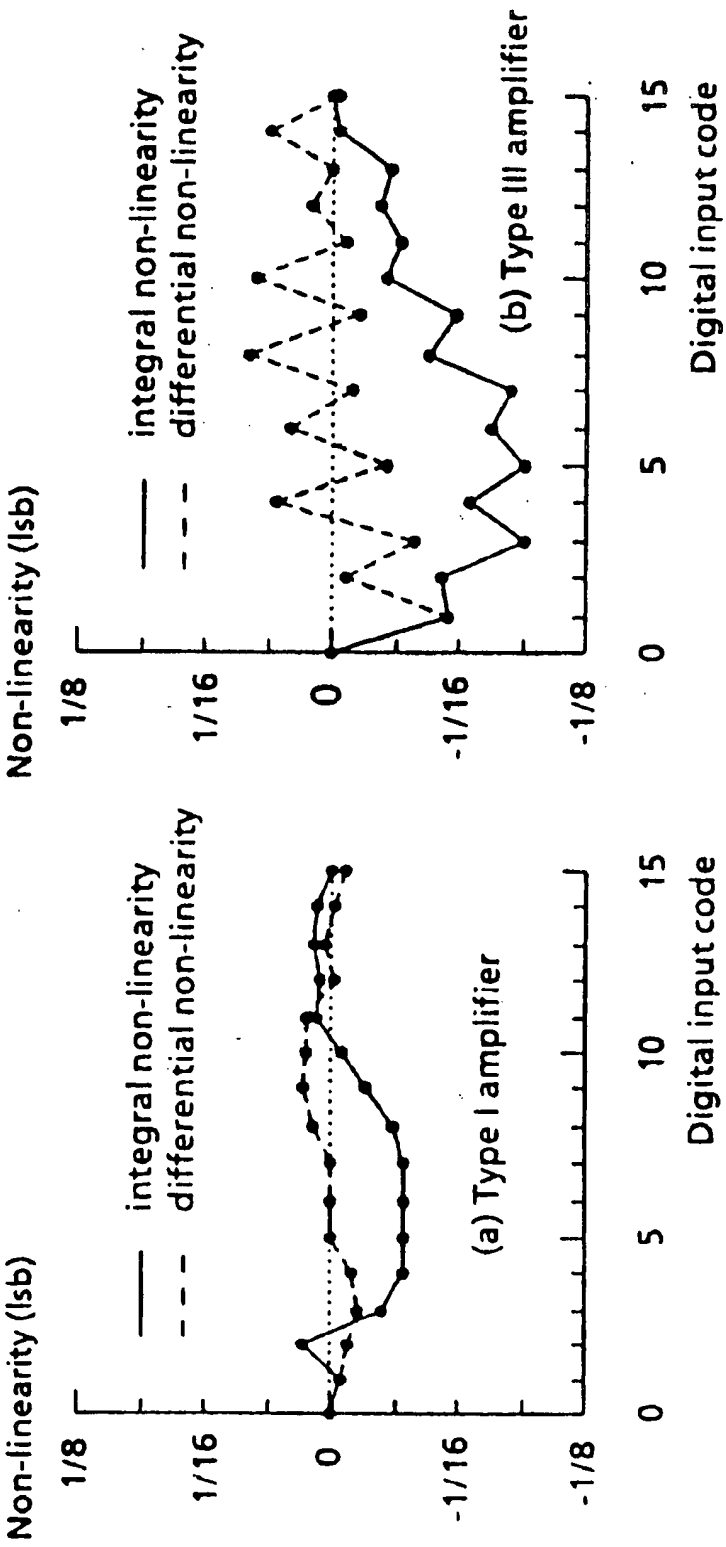


FIG. 13A

FIG. 13B

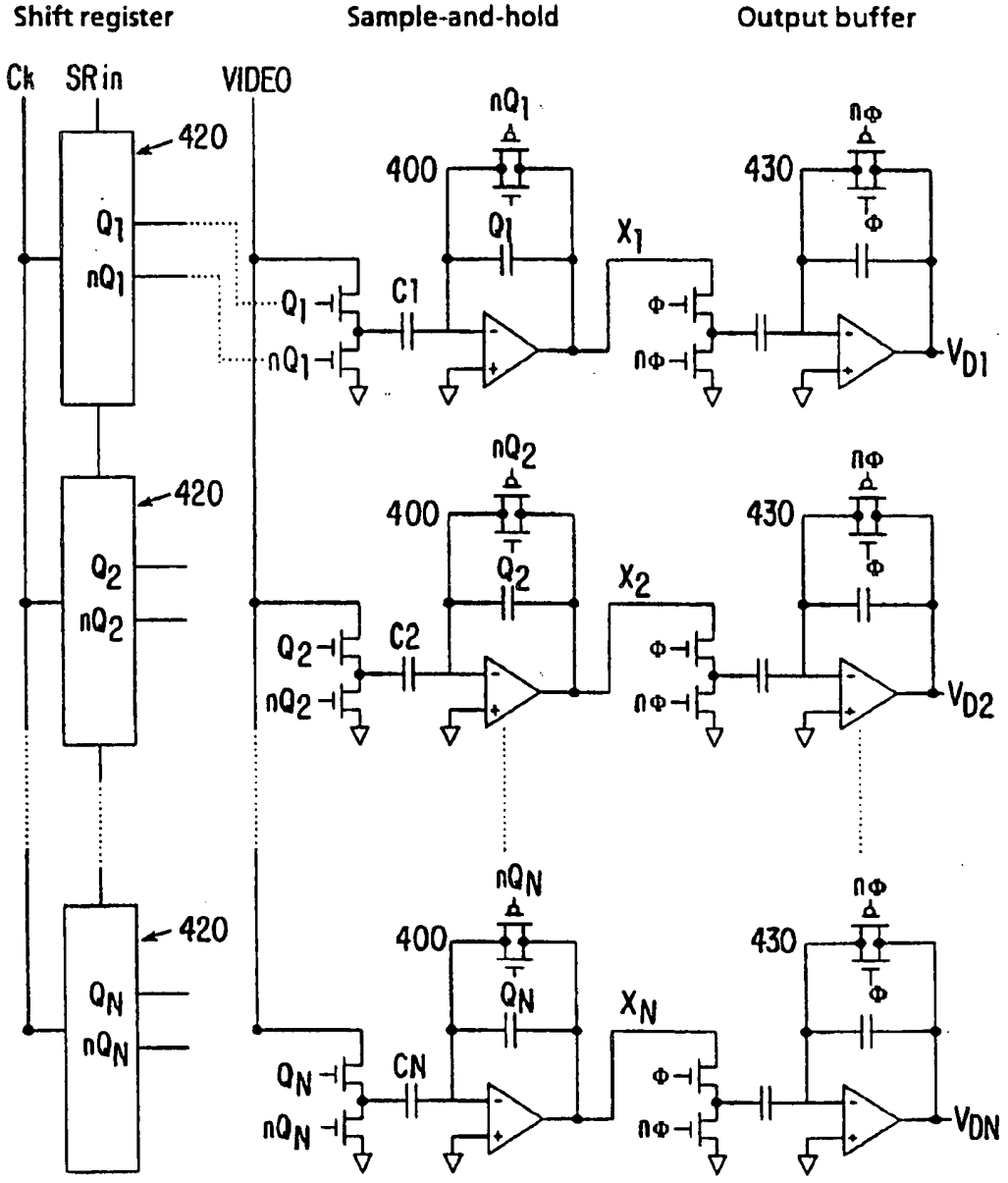

Shift register
Sample-and-hold
Output buffer
Ck
SRin
VIDEO
420
Q1
nQ1
Q2
nQ2
QN
nQN
400
430
C1
C2
CN
X1
X2
XN
nΦ
Φ
VD1
VD2
VDN

FIG. 14A

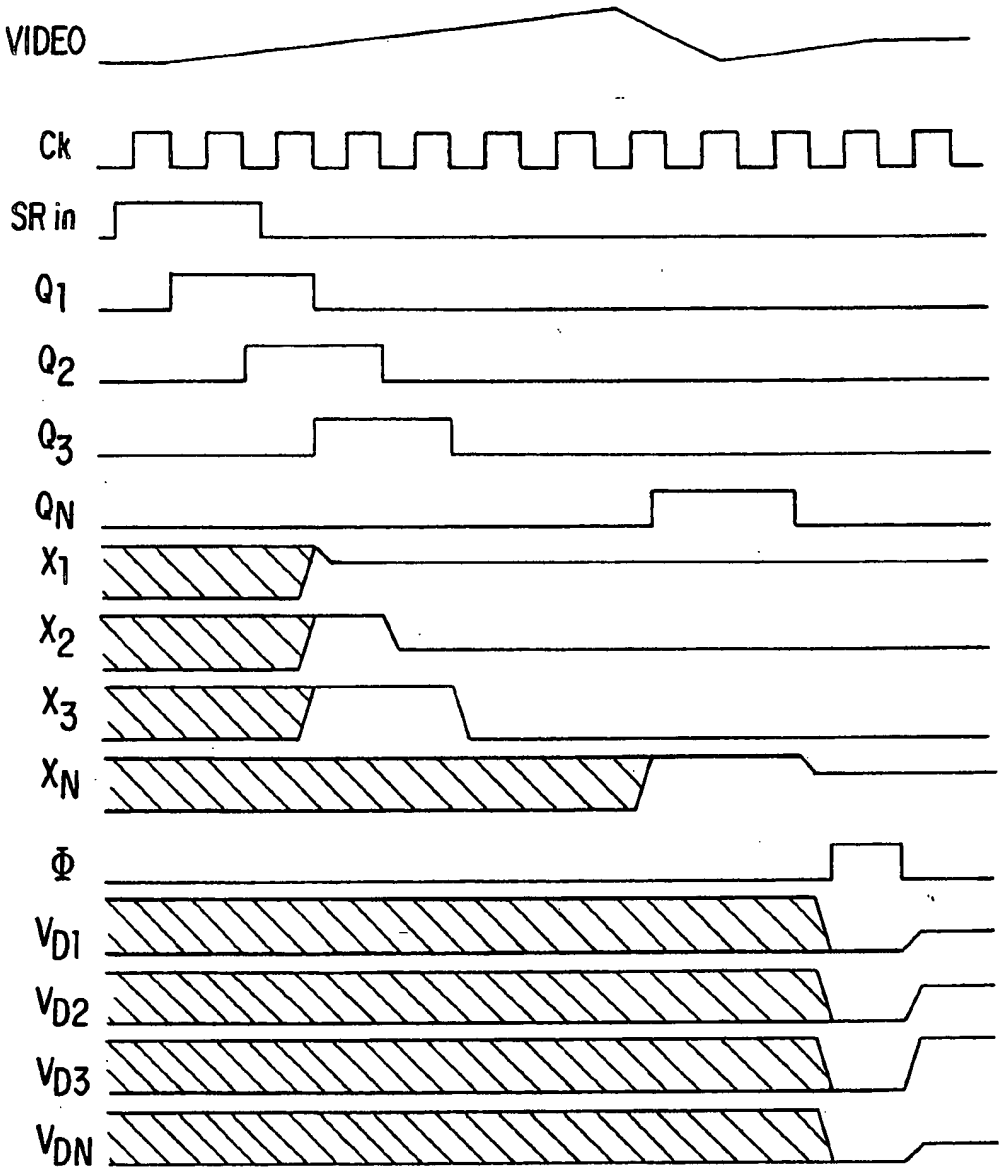


FIG. 14B

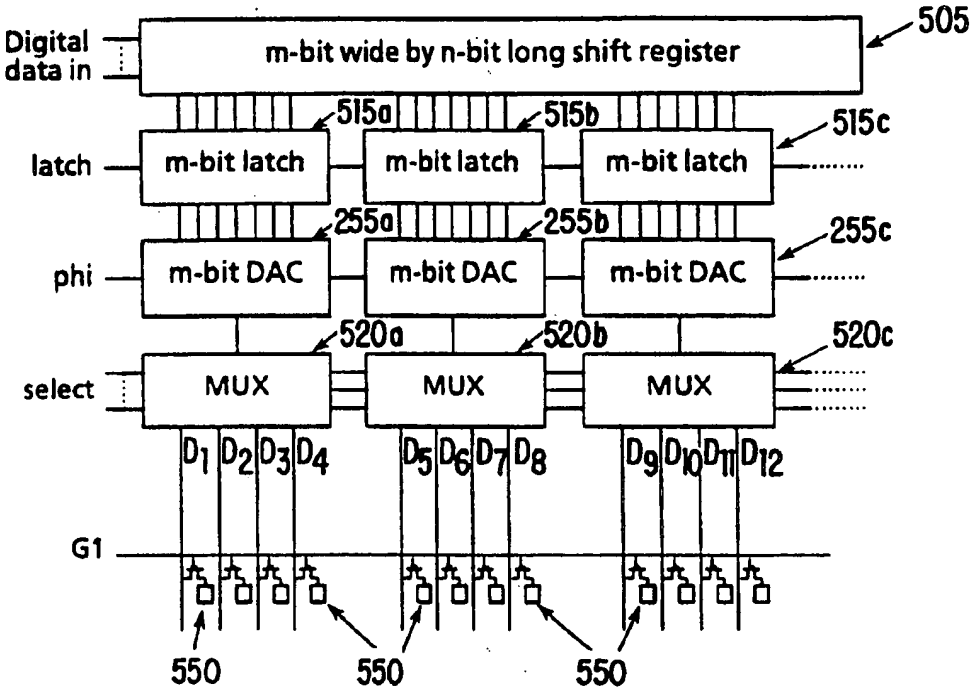


FIG. 15A

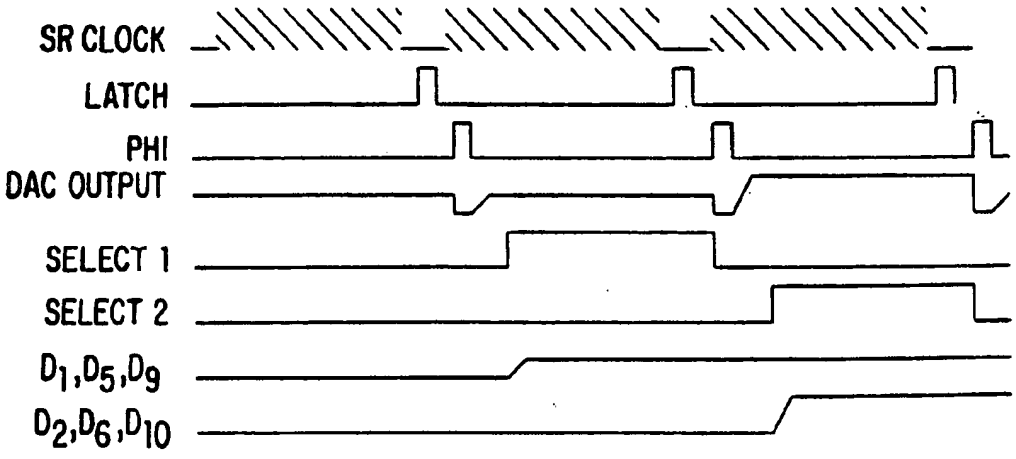


FIG. 15B

SWITCHED CAPACITOR ANALOG CIRCUITS USING POLYSILICON THIN FILM TECHNOLOGY

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention is directed to switched capacitor circuits formed from polysilicon thin film transistors (TFTs) and polysilicon thin film capacitors (TFCs), and in particular to switched capacitor analog circuits such as integrators, amplifiers, and digital-to-analog converters (DACs) using polysilicon TFTs and TFCs which can be used as analog driving circuitry for large area electronic (LAE) devices such as active-matrix liquid crystal displays, pagewidth optical scan arrays, or electrographic or ionographic printheads.

2. Background

Large area electronic devices usually consist of one- or two-dimensional arrays of thin-film circuit elements (often referred to as pixels). These pixels might contain, for example, liquid-crystal light valves for a display, or photodiodes for an optical scan array, or nibs for a print array. In each case the physical size of the array is determined by the application, and is much larger than a conventional silicon integrated circuit. The arrays are therefore built on large area substrates, usually of glass or quartz. The pixel arrays also require driving and interface circuitry, and in most cases this circuitry must be analog rather than digital, that is it must be capable of delivering or sensing a range of input signals. Suitable analog circuitry can be built using well-known switched capacitor techniques in conventional silicon integrated circuits (ICs). These ICs must then be mounted on or adjacent to the large area substrate containing the pixel array, and a large number of electrical connections must be made between the two. The cost of the peripheral drive and interface chips, their mounting and their electrical connection to the large area device can constitute a significant proportion of the overall cost of a system containing a large area device. If the ICs and connections can be eliminated or greatly reduced by integrating suitable circuitry on the large area substrate, then the system cost can be reduced and its reliability improved.

Thus, it is desirable to integrate drive circuitry with the pixel elements on a common substrate (e.g., glass or quartz). A number of circuits have been integrated with LAE displays using polysilicon and amorphous silicon thin film technologies. However, these have been purely digital circuits, or, where analog drive is needed, have used a simple pass transistor to deliver the analog signal to the array with the state of the pass transistor being controlled by digital circuitry.

It has been recognized that polysilicon thin film technology may enable the integration of drive circuitry on a substrate with a pixel array. However, due to the inferior performance of polysilicon thin film transistors (TFTs) when compared with conventional single crystal silicon MOS field effect transistors (MOSFETs), it has been thought that the fabrication of true analog circuits using polysilicon thin film technologies is not possible.

Polysilicon TFTs are inferior to conventional silicon MOSFETs in several ways. First, the electrical drive current available from a polysilicon TFT is much lower than that of a similar-sized MOSFET. This limitation also applies to digital circuits, but is more severe under the bias conditions typically employed in analog amplifiers. Second, the saturation characteristics of polysilicon TFTs are poor, with a low output impedance caused by the so-called "kink" effect which arises from channel avalanche multiplication and which is made worse by the presence of trap states in the device channel. This low output impedance is much more important for analog circuits than digital since it can limit the voltage gain available from an amplifier. Third, polysilicon TFTs are known to suffer from relatively high off-state leakage currents compared with MOSFETs. In analog applications, it is often necessary to store charge on a capacitor, and any charge lost due to TFT leakage will cause an error in the analog signal. Digital circuits, on the other hand, are much less susceptible to leakage; even in a dynamic design, where charge is also stored on a capacitive node, the total charge loss must exceed some threshold value before any signal error will arise, and this threshold is normally much larger than the acceptable charge loss in an analog circuit. Fourth, polysilicon TFTs exhibit much higher electrical noise then MOSFETs, a problem which is again much more important in analog applications than digital.

Single crystal thin-film technologies, also referred to as silicon-on-insulator technologies, such as silicon-on-saphire (SOS), separation by implanted oxygen (SIMOX) or zone-melt recrystallization (ZMR), also suffer some of the limitations discussed above, notably the kink effect (although it is not so severe in single crystal SOI MOSFETs as in polysilicon TFTs) and increased leakage. These technologies are not commonly used for analog applications, in part for these reasons.

A number of references recognize that it would be desirable to use TFTs to form integrated drivers for LAE devices such as liquid crystal displays. These references disclose polysilicon treatments which improve some of the characteristics of TFTs, however, even the improved polysilicon TFTs do not approach single crystal transistors in operating characteristics. Moreover, none of these references disclose switched capacitor analog circuits constructed using polysilicon thin film technology.

Alan G. Lewis and Richard Bruce, in "Circuit Design and Performance for Large Area Electronics", 1990 IEEE International Solid-State Circuits Conference, pp. 222–223, Feb. 16, 1990, discuss the use of polysilicon TFTs to form operational amplifiers (see FIG. 4). The use of cascodes (two or more transistors in series with separated gates) is disclosed in order to compensate for the kink effect in polysilicon TFTs. In spite of the low performance of polysilicon TFTs (low drive currents, higher threshold voltages), digital shift registers were fabricated which operate at high speeds (30 MHz). This is believed to be due to the low parasitic capacitance between the TFTs and the insulator substrate. Additionally, an operational amplifier constructed entirely from polysilicon TFTs is disclosed. This op-amp minimizes drain biases on the n-channel TFTs which are most susceptible to the degradation of output impedance due to the kink effect, and a complementary source-follower output stage is used to overcome the limited drive current. However, switched capacitor circuits were not demonstrated, and issues such as TFT leakage, compensation of the amplifier required for switched capacitor applications, and the linearity of thin film capacitors were not discussed.

S. N. Lee et al, in "A 5×9 inch Polysilicon Gray-Scale Color Head Down Display Chip", 1990 IEEE Solid-State Circuits Conference, pp. 220–221, Feb. 16, 1990, and R. G. Stewart et al in "A 9V Polysilicon LCD with Integrated Gray-Scale Drivers", pp. 319–322, SID 90 Digest, disclose a driver circuit for an LCD display which receives a digital input and an analog ramp-voltage input to produce an analog

09/22/2002, EAST Version: 1.03.0002

output to control the gray scale of the LCDs. All the polysilicon circuitry is digital; the bulk of it controls the time during which a pass transistor is held in the conducting state, and hence how much of the externally generated ramp is delivered to a given data line.

N. Yamauchi et al in "Drastically Improved Performance in Poly-Si TFTs With Channel Dimensions Comparable to Grain Size", IEDM, pp. 353–356, 1989, discloses processes for forming polysilicon TFTs which improve their field-effect mobility and current leakage.

D. M. Kim et al, in "Characterization and Modeling of Polysilicon TFTs and TFT-CMOS Circuits for Display and Integrated Driver Applications", SID Digest, pp. 304–306, 1990 disclose digital flip-flops, level shifter devices and buffer devices constructed from polysilicon TFTs.

K. Nakazawa et al in "Lightly Doped Drain TFT Structure for Poly-SiLCDs", SID Digest, pp. 311–314, 1990, discusses the promise of forming on-glass peripheral circuits made from polysilicon TFTs on full-color flat-panel liquid crystal displays. However, the low field-effect mobility and high current leakage are recognized as problems which still need to be overcome.

K. Ono et al in "Polysilicon TFTs With Low Gate Line Resistance and Low Off-State Current Suitable for Large Area and High Resolution LCDs", IEDM Digest, pp. 345–348, 1989, disclose polysilicon TFTs having lower gate line resistances and lower off-state currents by reacting Pt with gate polysilicon films.

Alan G. Lewis et al in "Physical Mechanisms for Short Channel Effects in Polysilicon Thin Film Transistors", IEDM Digest, 349–352, 1989, discuss the physical mechanisms responsible for short-channel threshold shifts in n- and p-channel polysilicon thin film transistors.

Japanese Patent Publication No. 59-182569 to Kumada discloses a thin film transistor having improved output characteristics by inactivating the surface of the thin film source and drain electrodes through heat treatment in a mixed gas containing hydrogen when the transistor is formed on an insulating substrate.

Wu et al in "Performance of Polysilicon TFT Digital Circuits Fabricated With Various Processing Techniques and Device Architectures", SID Digest, pp. 307–310, 1990, discuss fabrication processes for improving polysilicon TFTs, as well as digital driver circuits for LAE devices formed from these polysilicon TFTs.

Y. Matsueda et al in "New Technologies for Compact TFT LCDs With High-Aperture Ratio", SID Digest, pp. 315–318, 1990 disclose an LCD matrix wherein one storage capacitor line is provided for every two scanning lines.

Additional references which disclose TFTs used in digital circuits for LAE devices include U.S. Pat. No. 4,872,002 to Stewart et al, U.K. Patent Application No. 2,117,970 to Oshima et al, and Japanese Patent Publication No. 61-13665 to Hiranaka.

U.S. Pat. No. 4,872,002 to Stewart et al describes switched capacitor load circuits used in an integrated digital display driver. These load circuits are used to simulate a resistive load for TFT latches, and allow the gain of the latch to be modified. This load circuit does not include an amplifier, and is more simple than the circuits of the present invention, both in consisting of fewer elements, and in what it achieves. More complex circuits are not suggested. Stewart et al also note that their switched capacitor circuits deviate from ideal behavior (a feature of all switched capacitor circuits which limits their usefulness). It was expected that the analog circuits constructed according to the present invention would be fairly poor because of this characteristic of polysilicon switched capacitor circuits. However, surprisingly, they performed much better than expected.

U.K. Patent Application No. 2,117,270 to Oshima et al discloses digital circuits constructed from polysilicon TFTs.

The abstract "Charge-Sensitive Poly-Silicon Amplifiers For A-Si Pixel Particle Detectors", by Cho et al states that charge-sensitive poly-silicon TFT amplifiers have been made, but no details are given.

U.S. Pat. No. 4,783,146 to Stephany et al disclose TFTs used as switches in a liquid crystal print bar.

U.S. Pat. No. 4,772,099 to Kato et al discloses the use of polysilicon TFTs as switches in liquid crystal displays.

Additional background material relating to TFTs include "Depositing Active And Passive Thin-Film Elements On One Chip" by Harold Borkan, Electronics, Apr. 20, 1964 and "The TFT-A New Thin-Film Transistor" by Paul K. Weimer, Proceedings of the IRF, 1962.

The above references are incorporated herein by reference for purposes of background material regarding digital and analog driver circuitry.

While many of these references recognize the desirability of forming driver or interface circuitry from polysilicon TFTs because such circuitry can be integrated on the large area substrates which currently contain the arrays of LC light valves, photodiodes or print nibs, none of these references disclose the present invention. Many of the references seek to improve the performance of polysilicon so that TFTs function more like single crystal devices. Other references form digital circuits from polysilicon TFTs. However, none of the references disclose true analog circuits made from polysilicon, and in fact, the skilled artisan would not expect such circuits to achieve useful performance due to the limited performance of polysilicon TFTs discussed above.

OBJECTS AND SUMMARY OF THE INVENTION

It is an object of the present invention to provide analog switched capacitor circuits which can be fabricated on large area insulating substrates, such as quartz or glass, from polysilicon.

It is another object of the present invention to fabricate analog switched capacitor drive and interface circuits suitable for integration with other circuit elements in large area electronic devices.

To achieve the foregoing and other objects, and to overcome the shortcomings discussed above, switched capacitor circuits are fabricated using polysilicon TFTs and TFCs. While switched capacitor circuits, as well as TFTs and TFCs are well known, it was not previously believed that TFTs and TFCs could be used to fabricate analog switched capacitor circuits due to the poor performance of polysilicon TFTs (versus single crystal silicon MOSFETs). However, surprisingly, it has been found that analog switched capacitor circuits fabricated using TFTs and TFCs are accurate enough for use as analog control circuitry in LAE devices. Moreover, since TFTs and TFCs can be formed on glass substrates, they can be integrated with the pixel elements (which are already being formed on the substrates using thin film technology). Accordingly, LAEs can be fabricated having a reduced number of, or no, peripheral driver chips, reducing chip-to-substrate connections, so as to reduce overall cost and improve reliability.

Switched capacitor amplifiers, charge redistribution digital-to-analog converters, and sampling amplifiers are disclosed, and have been built, which exhibit performance characteristics suitable for driving LAE devices such as LCDs, pagewidth image sensors, and pagewidth electrographic or ionographic printheads.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements and wherein:

FIG. **1** is a cross section of n- and p-channel polysilicon TFTs and a polysilicon TFC formed on a common insulator substrate;

FIGS. **2A** and **2B** show typical characteristics for n- and p-type polysilicon TFTs and illustrate the low current drives, high threshold voltages and kink effect;

FIGS. **3A–3C** are three polysilicon TFT operational amplifiers used to form switched capacitor circuits;

FIG. **4** shows the frequency response for the FIG. **3A–C** operational amplifiers;

FIG. **5** is one embodiment of a switched capacitor amplifier constructed from polysilicon TFTs and TFCs;

FIG. **6** shows waveforms produced by a switched capacitor amplifier constructed from the FIG. **3A** op amp;

FIG. **7** shows waveforms produced by a switched capacitor amplifier constructed from the FIG. **3C** op amp;

FIG. **8** shows waveforms produced by a switched capacitor amplifier constructed from the FIG. **3A** op amp driven at a clock frequency of 50 kHz with a 1 kHz triangular wave input;

FIG. **9** shows a waveform produced by a switched capacitor amplifier constructed from the FIG. 3C op amp driven at a clock frequency of 20 kHz with a triangular wave input similar to that in FIG. **8**;

FIG. **10** is one embodiment of a charge redistribution digital-to-analog converter constructed from polysilicon TFTs and TFCs;

FIG. **11** is a waveform produced by the FIG. **10** charge redistribution digital-to-analog converter;

FIG. **12** shows the response for DACs constructed from the type I and type III amplifiers;

FIGS. **13A** and **13B** show the converter error for DACs constructed from the type land type III amplifiers, respectively;

FIG. **14A** illustrates a video signal sample-and-hold circuit (sampling amplifier) for display driving;

FIG. **14B** shows the timing for the video signal sampling amplifier circuit of FIG. **14A**; and

FIGS. **15A** and **15B** show a digital-to-analog converter display driver, and timing signals therefore.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is particularly applicable to forming analog interface and driving circuitry for LAE devices which can be integrated on the same substrate as the circuit elements with which they are associated. For example, the analog switched capacitor circuits of the present invention can be used to form data drivers, including sampling amplifiers and digital-to-analog converters for active matrix LCDs (AMLCDS).

While some specific circuits constructed from polysilicon TFTs and TFCs are shown, these circuits are merely illustrative. The present invention involves the discovery that analog switched capacitor circuits made from polysilicon can be constructed which have operating characteristics appropriate for use as data drivers and interface circuits for LAE devices.

As described above, polysilicon TFTs are commonly used to form switches and digital circuits integrally on a substrate with LCDs. See the above incorporated U.S. Pat. Nos. 4,872,002, 4,772,099, and 4,783,146. Polysilicon thin film technology is also well suited for the integration of capacitors. FIG. **1** shows cross sections of n- and p-channel TFTs **110**, **120**, respectively, and a capacitor **130** built on the same insulating quartz or glass substrate **100**. Each TFT includes active polysilicon islands **112** and **122**, a gate oxide layer **114**, **124**, and a polysilicon gate **116**, **126**. The capacitor requires only one additional implant to make a conducting bottom plate **132** out of the active device island, and uses the TFT gate dielectric **134**. In layout, the capacitor is similar to a polysilicon to diffusion capacitor in a conventional MOS analog process. However, in a thin film technology, this structure has the important advantage of negligible parasitic capacitance associated with either plate due to its formation on insulating substrate **100**.

FIG. **2** shows typical characteristics for n- and p-channel TFTs, each having a width (W) of 50 μm and a length (L) of 10 μm. Drain current is shown as a function of drain-source bias for various values of gate-source bias. The drive currents are about an order of magnitude lower than for single crystal devices, as noted above, and the threshold voltages are higher. The saturation characteristics also display the kink effect described above. The low drive current and poor saturation characteristics both suggest that these devices are not suitable for analog circuit design, as discussed above.

FIGS. **3A–C** show schematics for three operational amplifiers which were formed entirely using polysilicon thin film technology. The circuits have all been fabricated using polysilicon thin-film transistors and employ design rules compatible with large area processing on 32 cm×34 cm plates (i.e., minimum feature size is 10 μm). The simple amplifier (type I in FIG. **3A**) uses cascodes to overcome the poor output impedance of the TFTs in saturation due to the kink effect. See, for example, the above-incorporated paper by Lewis and Bruce entitled "Circuit Design and Performance for Large Area Electronics", 1990 IEEE International Solid-State Circuits Conference, pp. 222–223 (Feb. 16, 1990). This circuit used the minimum number of TFTs, and is important since in most applications the area available for the circuits is limited. The type II (FIG. **3B**) circuit provides a differential input and retains the cascode. The type III circuit (FIG. **3C**) uses two stages for increased gain and a complementary source follower output stage for increased drive; it does, however, require compensation (by capacitor C_{COMP}) to ensure stability.

FIG. **4** shows the frequency response of each amplifier when driving a 30 pF load capacitance. Amplifier gain (dB) is shown as a function of frequency. Each TFT had geometric characteristics of L=10 μm and W=200 μm, (except * in the Type II and Type III amplifiers, for which W=400 μm). V_{DD}=20V, and the bias current was 100 nA/μm width. The high low-frequency gain of the two stage design is clear, along with its improved bandwidth.

FIG. **5** shows the schematic of a switched capacitor amplifier **200** fabricated using the thin film polysilicon technology. The switched capacitor circuits of the present

invention are standard circuits, although they have not been implemented previously in polysilicon thin film technology. For a general understanding of switched capacitor circuits, see Bipolar and MOS Analog Integrated Circuit Design, by Alan B. Grebene, John Wiley & Sons, pages 703–711, the disclosure of which is incorporated herein by reference.

Although the switched capacitor amplifier **200** of FIG. **5** is of straightforward design, a brief description is provided. The switched capacitor amplifier functions to provide an output voltage V_{OUT} at terminal **250** which is proportional to the input voltage V_{IN} supplied to terminal **205**. The gain is controlled by the ratio of the capacitances of input capacitor **225** and feedback capacitor **230**. In one example, the capacitance of capacitor **225** was 35 pF, while feedback capacitor **230** had a capacitance value of 3.5 pF. Digital clock signals ϕ and $n\phi$ ($n\phi$ being the inverse of ϕ), are applied to transistor switches **210, 220, 235** and **240** so that the output of circuit **200** is set by the transfer and distribution of charge among input capacitor **225** and feedback capacitor **230** under the control of the transistor switches. Transistor **235** is a p-channel TFT and conducts when a low clock signal is applied to its gate, while transistors **210, 220** and **240** are n-channel TFTs and conduct when a high clock signal is applied to their gates.

In order to understand the operation of this circuit, suppose first that clock signal ϕ is high (and $n\phi$ low). This is the reset condition; TFTs **235** and **240** are both conducting so that feedback capacitor **230** is discharged and the output node **250** is at ground (0v). At the same time, TFT **210** is conducting and TFT **220** is non-conducting, so the left hand plate of the input capacitor **225** is at the potential of the input node **205**, V_{IN}, which is assumed to be positive here. The right hand plate of capacitor 225 is connected to the operational amplifier **245** inverting input which acts as a virtual ground and so is at 0v. Thus, the input capacitor **225** has a voltage equal to the input voltage V_{IN} across it. The amplification phase of the cycle is initiated when ϕ goes low (and $n\phi$ goes high). The reset TFTs **235** and **240** then become non-conducting, and the feedback capacitor **230** is free to become charged. At the same time, TFT **210** becomes nonconducting, isolating the left hand plate of input capacitor **225** from the input node **205**, and TFT **220** becomes conducting, connecting the left hand plate of input capacitor **225** to ground. The inverting input of the operational amplifier **245** is thus driven towards a negative voltage, causing the output node **250** to swing to a positive voltage. Current flows via the feedback capacitor **230** to the operational amplifier inverting input, and this current discharges input capacitor **225**. The result is a transfer of electrical charge from the input capacitor **225** to the feedback capacitor **230**. This continues until only a small residual charge is left on the input capacitor **225** and the feedback capacitor **230** holds almost all the charge originally present on the input capacitor. The output voltage present at node **250** is then given by:

$$V_{OUT} = V_{IN} \cdot \frac{C_{IN}}{C_{FB}} \cdot \left(\frac{A}{1+A} \right)$$

where V_{OUT} is the final voltage at node **250**, V_{IN} is the voltage at node **205** at the time when ϕ goes low, C_{IN} is the capacitance of the input capacitor **225**, C_{FB} is the capacitance of the feedback capacitor **230**, and A is the voltage gain of the operational amplifier 245. Normally the amplifier gain A is very high, so the output voltage is close to being the input voltage scaled by the ratio of the input and feedback capacitors.

Once the output voltage has settled and been used (for example by being transferred from a data line into the selected pixel in an active matrix liquid crystal display), the clock signal ϕ goes high again (and $n\phi$ low), resetting the amplifier ready to sample the next input voltage.

FIGS. **6** and **7** show clock (ϕ) (upper trace) and output (lower trace) waveforms for the switched capacitor amplifier of FIG. **5** implemented with type I and type III operational amplifiers respectively. The two phases of reset (with the clock signal high) and amplification (with the clock signal low) can be seen. In FIG. **6** output waveforms are shown for fixed input voltages of 1.5 and 0v, while in FIG. **7** the input voltages are +0.5v and −0.5v. The load capacitance was 30 pF for the circuit using a type I operational amplifier (FIG. **3***a*), but with the type III amplifier (FIG. **3***c*) a much higher load capacitance of 250 pF could be used without degrading the output settling too severely. This emphasizes the higher drive available from the type III operational amplifier. In both the circuits used to obtain FIGS. **6** and **7**, the TFT lengths were all 10 μm, and the bias current was 100 nA/pm width for the amplifier TFTs, and both the supply voltage and clock pulse peak-peak amplitude were 20v.

The line time available for a conventional TV resolution active matrix liquid crystal display is about 60μs. FIGS. **6** and **7** show that the switched capacitor amplifiers are able to settle with cycle times well below this, even with large capacitive loads. The output swings are also suitable for liquid crystal displays. Thus an array of such amplifiers could be used to provide the parallel drive needed for the data lines of an active matrix display.

FIGS. **8** and **9** show the response of the amplifiers to 1 kHz triangle wave inputs. The top trace is of the input signal, while the lower trace is of the output. The clock frequency used with the type I circuit was 50 kHz, while a clock frequency of 20 kHz was used for the type III circuit. Good linearity and the absence of clipping can be seen.

It should also be noted that a switched capacitor integrator is provided by op amp **245**, capacitor **230** and reset TFTs **235** and **240** of the FIG. **5** circuit. The output of the switched capacitor integrator is set by the accummulation of charge on capacitor **230** under the control of transistors **235** and **240**, and op amp **245**.

Another useful but more complex circuit for AMLCD data driving or other LAE applications is an on-glass digital-to-analog converter. The present invention permits the construction of all thin-film charge redistribution DACs. The basic circuit of a demonstration charge redistribution DAC **255** is shown in FIG. **10**, and again circuits using the different amplifiers shown in FIGS. 3A–C have been fabricated. The DAC of FIG. **10** receives 4 bits of input data to produce a variable output voltage based on the input. Operation of the DAC is somewhat similar to the operation of the switched capacitor amplifier discussed above. However, instead of a single input capacitor, a plurality of input capacitors are used.

During the reset phase, the clock signal ϕ is high and the feedback capacitor **230** is discharged. The right hand plates of the input capacitors **225***a–d* are all held at virtual ground, but the left hand plates are either held at the reference voltage V_{REF} or at ground depending on the state of the corresponding input bit. If the input bit is 1 (high) then the appropriate circuit **260***a–d* connects the left hand plate to V_{REF} and the input capacitor is charged to V_{REF}, but if the input bit is 0 (low) then the left hand plate is held at ground and the input capacitor remains uncharged. During the amplification phase, when the clock signal ϕ is low, the charge is transferred from the input capacitors **225***a–d* to the feedback capacitor **230** as discussed above for the simple switched capacitor amplifier. The total charge transferred to

feedback capacitor **230** thus depends on the sizes of the input capacitors **225***a–d* and the digital input word. In order to obtain the correct DAC operation, the input capacitors must ascend in binary sequence; in this example, **225***a*=C_O, **225***b*=2C_O, **225***c*=4C_O, **225***d*=8C_O and the feedback capacitor **230**=16C_O, where C_O is 1 pF. (In practice, the capacitors are made up of parallel combinations of either 1, 2, 4, 8 or 16 identical unit capacitors respectively in order to eliminate errors due to edge effects, process variation and so on).

FIG. **11** shows the clock (upper trace) and output (lower trace) waveforms for the DAC of FIG. **10** fabricated using the type I operational amplifier (FIG. 3*a*). In this example, the circuit is operating at 50 kHz conversion rate, although the settling time is short enough to allow faster operation. Other circuit parameters are the same as for the circuits tested in FIGS. **6** and **7**. Output signals are shown for input codes of 0000 and 1111; any binary input between these values produces an intermediate output.

FIG. **12** shows the output voltage just before reset as a function of the digital input code for DACs built using the type I (FIG. 3*a*) and type III (FIG. 3*c*) operational amplifiers. FIGS. **13***a* and **13***b* show the differential and integral nonlinearity obtained from the curves shown in FIG. **12**. Although 4-bit DACs were built for demonstration purposes, their precision is better than ½16th lsb, that is the circuit accuracy obtained with this example configuration is adequate for an 8-bit DAC.

The input switching circuits **260***a–d* are shown for the sake of example. Other circuits for achieving the same function will be apparent to those skilled in the art.

In view of the poor performance of polysilicon TFTs in comparison with conventional MOSFETs normally used to implement switched capacitor circuits, and particularly since their performance limitations (low drive, poor saturation, leakage and noise) are likely to have a greater impact on analog circuits than digital as discussed above, it is surprising that switched capacitor circuits with the useful levels of performance described above can be built using these devices.

Switched capacitor circuits built entirely using polysilicon thin film devices on quartz substrates have been demonstrated for the first time according to the present invention. Charge redistribution amplifiers and digital-to-analog converters are shown to operate at clock rates of above 50 kHz despite the relatively poor performance of polysilicon TFTs in comparison to conventional MOSFETs. Better than 8-bit accuracy is demonstrated for the DACs. These results offer the possibility of greatly increased functionality on large area devices such as flat-panel displays, pagewidth scan arrays or pagewidth printheads.

One way in which this can be achieved is illustrated in FIG. **14A**. This shows an array of video sampling amplifiers which might be used to drive the data lines of an AMLCD. Circuits such as this are currently implemented using single crystal technologies, but have not been reported in polysilicon thin film technology. The circuit uses two sampling amplifiers similar to the circuit shown in FIG. **5** for every output. The first amplifier, **400**, samples the input video signal and is controlled by a conventional prior art polysilicon TFT shift register **420**. When the output Q_i of the ith shift register stage goes high (and its complement,nQ_i low), the corresponding switched capacitor amplifier is reset and its input capacitor is charged to the voltage present on the analog video input line. When Q_i goes low again, the voltage present on the video line is amplified and becomes available at the amplifier output. Thus, by passing a single '1' through the shift register during one display line time, the serial video input is converted, by the end of that line time, to N separate voltages at the outputs of the amplifiers **400**, where each voltage corresponds to the data for the pixel at one location across the display line. Before the next line begins, all N voltages are sampled and amplified by the second set of switched capacitor amplifiers **430** under the control of the clock signal ϕ and its complement $n\phi$, and become available at the outputs V_{D1}–V_{DN}, where they remain while the analog data for the subsequent line is being sampled by the first amplifiers **400**.

The timing and control signals for the circuit shown in FIG. **14A** are shown in FIG. **14B**. In this case, a double '1' is passed through the shift register so that two outputs (Q_1 and Q_2, Q_2 and Q_3, Q_3 and Q_4 etc) are high simultaneously. This arrangement allows a longer time for the input capacitor of the first stage amplifiers **400** to charge to the video input signal.

The circuit shown in FIG. **14A** and the timing scheme of FIG. **14B** are for illustration only. Variations on the basic architecture which would achieve the same functionality will be apparent to persons skilled in the art.

FIG. **15A** shows a possible display driver architecture using DACs **255***a–c*, which could again be implemented entirely in polysilicon TFTs and TFCs. FIG. **15B** shows a timing diagram for the FIG. **15A** architecture. The input data is now digital reducing still further the amount of external processing (since in many applications the image source is digital). The data for a complete line is loaded serially into a shift register **505**, and then transferred in parallel into a set of digital latches **515***a–c*. These drive the charge redistribution DACs **255***a–c*, which are controlled by a single clock, phi (and its complement) as indicated in FIG. **10**. Thus all the serial input digital data is converted to analog form and made available simultaneously at the DAC outputs.

FIG. **15A** also shows multiplexers at the output of each DAC. Since the DACs themselves are large, there may not be room to have one for each data line. The multiplexers allow each DAC to serve several lines (four in this example) by switching the DAC output between the data lines so that each is charged to the required voltage in turn. Such a scheme does, however, mean that the DAC conversion time must be smaller. The charge on each data line is then received by a corresponding liquid crystal light shutter **250** when a gate of a switch TFT associated therewith is switched on. The basic AMLCD actuation scheme is conventional. See, for example, the above-incorporated U.S. Pat. No. 4,872,002 to Stewart et al.

The arrangement of FIGS. **15A–B** could also be used to control the LCDs in a printing bar as disclosed in the above incorporated U.S. Pat. No. 4,783,146 to Stephany et al. Alternatively, analog driver circuitry according to the present invention could be used to control electrographic or ionographic printing devices.

The polysilicon TFTs and TFCs can be formed on quartz or glass substrates using previously reported techniques (for example in the above incorporated paper by Wu et al entitled "Performance of Polysilicon TFT Digital Circuits Fabricated with Various Processing Techniques and Device Architectures", SID 90 Digest, pp. 307–310). The circuits described and tested herein were constructed on quartz substrates as follows. An active silicon layer was deposited and implanted with silicon to retard grain growth, resulting in a large grain size following the 600° C. crystallization anneal (see Wu et al, J. Appl. Phys., 65, pp. 4036–9 (1989)). Following island definition, the gate dielectric was formed by deposition of an LPCVD SiO_2 film and a 950° C. anneal in oxygen, resulting

in a final gate oxide thickness of 100 nm. The gate material was a 350 nm thick LPCVD polysilicon film, doped by phosphorus ion implantation. The self-aligned source and drain regions were formed by boron and phosphorus ion implantation for the p-and n-channel devices respectively.

The process used to build the TFTs and TFCs required for the switched capacitor circuits described above is the same as that used to build the pixel TFTs and storage capacitors of and active matrix display. Thus no additional process steps are required to integrate the switched capacitor circuits with an AMLCD. All the circuits described were fabricated on quartz substrates using a maximum processing temperature well above the melting point of glass. Processes suitable for building TFTs on glass substrates are also well known, however, and could be used to fabricate switched capacitor circuits in the same way. The circuits could also be built in material on the periphery of an amorphous silicon TFT AMLCD which has been locally recrystallized by, for example, laser annealing.

While this invention has been described in conjunction with specific embodiments thereof, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. For example, analog-to-digital converters and switched capacitor filters can also be fabricated. Accordingly, the preferred embodiments of the invention as set forth herein are intended to be illustrative, not limiting. Various changes may be made without departing from the spirit and scope of the invention as defined in the following claims.

What is claimed is:

1. An analog switched capacitor circuit comprising:

at least one polysilicon thin film capacitor means;

at least one polysilicon thin film transistor switch means;

at least one polysilicon thin film amplifier means; and

interconnection means for interconnecting the capacitor means, the transistor switch means, and the amplifier means so that the output of said circuit is set by the accumulation of electrical charge on said capacitor means under the control of said transistor switch means and said amplifier means;

said capacitor means, said transistor switch means, said amplifier means, and said interconnection means all being formed on a common substrate.

2. The analog circuit of claim 1, wherein at least two said capacitor means are provided, and interconnected to said transistor switch means and said amplifier means by said interconnection means so that the output of said circuit is set by the accumulation and redistribution of charge among said capacitor means under the control of said transistor switch means and said amplifier means.

3. The analog circuit of claim 2, wherein an array of circuit elements driven by said analog circuit is integrally formed on said substrate.

4. The analog circuit of claim 3, wherein said array of circuit elements is a matrix of display devices, each of said display devices having a data line; and said analog circuit comprises:

a plurality of analog switched capacitor subcircuits having at least one of said capacitor means, at least one of said transistor means, and at least one of said amplifier means, all being formed on said substrate, each of said subcircuits being operatively coupled to at least one of said data lines; and the transistor switch means for each of said subcircuits being separately controlled.

5. The circuit of claim 4, wherein each of said subcircuits is operatively coupled to a plurality of data lines, and said analog circuit further comprises multiplexing means connected between each of said subcircuits and its corresponding data lines, for selectively connecting each subcircuit to its corresponding data lines.

6. The analog circuit of claim 3, wherein said array of circuit elements comprises a plurality of switch controlled display elements connected to respective data lines, and said analog switched capacitor circuit is operatively coupled to at least one of said data lines.

7. The analog circuit of claim 6, wherein said analog circuit comprises a plurality of separate control circuits having at least one polysilicon thin film capacitor means, at least one polysilicon thin film transistor switch means, and at least one polysilicon thin film amplifier means electrically connected with at least one of said data lines, said transistor switch means of each of said separate control circuits being controlled by a separate control signal.

8. The analog circuit of claim 7, wherein each of said separate control circuits is operatively coupled to a plurality of different data lines, and said analog circuit further comprises multiplexing means connected between each of said control circuits and its corresponding data lines, for selectively connecting each control circuit to its corresponding data lines.

9. The analog circuit of claim 7, wherein each of said separate control circuits comprises a digital-to-analog converter.

10. The analog circuit of claim 7, wherein each of said separate control circuits comprises sample-and-hold means.

11. The analog circuit of claim 2, wherein said capacitor means, said transistor switch means, and said amplifier means are configured as a digital-to-analog converter.

12. The analog circuit of claim 2, wherein said capacitor means, said transistor switch means, and said amplifier means are configured as a sampling amplifier means.

13. The analog circuit of claim 3, wherein said circuit elements are printing elements.

14. An analog switched capacitor circuit comprising:

an amplifier constructed from polysilicon thin film transistors and having an input and an output;

a polysilicon thin film input capacitor having an output attached to said amplifier input;

a first polysilicon thin film transistor attached to an input of said input capacitor, for selectively attaching said input capacitor to an input voltage source based upon a first control signal;

a second polysilicon thin film transistor attached to said input of said input capacitor, for selectively attaching said input capacitor to ground based upon a second control signal;

a polysilicon thin film feedback capacitor attached between said output and said input of said amplifier;

a third thin film polysilicon transistor attached between said output and said input of said amplifier, for selectively discharging said feedback capacitor based upon one of said first and second control signals;

wherein a capacitance of said input and said feedback capacitors is chosen, and said first, second and third transistors are controlled so that the output of said circuit is set by the transfer and distribution of charge among said input and feedback capacitors under the control of said first, second and third transistors; and

said amplifier, said input and feedback capacitors, and said first, second and third transistors all being formed on a common substrate.

15. The analog circuit of claim 14, further comprising:

a fourth polysilicon thin film transistor attached between said input and said output of said amplifier, for selectively discharging said feedback capacitor in conjunction with said third transistor, based on an opposite one of said first and second control signals.

16. The analog circuit of claim **15**, wherein said amplifier includes a plurality of transistors having gates attached to different voltage sources.

17. The analog circuit of claim **15**, wherein said amplifier is a two stage amplifier including a compensating polysilicon thin film capacitor.

18. The analog circuit of claim **15**, further comprising:

a plurality of said input capacitors, each having a different capacitance and a respective first and second thin film transistor, each of said first transistors being attachable to a common reference voltage source and being controlled by a different bit of a multi-bit digital input, so that each respective input capacitor is charged by the reference voltage based on its bit input, whereby said analog circuit is a digital-to-analog converter.

19. The analog circuit of claim **14**, wherein an array of circuit elements driven by said analog circuit is integrally formed on said substrate.

20. The analog circuit of claim **14**, wherein said array of circuit elements comprises a plurality of switch controlled display elements connected to respective data lines, and said analog switched capacitor circuit is operatively coupled to at least one of said data lines.

21. A method of fabricating an analog switched capacitor circuit comprising:

a) forming at least one polysilicon thin film capacitor means on a substrate;

b) forming at least one polysilicon thin film transistor switch means on said substrate;

c) forming at least one polysilicon thin film amplifier means on said substrate; and

d) forming polysilicon thin film interconnection means on said substrate, said interconnection means for interconnecting said capacitor means, said transistor switch means, and said amplifier means so that the output of said circuit is set by the accumulation of charge on said at least one capacitor means under the control of said transistor switch means, wherein said capacitor means, said transistor switch means, and said amplifier means are formed during the same polysilicon deposition process.

22. The method of claim **21**, wherein at least two said polysilicon thin film capacitor means are formed on said substrate, and are interconnected to said transistor switch means and said amplifier means by said interconnection means so that the output of said circuit is set by the transfer and distribution of charge among said capacitor means under the control of said transistor switch means and said amplifier means.

23. The method of claim **22**, further comprising:

forming at least one polysilicon circuit element on said substrate during said deposition process, said circuit element being operatively attached to said analog switched capacitor circuit.

24. The method of claim **23**, wherein said at least one circuit element is a liquid crystal display element.

25. The method of claim **23**, wherein said circuit element is a printing element.

26. The method of claim **22**, wherein said analog circuit is configured as a digital-to-analog converter.

27. The method of claim **22**, wherein said analog circuit is configured as a sampling amplifier.

* * * * *

US006380920B1

(12) **United States Patent**
Ozawa

(10) **Patent No.: US 6,380,920 B1**
(45) **Date of Patent: Apr. 30, 2002**

(54) **ELECTRO-OPTICAL DEVICE DRIVE CIRCUIT, ELECTRO-OPTICAL DEVICE AND ELECTRONIC EQUIPMENT USING THE SAME**

(75) Inventor: **Tokuro Ozawa**, Suwa (JP)

(73) Assignee: **Seiko Epson Corporation**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/419,971**

(22) Filed: **Oct. 18, 1999**

(30) **Foreign Application Priority Data**

Oct. 16, 1998 (JP) 10-295658

(51) **Int. Cl.**[7] **G09G 3/36**
(52) **U.S. Cl.** **345/100**; 345/98; 345/559
(58) **Field of Search** 345/87–89, 98–100, 345/96, 209, 204, 55, 559

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,170,158 A 12/1992 Shinya 345/98
6,046,719 A * 4/2000 Dengwau 345/100
6,049,321 A * 12/2000 Sasake 345/99
6,157,360 A * 12/2000 Jeong et al. 345/98
6,160,532 A * 12/2000 Kaburage et al. 345/87

OTHER PUBLICATIONS

Mosley, Alan "The structure, performance and future of passive matrix LCDs" John Wiley & Sons pp. 173–176, 1997.*

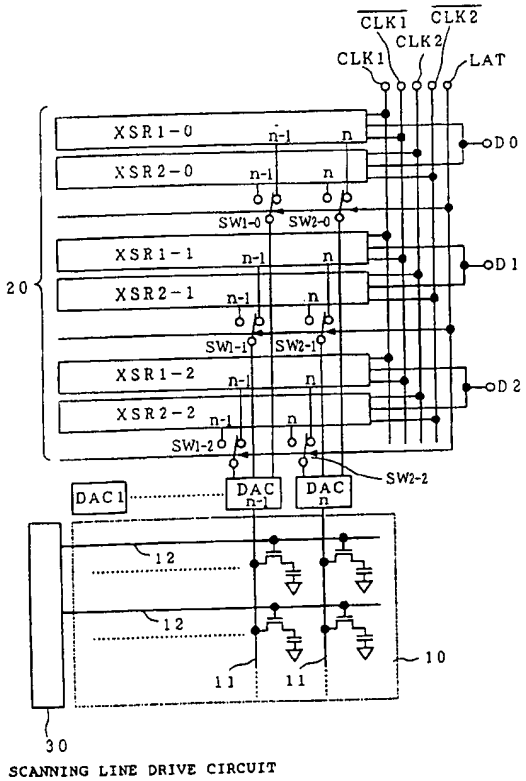
* cited by examiner

Primary Examiner—Richard Hjerpe
Assistant Examiner—Frances Nguyen
(74) *Attorney, Agent, or Firm*—Oliff & Berridge, PLC

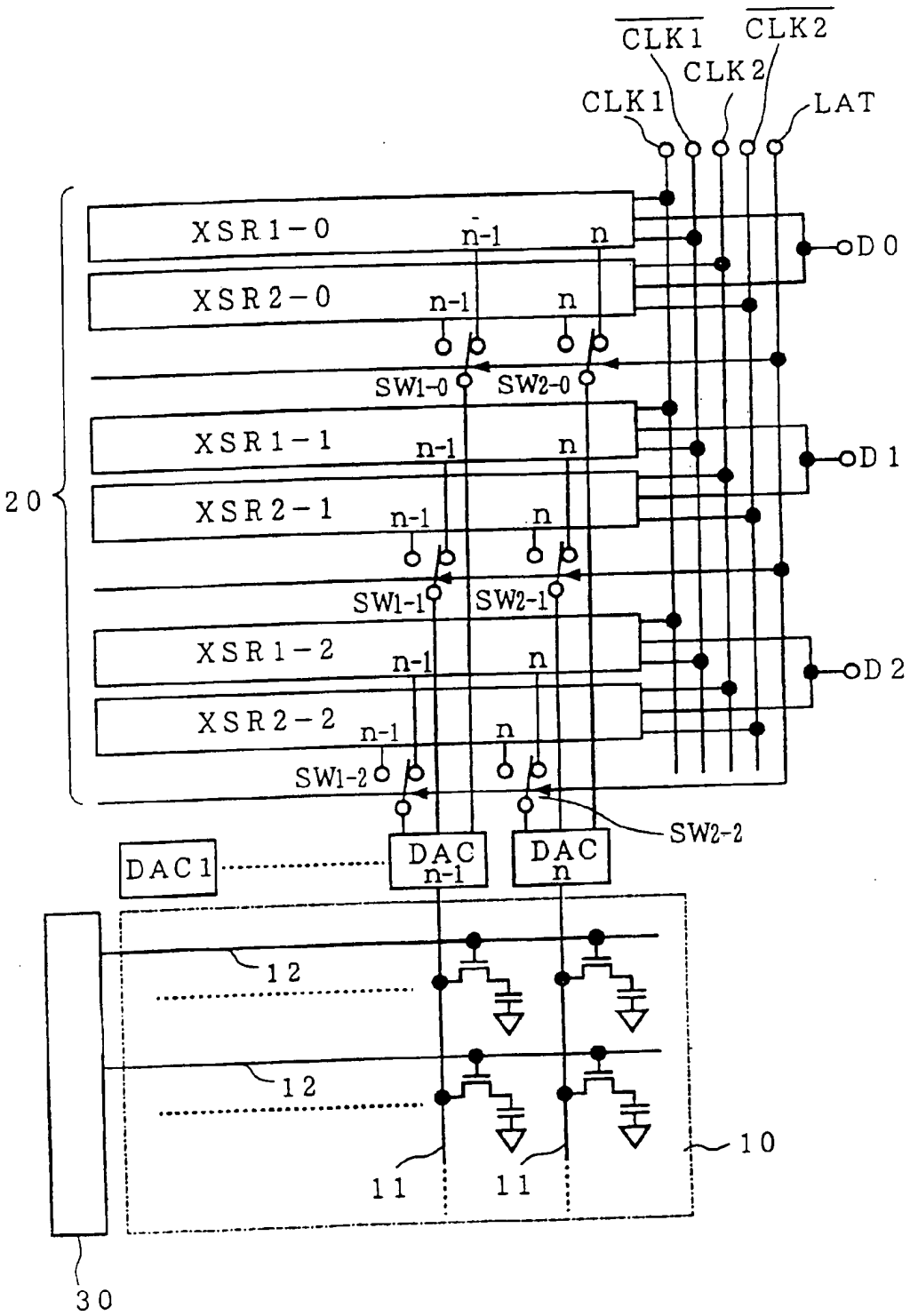
(57) **ABSTRACT**

A drive circuit for an electro-optical device, which has a plurality of pairs of shift registers for latching and holding signals representing bits of image data, a D/A converter for performing D/A-conversion on image data latched by the shift register n-bits by n-bits, for generating voltages corresponding to 2^N gray scales and for supplying the generated voltages to signal lines, and a switch group for selectively supplying image data latched by one of the shift registers of each of the pairs to the D/A converter. This drive circuit is adapted to repeatedly perform an operation of supplying the D/A converter with image data held by one of the shift registers of each of the pairs during image data is latched by the other shift register. Thus, image data can be inputted thereto at a high speed.

24 Claims, 13 Drawing Sheets

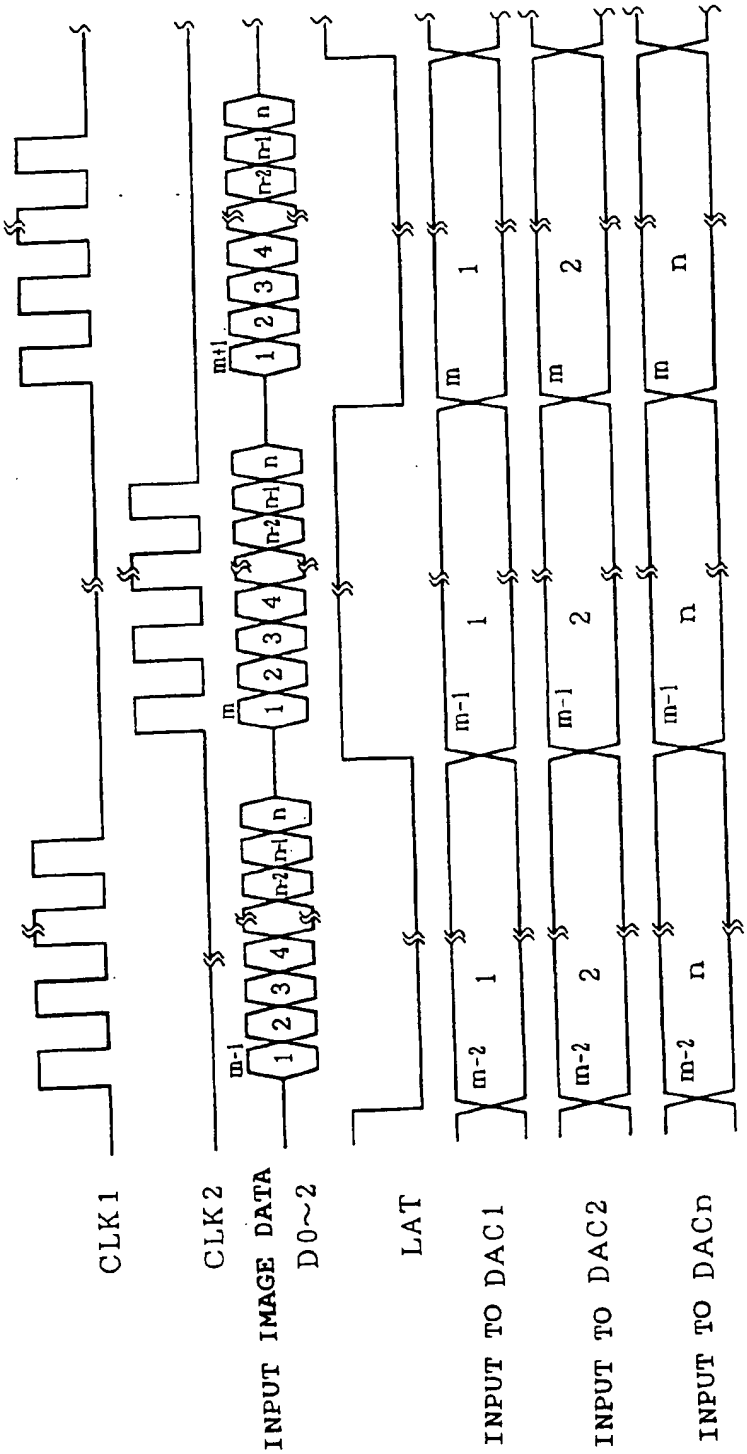


[FIG. 1]

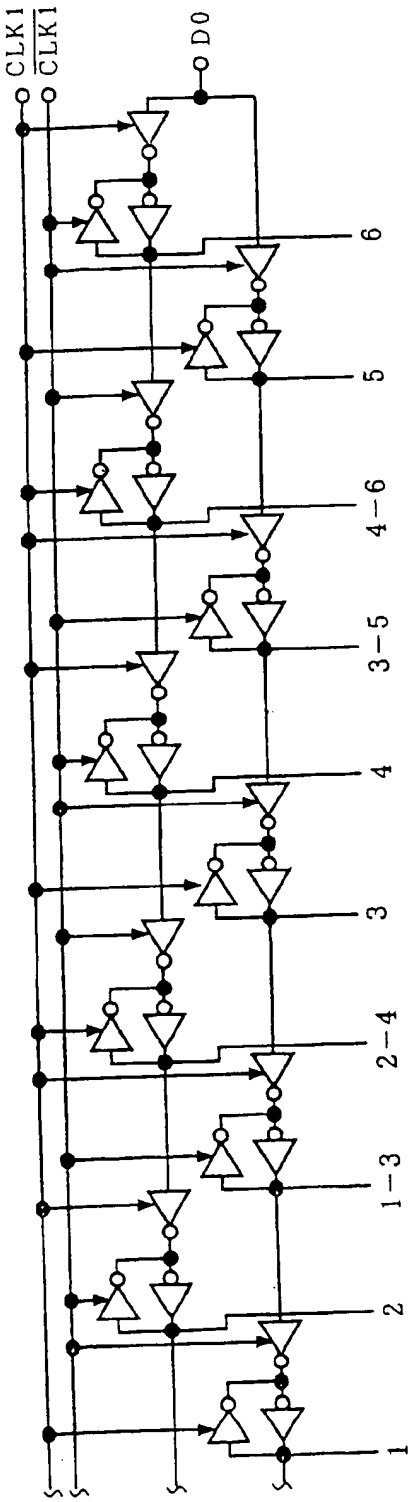


SCANNING LINE DRIVE CIRCUIT

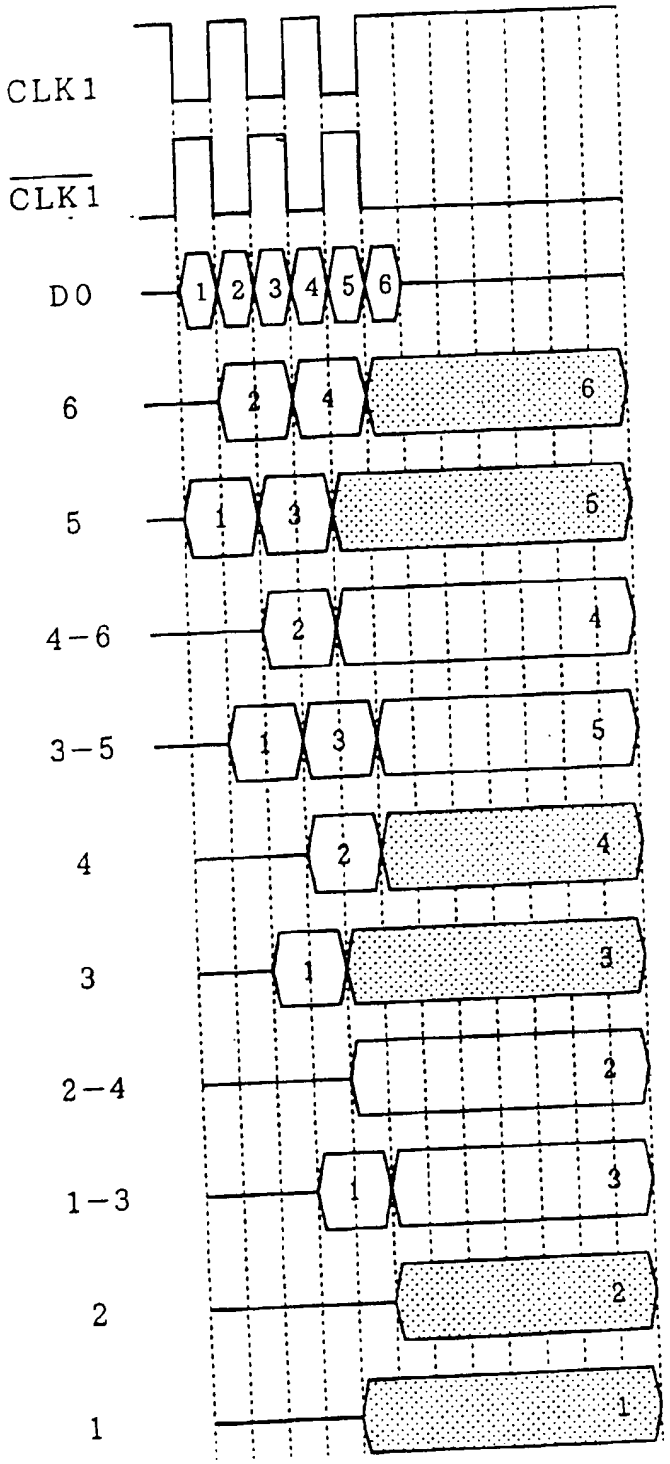
[FIG. 2]


CLK1
CLK2
INPUT IMAGE DATA D0~2
LAT
INPUT TO DAC1
INPUT TO DAC2
INPUT TO DACn

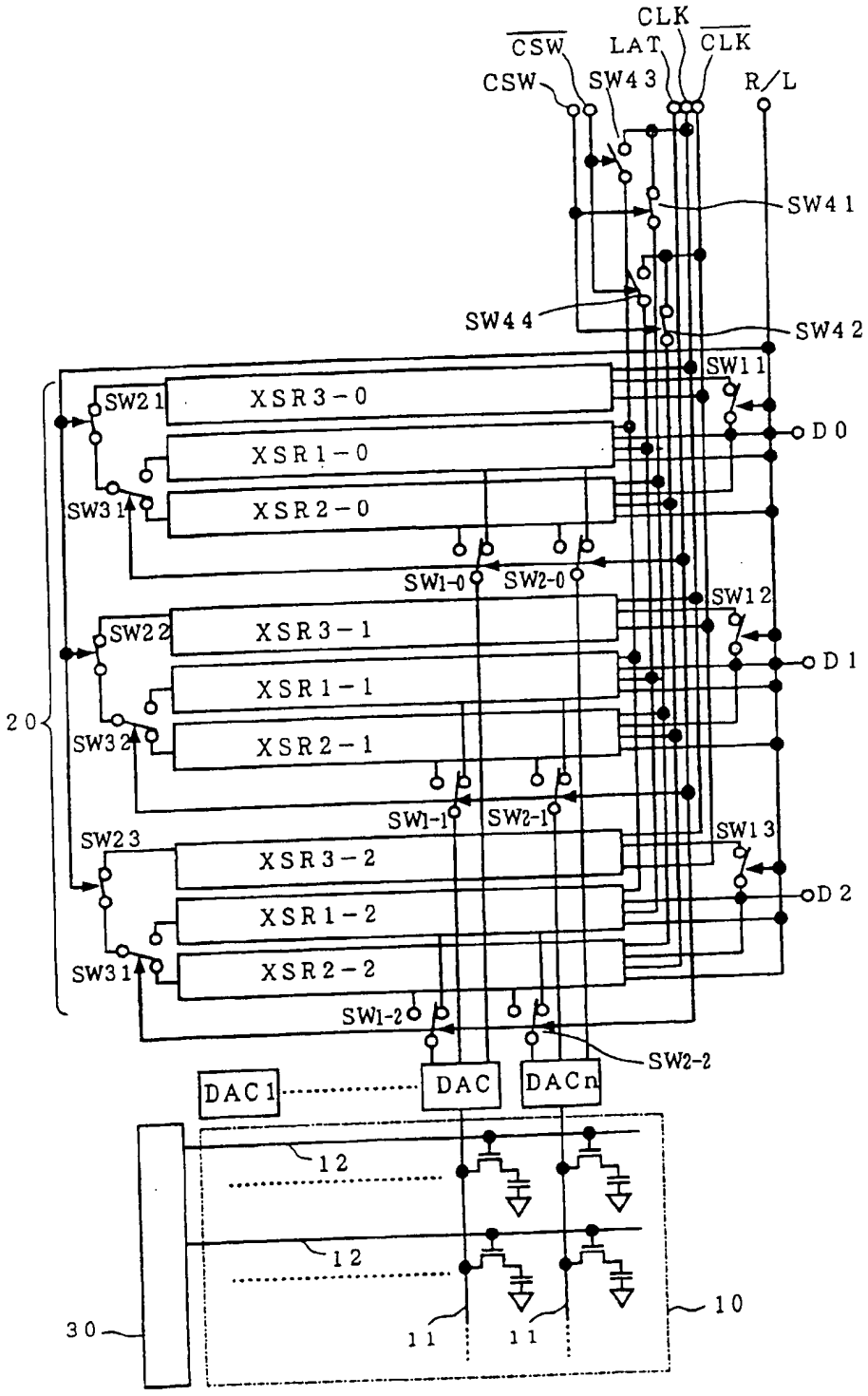
[FIG. 3]



[FIG. 4]


CLK1
$\overline{CLK1}$
DO
1 2 3 4 5 6
6
2 4 6
5
1 3 5
4-6
2 4
3-5
1 3 5
4
2 4
3
1 3
2-4
2
1-3
1 3
2
2
1
1

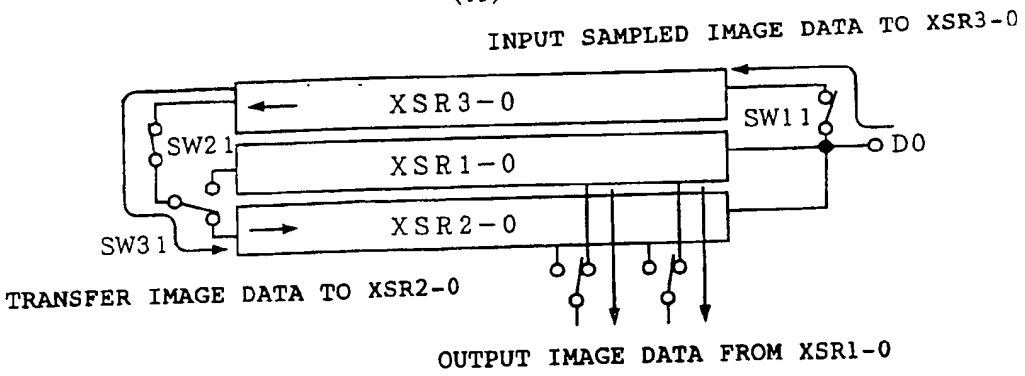
[FIG. 5]



SCANNING LINE DRIVE CIRCUIT

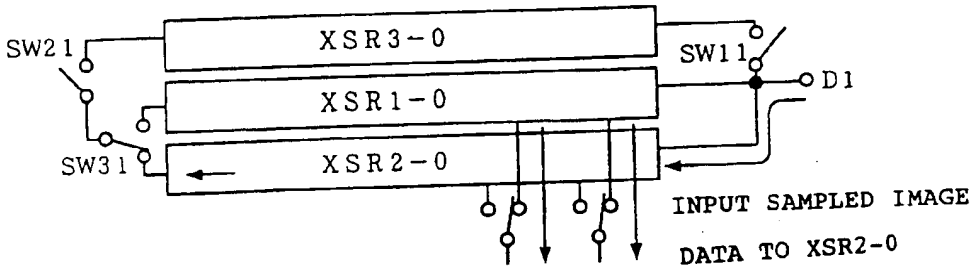
[FIG. 6]

(A)



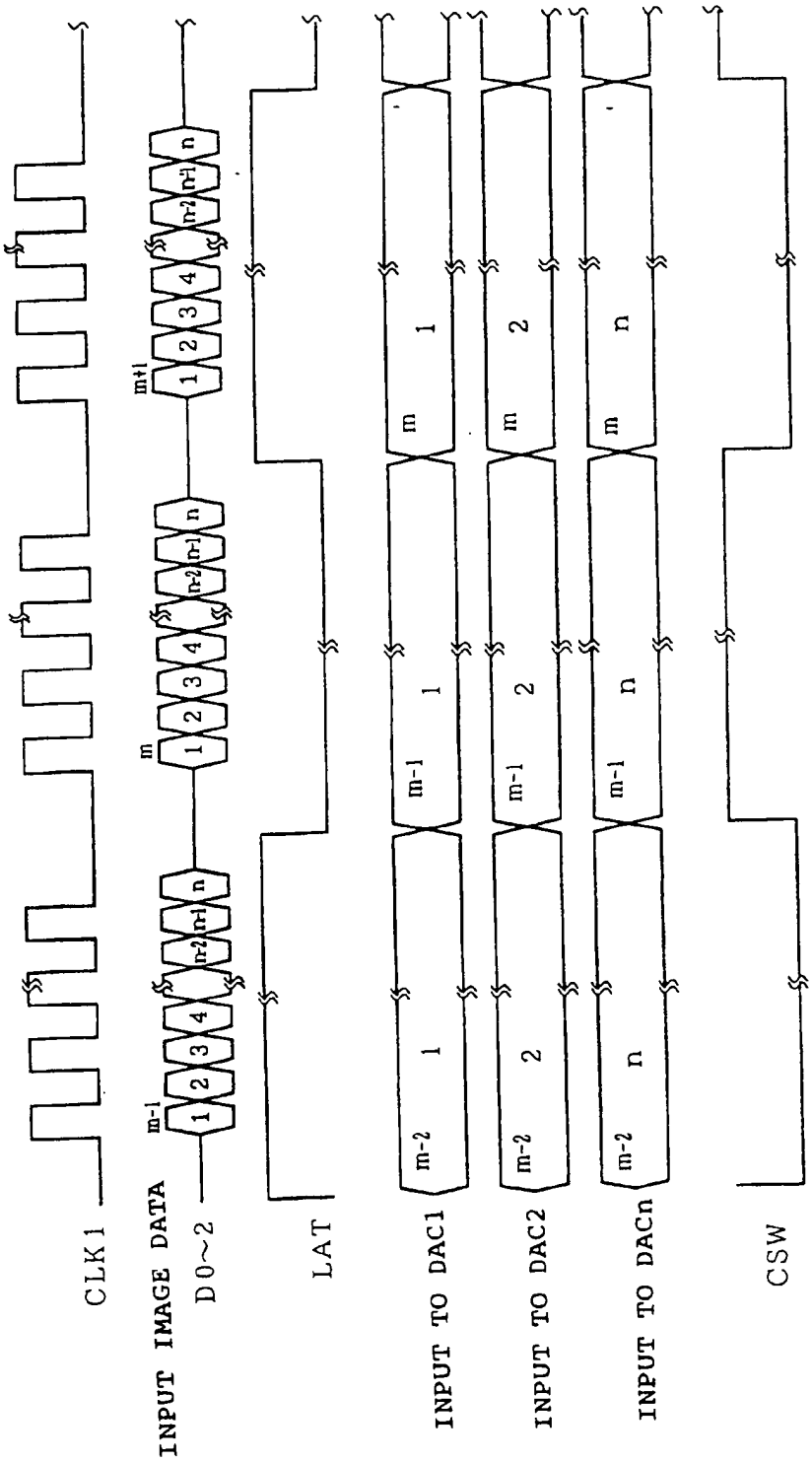
IN CASE OF PERFORMING LATERAL INVERSION

(B)

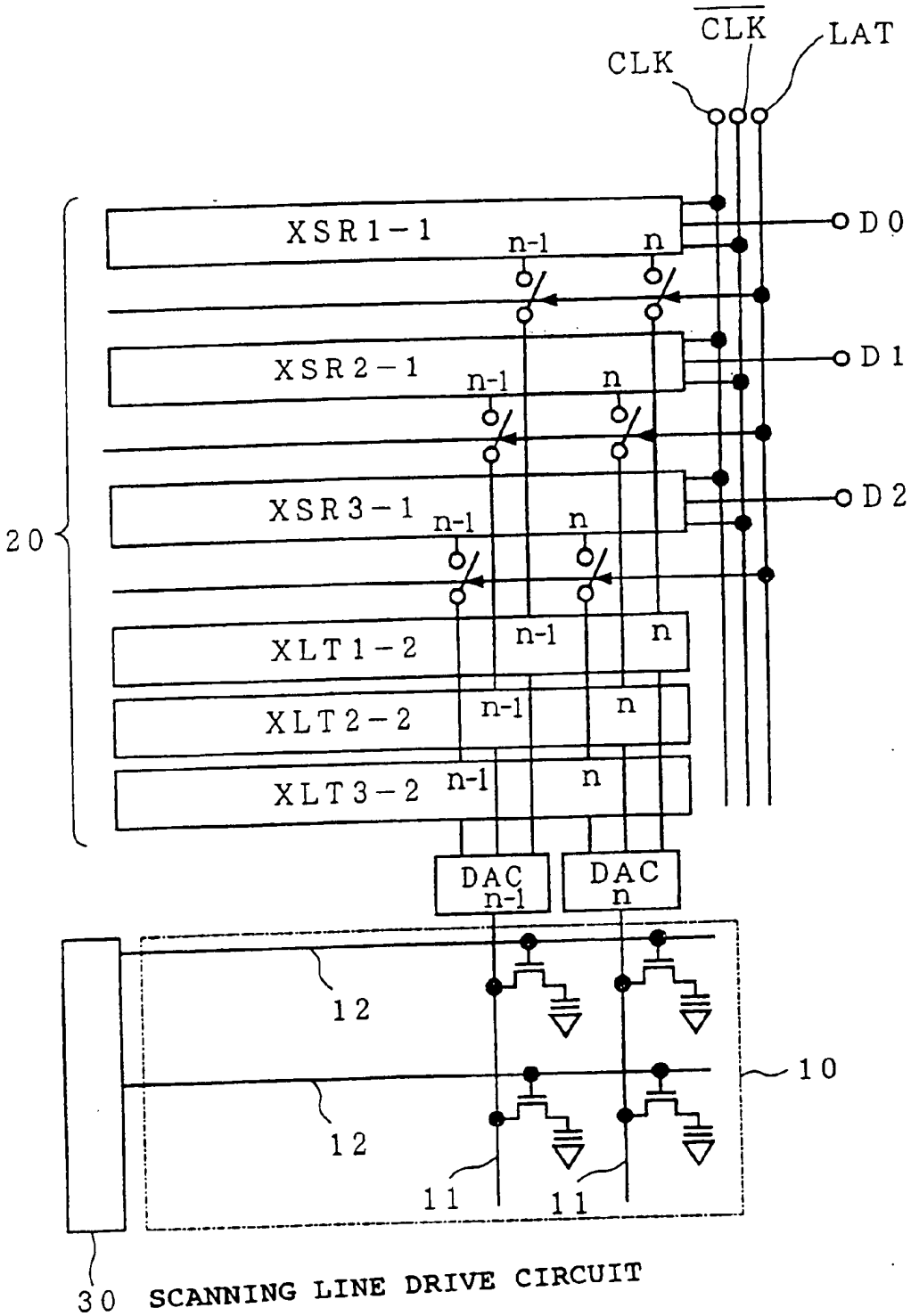


IN CASE OF PERFORMING NO LATERAL INVERSION

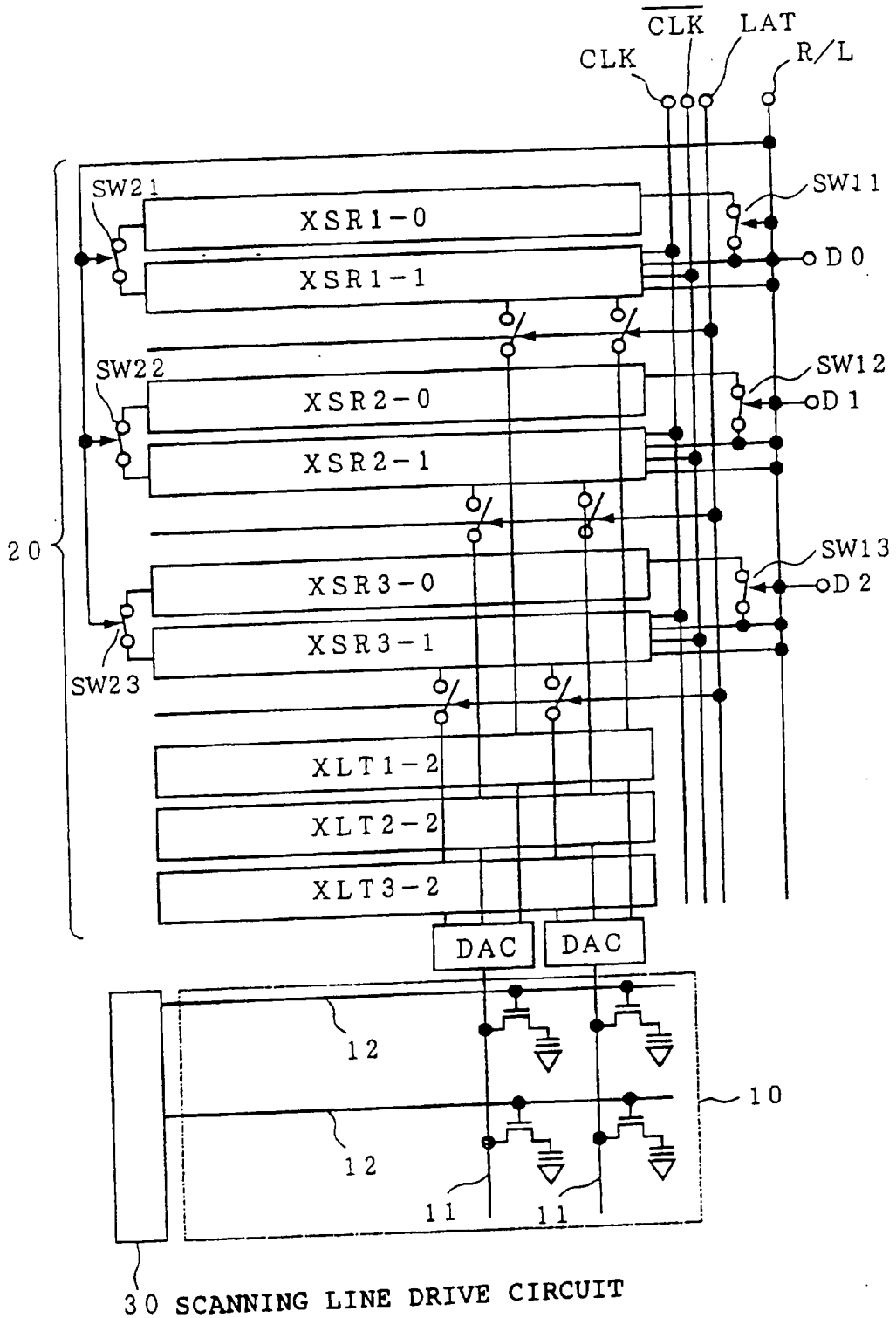
[FIG. 7]


CLK1
INPUT IMAGE DATA
D0~2
LAT
INPUT TO DAC1
INPUT TO DAC2
INPUT TO DACn
CSW

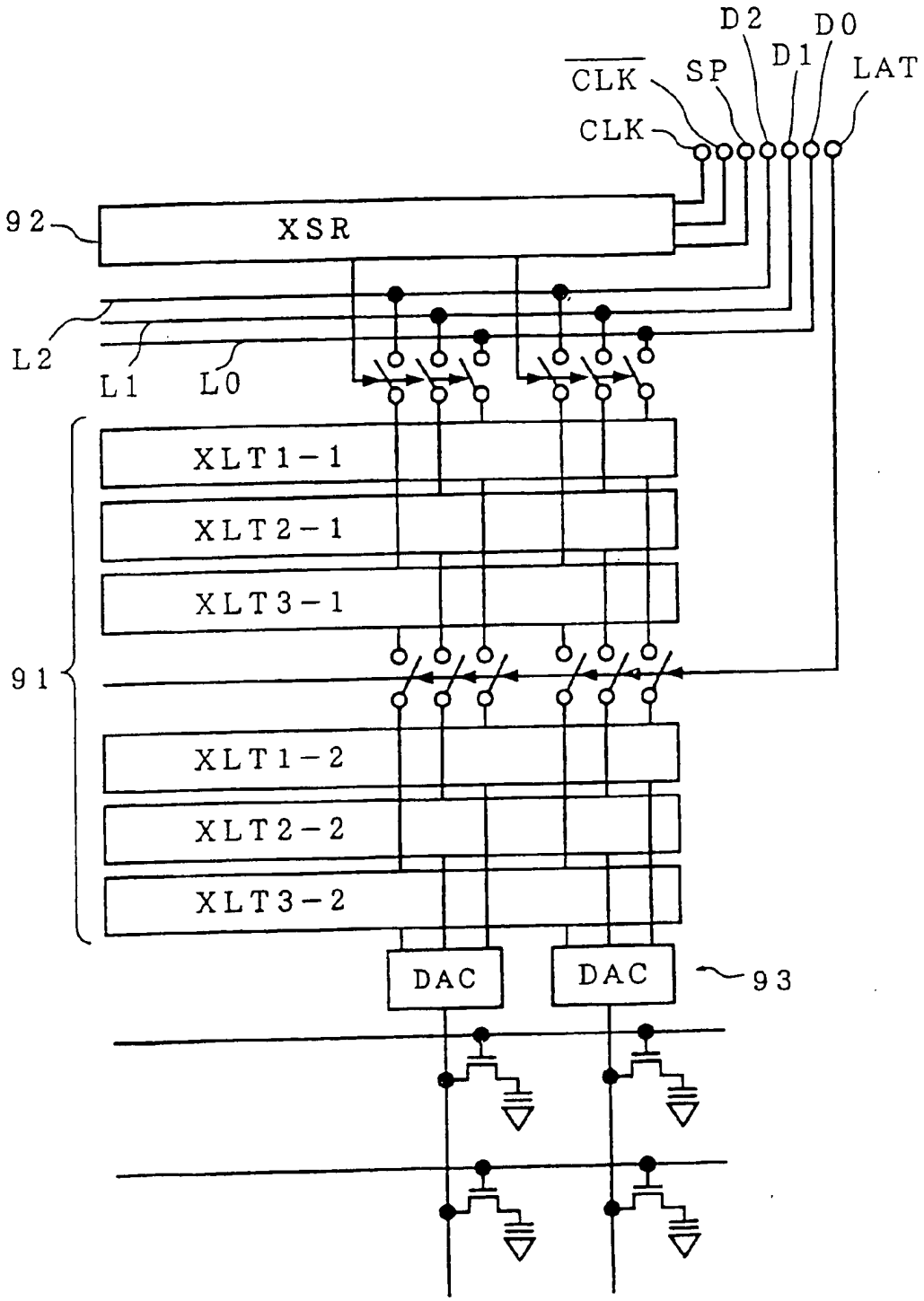
[FIG. 8]


CLK
CLK
LAT
XSR1-1
XSR2-1
XSR3-1
XLT1-2
XLT2-2
XLT3-2
n-1
n
D0
D1
D2
20
DAC
n-1
DAC
n
12
12
10
11
11
30
SCANNING LINE DRIVE CIRCUIT

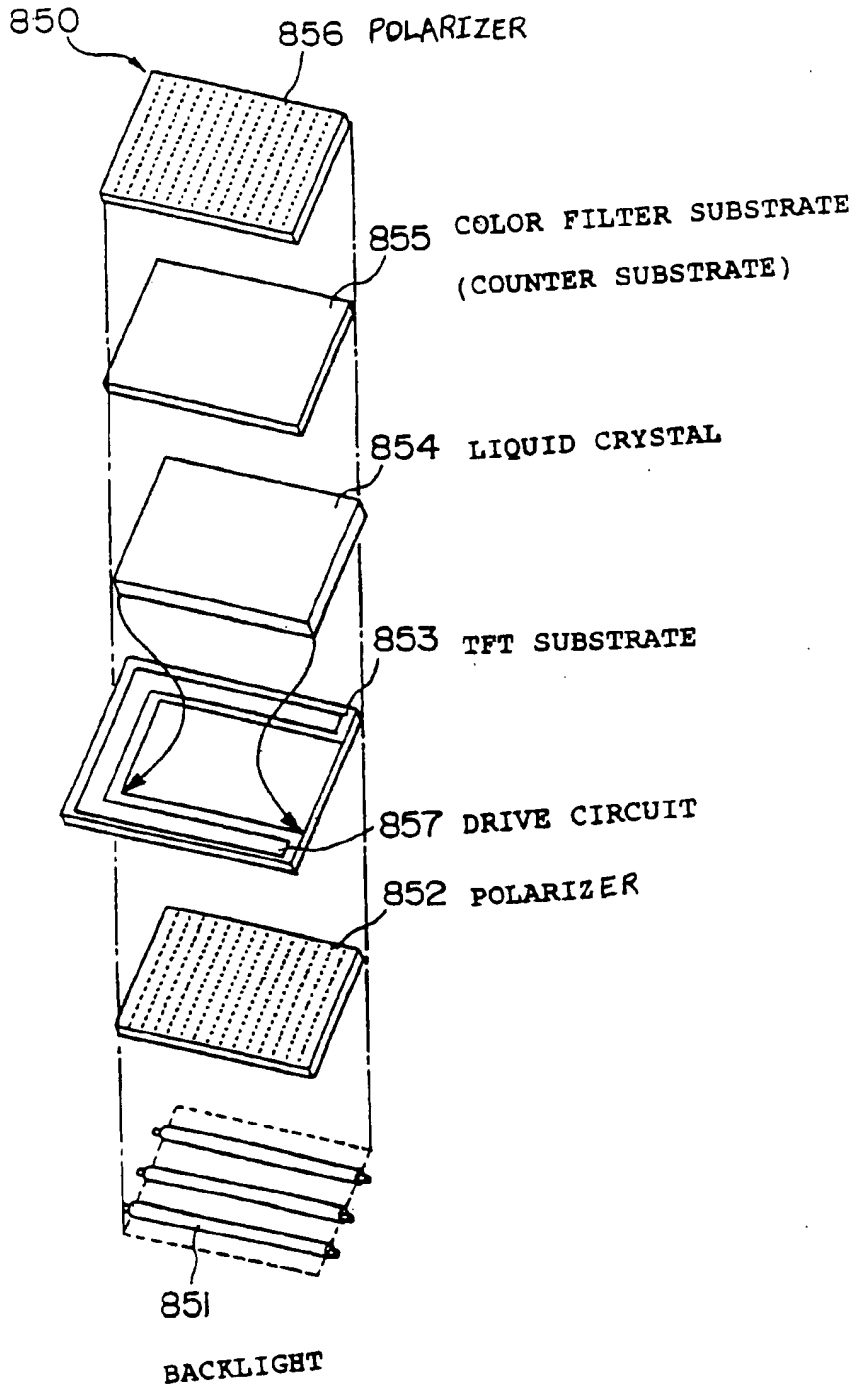
[FIG. 9]


CLK
LAT
R/L
SW21
SW11
XSR1-0
XSR1-1
D0
SW22
SW12
XSR2-0
D1
XSR2-1
20
SW13
XSR3-0
D2
XSR3-1
SW23
XLT1-2
XLT2-2
XLT3-2
DAC
DAC
12
10
12
11
11
30 SCANNING LINE DRIVE CIRCUIT

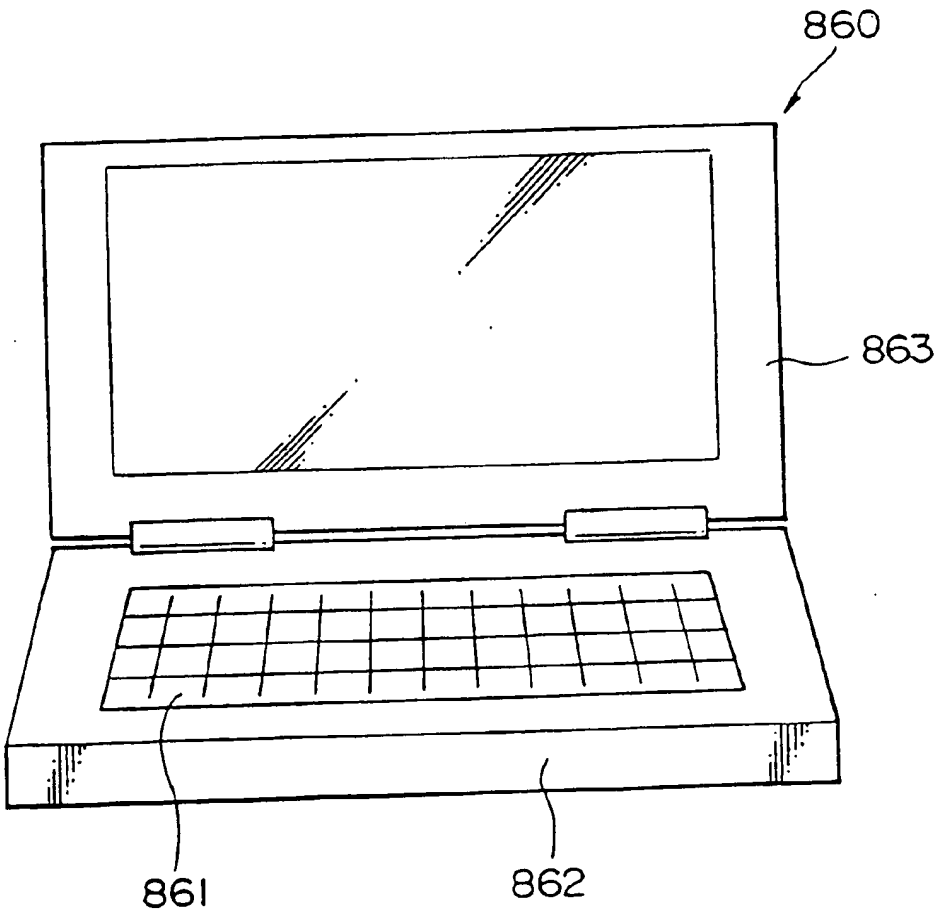
[FIG. 10]


D2
D0
D1
LAT
SP
CLK
CLK
92
XSR
L2
L1
L0
XLT1-1
XLT2-1
XLT3-1
91
XLT1-2
XLT2-2
XLT3-2
DAC
DAC
93

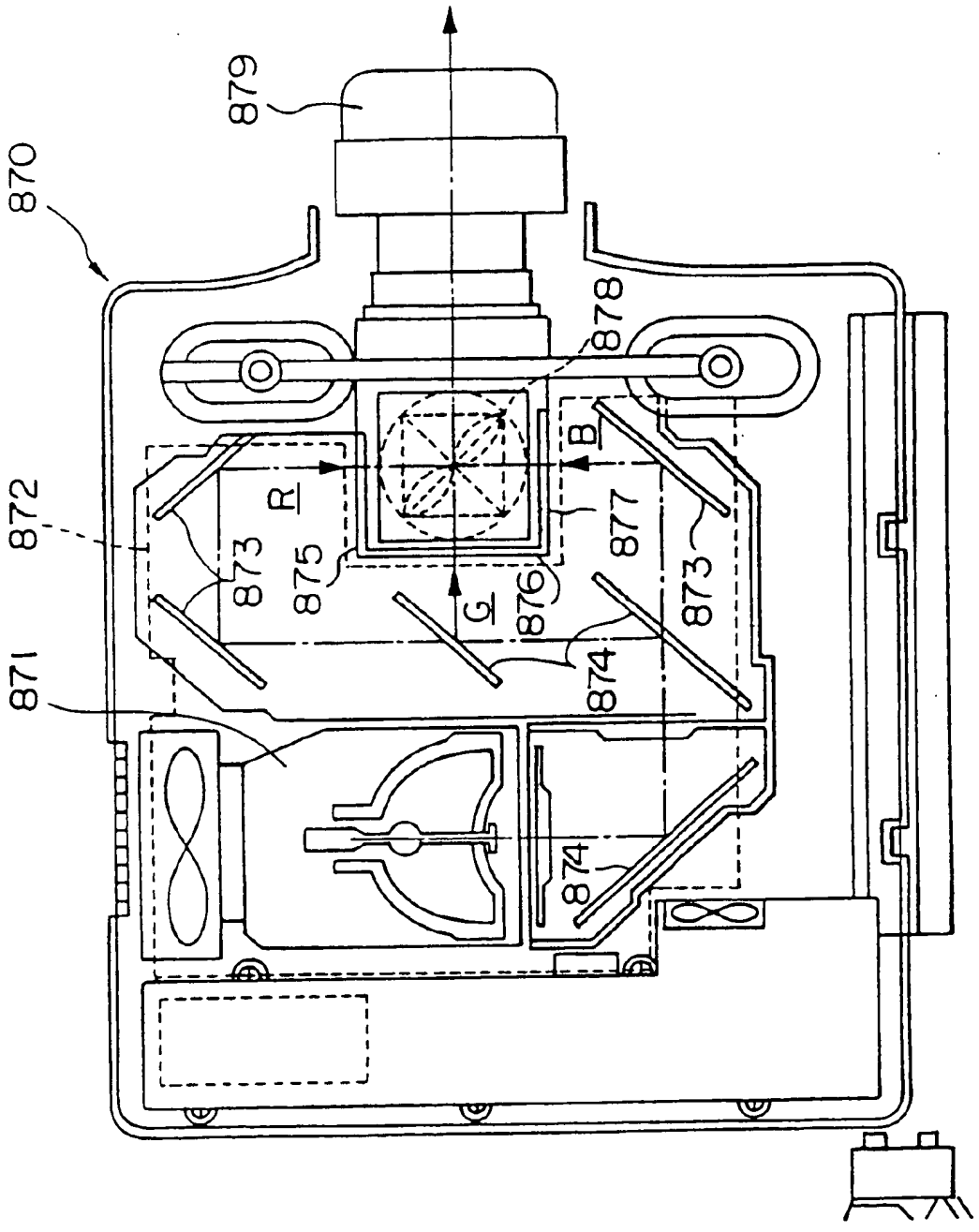
[FIG. 11]


850
856 POLARIZER
855 COLOR FILTER SUBSTRATE
(COUNTER SUBSTRATE)
854 LIQUID CRYSTAL
853 TFT SUBSTRATE
857 DRIVE CIRCUIT
852 POLARIZER
851
BACKLIGHT

[FIG. 12]



[FIG. 13]



ELECTRO-OPTICAL DEVICE DRIVE CIRCUIT, ELECTRO-OPTICAL DEVICE AND ELECTRONIC EQUIPMENT USING THE SAME

BACKGROUND OF THE INVENTION

1. Field of Invention

The present invention generally relates to a drive circuit for an electro-optical device, and more particularly, to a liquid crystal drive circuit having a D/A converter (namely, a digital-to-analog conversion circuit), and to an electro-optical device using this drive circuit, and to electronic equipment using this electro-optical device for displaying an image.

2. Description of Related Art

As shown in FIG. **10**, a conventional drive circuit for an electro-optical device comprises latching means **91** consisting of a first group of latch circuits XLT1-1 to XLT3-1, each of which sequentially latches and holds digital image data (hereunder referred to simply as image data) supplied from an external control device to terminals D0, D1 and D2, and a second group of latch circuits XLT1-2 to XLT3-2, to which image data of one line is latched by the first group of latch circuits. This drive circuit further comprises a shift register **92** for generating clock signals, which provide timing in serially latching image data present on data lines L0, L1 and L2, according to clocks CLK and $\overline{\text{CLK}}$ supplied from an external circuit. This drive circuit furthermore comprises a D/A converter **93** adapted to perform the D/A conversion of data (consisting of 3 bits in the case shown in this figure) of each of pixels respectively represented by the image data latched by the second group of latch circuits XLT1-2 to XLT3-2 for supplying predetermined voltages to each signal line in the pixel region.

In the aforementioned drive circuit, image data are input from an external circuit to the data lines L0, L1 and L2, respectively. However, the parasitic capacitance of the data lines L0, L1 and L2 has an extremely large value (which may be 100 pF or more), in comparison with that of wirings of a semiconductor integrated circuit, because of the facts that the length of the aforementioned data lines L0, L1 and L2 of an electro-optical device reaches several tens of cm and that the electro-optical device has many signal lines intersecting the data lines L0, L1 and L2. Thus, the rate of transmission of image data at a point on each of the data lines L0, L1 and L2 decreases with a reduction in the distance between the point and a tip end thereon, namely, with the distance from a corresponding data input terminal to the point. This results in a decrease in the timing margin of the clock signal providing the first group of latch circuits XLT1-1 through XLT3-1 with data latch timing with which data output from the shift register **92** is latched by the first group of latch circuits XLT1-1 to XLT3-1. Consequently, it becomes difficult to input image data thereto at a high speed.

Further, the output impedance of an IC for outputting image data should be reduced so as to achieve the high-speed input Of image data. However, the large parasitic capacitance of the data lines L0, L1 and L2 makes it extremely difficult to realize the high-speed input of image data. For instance, in the case of a liquid crystal panel having a resolution of 640x480 dots and conforming to the VGA (Video Graphic Array) standard, the frequency of an image data input signal is 20 MHz or so. Moreover, in the case of a liquid crystal panel conforming to the SVGA (Super Video Graphics Array) standard, the frequency of an image data input signal reaches 100 MHz. Therefore, it is difficult to realize the high-speed input of image data. Especially, in the case of an electro-optical device using a polysilicon TFT as an element of a drive circuit, at least 3.3 V, preferably, 5 V or more is needed as the amplitude of a signal representing the aforementioned image data. The driving ability of the IC outputting image data should be enhanced so as to input image data to the data lines having large parasitic capacitance at a high speed by using a signal of a large amplitude.

SUMMARY OF THE INVENTION

The present invention is proposed to solve the aforementioned problems of the conventional drive circuit. Accordingly, the present invention provides a drive circuit for an electro-optical device, to which image data can be input at a high speed from an external circuit.

The present invention also provides a drive circuit for an electro-optical device, which is enabled to lower the driving ability of the IC inputting image data and reduce the power consumption thereof.

The present invention also provides a drive circuit for an electro-optical device, which decreases the wiring pitch of signal lines in a pixel area.

The present invention provides a drive circuit for an electro-optical device having a function of performing lateral inversion of an image, which can perform lateral inversion of an image without having what is called a reverse reading circuit for reading image data of one line in a reverse direction from a memory in which image data is stored.

According to an aspect of the present invention, there is provided a drive circuit for an electro-optical device, which is configured so that the shift register is used for latching image data, instead of generating clock signals providing data latching timing to the latch circuit for latching image data input from an external circuit, differently from the conventional drive circuit.

This results in a decrease in the length of each of the data lines between the corresponding image data input terminal and the shift register for latching image data. Thus, in the case of the drive circuit of the present invention, there is no necessity for considering the timing margin of the clock signal providing each of the latch circuits with the latching timing, differently from the conventional drive circuit. Consequently, there is provided a drive circuit for an electro-optical device, which enables the high-speed input of image data to an electro-optical device from an external circuit at a high speed and lowers the driving ability of the IC for inputting image data and reduces the power consumption thereof.

Moreover, according to the present invention, a liquid crystal drive circuit having a D/A converter is configured so that a pair of shift registers for latching image data is provided corresponding to each of bits of the image data, that the image data is latched from an external circuit to one of the shift registers of such a pair, image data of one line latched into the other shift register is simultaneously transferred to the D/A converter, and that a transferring switch for enabling this transfer of such image data is placed between the shift register provided corresponding to each of the bits.

Thus, there is provided a drive circuit for an electro-optical device, which sets the wiring pitch of signal lines in a pixel area at a smaller value, as compared with the case of placing all of the transferring switches at the D/A-converter side.

Furthermore, a delaying shift register is provided in addition to the pair of shift registers corresponding to each

of the bits. Moreover, an on-off switch for enabling and/or disabling the transfer of image data is provided between this delaying shift register and an image data input terminal. An on-off switch for enabling and/or disabling the transfer of image data and a changing switch for permitting the transfer of image data to one of the shift registers of this pair are provided between the delaying shift register and another pair of shift registers.

Thus, the switches are controlled to thereby cause the delaying register to operate. Consequently, the lateral inversion of an image can be enabled only by a drive circuit of the present invention without providing what is called a reverse reading circuit, which is used for reading image data of one line from a memory storing the image data in a reverse direction, in an electro-optical device having the function of performing the lateral inversion of an image.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features, objects and advantages of the present invention will become apparent from the following description of preferred embodiments with reference to the drawings in which like reference characters designate like or corresponding parts throughout several views, and in which:

FIG. **1** is a circuit diagram showing the configuration of a first embodiment of a drive circuit for a liquid crystal display device according to the present invention;

FIG. **2** is a timing chart illustrating the operation timing of a signal line drive circuit shown in FIG. **1**;

FIG. **3** is a circuit diagram showing the configuration of a practical example of a logic circuit of a shift register provided in the signal line drive circuit shown in FIG. **1**;

FIG. **4** is a timing chart illustrating the operation timing of the shift register shown in FIG. **3**;

FIG. **5** is a circuit diagram showing the configuration of a second embodiment of a drive circuit for a liquid crystal display device according to the present invention;

FIGS. 6(A) and 6(B) are diagrams illustrating the function of a signal line drive circuit of the embodiment shown in FIG. **5**;

FIG. **7** is a timing chart illustrating the operation timing of a signal line drive circuit of the embodiment shown in FIG. **5**;

FIG. **8** is a circuit diagram showing the configuration of a third embodiment of a drive circuit for a liquid crystal display device according to the present invention;

FIG. **9** is a circuit diagram showing the configuration of a fourth embodiment of a drive circuit for a liquid crystal display device according to the present invention;

FIG. **10** is a circuit diagram showing the configuration of an example of a conventional drive circuit for a liquid crystal display device;

FIG. **11** is a diagram illustrating an embodiment of a liquid crystal display device of the present invention;

FIG. **12** is a diagram illustrating a portable computer that is an embodiment of electronic equipment of the present invention; and

FIG. **13** is a diagram illustrating a projector that is another embodiment of electronic equipment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. **1** is a circuit diagram showing the configuration of a first embodiment of a drive circuit for a liquid crystal panel according to the present invention. In this figure, reference numeral **10** designates a pixel area in which a plurality of pixel elements each consisting of a pixel electrode and a TFT are placed in a matrix-like manner. Reference numeral **20** denotes what is called an X-system, namely, a signal line drive circuit for driving signal lines **11**. Reference numeral **30** designates a scanning line drive circuit for selecting scanning lines **12** in turn. In this embodiment, the aforementioned signal line drive circuit **20** is constructed to drive signal lines for 3-bit (or 8-gray scale) digital image data. Incidentally, the present invention is not limited to this signal line drive circuit **20**. Further, pairs of shift registers XSR1-0, XSR2-0; XSR1-1 XSR2-1; and XSR1-2, XSR2-2 are provided in the circuit **20** corresponding to input terminals D0, D1 and D2 through which the bits of image data supplied from an external control device are inputted, respectively.

Reference characters DAC1 to DACn designate 3-bit D/A converters provided in such a manner as to respectively correspond to the signal lines **11** drawn in the pixel area **10**. In this embodiment, each pair of switches SW1-0, SW2-0; SW1-1, SW2-1; SW1-2, SW2-2 for switching and transferring data are provided between a corresponding pair of shift registers XSR1-0, XSR2-0; XSR1-1 XSR2-1; and XSR1-2, XSR2-2 and the corresponding ones of the D/A converters DAC1 to DACn. The states of these switches are changed according to a switching control signal LAT supplied from the external control device. Thus, 1-bit image data is supplied from one of the shift registers XSR1-0, XSR2-0; XSR1-1, XSR2-1; and XSR1-2, XSR2-2 of each of the pairs, namely, image data composed of a total of 3 bits are supplied therefrom to the D/A converters DAC1 to DACn, whereupon the image data are D/A-converted. Then, voltages respectively corresponding to 8 gray scales are generated and supplied to the corresponding signal lines **11**.

Further, each of the pairs of shift registers XSR1-0, XSR2-0; XSR1-1, XSR2-1; and XSR1-2, XSR2-2 is connected to the image data input terminals D0, D1 and D2. The shift registers XSR1-0, XSR1-1 and XSR1-2 are caused according to the clock signals CLK1 and $\overline{\text{CLK1}}$ supplied from the external control device to latch the data and perform shifting operations. Moreover, the shift registers XSR2-0, XSR2-1 and XSR2-2 are caused according to the clock signals CLK2 and $\overline{\text{CLK2}}$ to latch the data and perform shifting operations. Thus, each of these shift registers operate in such a way as to sequentially latch the image data bit by bit from the image data input terminals D0, D1 and D2 and then shift the data in a reverse direction.

As shown in FIG. **1**, among the switches for controlling data transfer between the shift registers XSR1-0, XSR2-0; XSR1-1 XSR2-1; and XSR1-2, XSR2-2 and the D/A converters DAC1 to DACn, the switches SW1-0, SW2-0 are provided between the shift registers XSR2-0 and XSR1-1, while the switches SW1-1 and SW2-1 are provided between the shift registers XSR2-1 and XSR1-2. Although these switches may be placed between the shift register XSR2-2 and each of the D/A converters DAC1 to DACn, these switches are provided between the shift registers as described above. Thus, the wiring pitch of the signal lines in the pixel area can be made to be small, as compared with that of the signal lines in the case of placing these switches at the side of the D/A converters. Consequently, this embodiment has an advantage in that the pixel area can be highly integrated.

Moreover, even when the pixel area and the drive circuit are formed on a substrate, it is preferable that the image data input terminals D0, D1 and D2 are positioned at the right

side of the substrate corresponding to the circuit of FIG. 1, as viewed in this figure. Generally, in the case of the conventional drive circuit, the image data input terminals are placed at the left side of the substrate, and the data are shifted in a direction from the shift register, which is closest to the input terminals, to the shift register that is most distant therefrom. It is, thus, necessary for the external control device to perform the reverse reading of image data when image data of 1 line is read from a memory storing the image data. In contrast, this embodiment eliminates the necessity for the reverse reading of image data by placing the image data input terminals at the right side of the substrate. Thus, this embodiment has an advantage in that the method of reading image data from the memory is simplified.

Next, an operation of the aforementioned signal line drive circuit **20** will be described hereinbelow by referring to a timing chart of FIG. **2**. First, 3-bit image data VD0, VD1 and VD2 are sequentially inputted in parallel to the image data input terminals D0, D1 and D2 from the control device placed outside or the like. Moreover, clock signals CLK1, $\overline{CLK1}$ or CLK2, $\overline{CLK2}$ synchronized with the aforementioned image data VD0, VD1 and VD2 are input to the signal line drive circuit **20**. In this embodiment, the signal level of a switching control signal LAT supplied from the external control device is changed between high and low levels every input of image data of 1 line. Furthermore, each pair of the clock signals (CLK1, $\overline{CLK1}$) or (CLK2, $\overline{CLK2}$) is generated in response to the switching control signal LAT so that when one of the pairs of the clock signals is being input, the inputting of the other pair of the clock signals is halted.

Thus, when the switching control signal LAT is at the low level, the input image data VD0, VD1 and VD2 are sequentially latched by a set of the shift registers XSR1-0, XSR1-1 and XSR1-2 in response to the clock signals CLK1 and $\overline{CLK1}$, and then shifted therein. In contrast, when the switching control signal LAT is at the high level, the inputted image data VD0, VD1 and VD2 are sequentially latched by the other set of the shift registers XSR2-0, XSR2-1 and XSR2-2 in response to the clock signals CLK2 and $\overline{CLK2}$, and then shifted therein.

Further, when one of the sets of the shift registers XSR1-0, XSR1-1 and XSR1-2 latch image data (namely, the switching control signal LAT is at the low level) by controlling the switching control switches SW1-0 to SW2-2 according to the switching control signal LAT, image data latched by the other set of the shift registers XSR2-0, XSR2-1 and XSR2-2 is transferred to the D/A converters DAC1 to DACn. Conversely, when the latter set of the shift registers XSR2-0, XSR2-1 and XSR2-2 latch image data (namely, the switching control signal LAT is at the high level), the image data latched by the former set of the shift registers XSR1-0, XSR1-1 and XSR1-2 is transferred to the D/A converters DAC1 to DACn. As a result of repeatedly performing this process, voltage signals obtained by D/A-converting image data of one screen are successively supplied to the signal lines **11** in the pixel area **10**.

Incidentally, the scanning lines **12** are driven in turn by a scanning-line-side (namely, a Y-system) drive circuit (not shown) to a selection level (namely, the high level) in synchronization with a change in the output of each of the D/A converters DAC1 to DACn in the pixel area **10**. Then, a TFT corresponding to each pixel element connected to the selected scanning line is turned on. Further, a voltage of the signal line **11** is applied to a corresponding pixel electrode.

FIG. **3** shows a more practical example of the shift register XSR of the signal line drive circuit **20** of FIG. **1**. Further, FIG. **4** illustrates an operation of this shift register. Incidentally, FIG. **3** shows 10 stages of the signal line drive circuit of FIG. **1**. FIG. **4** illustrates the operation timing in the case that 6-bit data is latched by the 10 stages of the shift register. As illustrated in FIG. **3**, one stage of the shift register XSR comprises an inputting clocked inverter for inputting signals, and a latch circuit constituted by a pair of inverters respectively having an input terminal and an output terminal, which are connected to each other. The feedback inverter of this latch circuit is constituted as a clocked inverter, and is operated according to a clock of a phase opposite to the phase of a clock corresponding to the other inverter thereof inputting signals. Further, the inputting inverters of odd-numbered stages of the latch circuit are operated by the same clock CLK1. Moreover, the inputting inverters of even-numbered stages of the latch circuit are operated according to the same clock $\overline{CLK1}$ having a phase opposite to the phase of the clock CLK1.

According to the shift register of the aforementioned configuration, the length of the data line between the image data input terminal and the shift register for latching image data is short. Thus, this embodiment eliminates the necessity for considering the timing margin of the clock providing the first group of latch circuit with the latching timing. Consequently, it is possible for this embodiment to input image data at a high speed from an external circuit thereto. Moreover, in the case of the signal line drive circuit of the aforementioned embodiment, lines for supplying clock signals are longer than the data lines L0, L1 and L2, differently from the conventional signal line drive circuit of FIG. **10**. However, as is apparent from FIG. **2**, the frequency of the clock signal is half the frequency of a signal representing image data. Thus, in the case of inputting clock signals, the degree of necessity for high-speed input capability is not high, as compared with the case of inputting image data. It is, therefore, unnecessary that the degree of enhancing the driving ability of the IC (or controller) outputting image data and clocks is not high, differently from the case of using the signal line drive circuit of FIG. **10**. Consequently, the power consumption of the drive circuit and the cost of the IC can be prevented from increasing.

FIG. **5** is a circuit diagram showing the configuration of a second embodiment of the signal line drive circuit for a liquid crystal display device according to the present invention. The signal line drive circuit of this embodiment has a configuration for facilitating the lateral inversion of a display of an image, and is constructed as a signal line drive circuit for 3-bit image data, similar to the signal line drive circuit of the first embodiment of FIG. 1. Namely, the signal line drive circuit of the second embodiment has delay shift registers XSR3-0, XSR3-1 and XSR3-2 corresponding to the input terminals D0, D1 and D2 for inputting the bits of image data supplied from the external control device, in addition to the shift registers XSR1-0, XSR2-0; XSR1-1, XSR2-1; and XSR1-2, XSR2-2.

Even in the second embodiment, among the switches for controlling data transfer between the shift registers XSR1-0, XSR2-0; XSR1-1, XSR2-1; and XSR1-2, XSR2-2 and the D/A converters DAC1 to DACn, the switches SW1-0 and SW2-0 are provided between the shift registers XSR2-0 and XSR1-1, while the switches SW1-1 and SW2-1 are provided between the shift registers XSR2-1 and XSR1-2.

Further, in the signal line drive circuit of the second embodiment, switches SW11, SW12 and SW13 for enabling and disabling data transfer are respectively provided between the delay shift register XSR3-0 and the image data input terminal D0, between the delay shift register XSR3-1

and the image data input terminal D1 and between the delay shift register XSR3-2 and the image data input terminal D2. Furthermore, the switches SW21, SW22 and SW23 for enabling and disabling data transfer are respectively provided between the delay shift register XSR3-0 and a pair of the shift registers XSR1-0 and XSR2-0, between the delay shift register XSR3-1 and a pair of the shift registers XSR1-1 and XSR2-1 and between the delay shift register XSR3-2 and a pair of the shift registers XSR1-2 and XSR2-2. Moreover, the switches SW31, SW32 and SW33 for enabling data transfer between the corresponding input terminal and one of the shift registers of each of these pairs are respectively provided between the delay shift register XSR3-0 and the pair of the shift registers XSR1-0 and XSR2-0, between the delay shift register XSR3-1 and the pair of the shift registers XSR1-1 and XSR2-1 and between the delay shift register XSR3-2 and the pair of the shift registers XSR1-2 and XSR2-2.

Furthermore, in the second embodiment, each of switches SW41, SW42, SW43 and SW44 for enabling and disabling the supplying of shift clocks CLK, $\overline{CLK}$ is provided between the corresponding clock input terminal and the corresponding one of the shift registers XSR1-0, XSR2-0; XSR1-1, XSR2-1; and XSR1-2, XSR2-2. The switches SW41, SW42, SW43 and SW44 are configured in such a manner as to be enabled and disabled according to switch control signals CSW and $\overline{CSW}$, which are supplied from the external control device, in a complementary manner.

When the clocks CLK and $\overline{CLK}$ are supplied to the shift registers XSR1-0, XSR1-1 and XSR1-2 through the switch SW41, SW42; SW43, SW44, the supplying of the clocks to the shift registers XSR2-0, XSR2-1 and XSR2-2 is interrupted. Conversely, when the clocks CLK and $\overline{CLK}$ are supplied to the shift registers XSR2-0, XSR2-1 and XSR2-2, the supplying of the clocks to the shift registers XSR1-0, XSR1-1 and XSR1-2 is interrupted. On the other hand, the clocks CLK and $\overline{CLK}$ can be always supplied to the delay shift registers XSR3-0, XSR3-1 and XSR3-2.

Furthermore, the switches SW11, SW12, SW13, SW21, SW22 and SW23 are adapted to be simultaneously controlled according to control signals R/L supplied from the external control device in such a way as to be brought into an on-state or off-state. Further, regarding the shift registers XSR1-0, XSR2-0; XSR1-1, XSR2-1; and XSR1-2, XSR2-2, the direction, in which data is shifted, is controlled by this control signal R/L. When the switches SW11 to SW23 are turned off, a shifting operation is performed on the registers in a direction from the right to the left, as viewed in this figure, similarly as in the case of the first embodiment. Conversely, when the switches SW11 to SW23 are turned on, the shifting operation is performed on the registers in a direction from the left to the right.

Next, an operation of the shift register of the signal line drive circuit of the second embodiment will be described hereunder by referring to FIG. 6. When the lateral inversion of a display of an image is performed, the switches SW11, SW12 and SW13 provided between the aforementioned delay shift registers XSR3-0, XSR3-1, XSR3-2 and the image data input terminals D0, D1 and D2 are turned on. Moreover, the switches SW21, SW22 and SW23 provided between the delay shift registers XSR3-0, XSR3-1, XSR3-2 and the shift registers XSR1-0, XSR2-0; XSR1-1, XSR2-1; and XSR1-2, XSR2-2 are turned on.

FIG. 6(A) illustrates such an operation of the shift registers XSR1-0, XSR2-0 and XSR3-0. Incidentally, the switch SW31 (or SW32 or SW33) is closed in such a way as to connect data to the shift register XSR2-0 (or XSR2-1 or XSR2-2). Upon completion of transfer of data of 1 line, the switch SW11 (or SW12 or SW13) and SW21 (or SW22 or SW23) remain turned on, while the switch SW31 is closed in such a manner as to connect data to the shift register XSR3-0 (or XSR1-1 or XSR1-2). As illustrated in FIG. 6(A), image data inputted from the input terminal D0 (or D1 or D2) are latched sequentially by the shift register XSR3-0 (or XSR3-1 or XSR3-2). Then, the image data are transferred to the shift register XSR1-0 or XSR2-0 (or XSR1-1 or XSR2-1; XSR1-2 or XSR2-2), and shifted in a direction (namely, from the left to the right as viewed in this figure) opposite to the direction in which the image data are shifted in the first embodiment of FIG. 1. Thus, the inversion of a display of an image can be achieved without changing the order in which image data representing the image is read from a memory having stored the image data.

Incidentally, when the displaying of an image is performed without conducting the lateral inversion thereof, similarly as in the case of the first embodiment, it is sufficient that the switch SW11 (or SW12 or SW13), which is provided between the delay shift register XSR3-0 (or XSR3-1 or XSR3-2) and the input terminal D0 (or D1 or D2), and the switch SW21 (or SW22 or SW23), which is provided between the delay shift register XSR3-0 (or XSR3-1 or XSR3-2) and a pair of shift registers XSR1-0, XSR2-0 (or XSR1-1, XSR2-1; or XSR1-2, XSR2-2) are turned off, as illustrated in FIG. 6(B), and that the image data is latched by the shift register XSR1-0 or XSR2-0 (or XSR1-1 or XSR2-1; or XSR1-2, XSR2-2).

In the case of a conventional electro-optical device, when the lateral inversion of a display of an image is performed, an external control device needs to change a direction, in which image data is read, by using software. Thus, the conventional electro-optical device has a drawback in that a heavy load is put on the software. However, as a result of applying the signal line drive circuit to the device, the control device has only to generate the signal R/L for controlling the switches SW11 to SW23. Consequently, this embodiment has an advantage in that the load put on the software is considerably lightened.

FIG. 7 illustrates the operation timing of the signal line drive circuit of the embodiment of FIG. 5. As is obvious from the comparison between FIGS. 7 and 2, the signal line drive circuit of the embodiment of FIG. 5 has an advantage in that operations of the shift registers need only one kind of clocks. This is because the signal line drive circuit is controlled in the following manner. Namely, when the clocks CLK, $\overline{CLK}$ are supplied to the shift registers XSR1-0, XSR1-1 and XSR1-2 by using the switches SW41, SW42; and SW43, SW44 for changing the supplying of the clocks, the supplying of clocks to the shift registers XSR2-0, XSR2-1 and XSR2-2 is interrupted. Conversely, when the clocks CLK, $\overline{CLK}$ are supplied to the shift registers XSR2-0, XSR2-1 and XSR2-2, the supplying of clocks to the shift registers XSR1-0, XSR1-1 and XSR1-2 is interrupted. The signal LAT for controlling the data switching/transferring switches SW1-0, SW2-0; SW1-1, SW2-1; SW1-2, SW2-2 may be also used as the signal SW (or $\overline{SW}$) for controlling the switches SW41, SW42; SW43, SW44.

FIG. 8 shows another embodiment of the signal line drive circuit of the present invention. This embodiment is a modification of the signal line drive circuit of the embodiment illustrated in FIG. 1. Namely, the shift registers XSR2-0, XSR2-1 and XSR2-2 of the embodiment of FIG. 1 are replaced with register XLT1-2, XLT2-2 and XLT3-2 that do not have the shifting function. Moreover, the switches

SW1-0, SW2-0; SW1-1, SW2-1; SW1-2 and SW2-2 for switching data are provided between the shift registers XSR1-0, XSR2-0; XSR1-1, XSR2-1; XSR1-2, XSR2-2 and the D/A converters DAC1 to DACn in the embodiment of FIG. 1, while such switches are provided between the shift registers XSR1-1, XSR2-1 and XSR3-1 and the registers XLT1-2, XLT2-2 and XLT3-2 in the second embodiment.

As described above, the second embodiment has the advantage in that the circuit uses only one kind of clock signals for shifting data. However, during the data latched by the shift registers XSR1-1, XSR2-1 and XSR3-1 is transferred to the registers XLT1-2, XLT2-2 and XLT3-2, these shift registers cannot latch new image data. Thus, the latching timing should be changed.

FIG. 9 shows still another embodiment of the signal line drive circuit of the present invention. This embodiment is a modification of the signal line drive circuit of the embodiment of FIG. 5, which is obtained in a manner similar to the way in the case of changing the signal line drive circuit of the embodiment of FIG. 1 to that of the embodiment of FIG. 8. Namely, the shift registers XSR1-2, XSR2-2 and XSR3-2 of the embodiment of FIG. 5 are replaced with the simple registers XLT1-2, XLT2-2 and XLT3-2, respectively. Moreover, the switches SW1-0, SW2-0; SW1-1, SW2-1; SW1-2 and SW2-2 for switching data are provided between the shift registers ZSR1-1, XSR2-1 and XSR3-1 and the registers XLT1-2, XLT2-2 and XLT3-2 in this embodiment, differently from the first embodiment of FIG. 1 in which such switches are provided between the shift registers XSR1-0, XSR2-0; XSR1-1, XSR2-1; XSR1-2, XSR2-2 and the D/A converters DAC1 to DACn in the embodiment of FIG. 1.

The embodiment of FIG. 9 has an advantage in that the number of switches and the number of kinds of control signals are reduced, as compared with the embodiment of FIG. 5. However, during the data latched by the shift registers XSR1-1, XSR2-1 and XSR3-1 is transferred to the registers XLT1-2, XLT2-2 and XLT3-2, these shift registers cannot latch new image data. Thus, the latching timing should be changed, similarly as in the case of the embodiment of FIG. 8.

Although the embodiments of the signal line drive circuit of the present invention in the case of using 3-bit image data have been described above, it should be understood that the present invention is not limited thereto. For example, in the case that the image data is 6-bit data or other single-bit or multi-bit data, the present invention can be applied to the signal line drive circuit. Namely, it is sufficient for the drive circuit to have shift registers of sets of the number that is equal to the number of bits composing the image data.

Next, embodiments of electronic equipment, such as an electro-optical device having a liquid crystal panel substrate using the aforementioned signal line drive circuit, and a portable computer or a liquid crystal projector, which has this electro-optical device, will be described hereinbelow.

As illustrated in FIG. 11, a liquid crystal display device 850 serving as an electro-optical device is constructed by stacking backlights 851, a polarizer 852, a liquid crystal panel substrate (or a TFT substrate) 853, a liquid crystal 854, a counter substrate 855 having a counter electrode and a color filter, and a polarizer 856 in this order. In this embodiment, as described above, a pixel area and the drive circuit 878 of the aforementioned embodiment are formed on a TFT substrate 853.

As illustrated in FIG. 12, a portable computer 860 has a main unit portion 862, which has a keyboard 861, and a liquid crystal display screen 863.

As illustrated in FIG. 13, a liquid crystal projector 870 is a projector that employs a transparent liquid crystal panel as a light valve. This liquid crystal projector 870 has, for example, a triple prism type optical system. In the projector 870 of FIG. 13, projection light irradiated from a lamp unit 871 serving as a white light source is divided by a plurality of mirrors 873 and two dichroic mirrors 874 into component light rays respectively corresponding to primary colors R, G and B in a light guide 872. Such light components are directed to three liquid crystal panels 875, 876 and 877 respectively displaying images of such colors. Then, the component light rays modulated by the liquid crystal panels 875, 876 and 877 are incident on a dichroic prism 878 from three directions. In the dichroic prism 878, the component light rays respectively corresponding to R (red) component light and B (blue) component light are deflected by 90 degrees. On the other hand, G (green) component light travels rectilinearly. A color image is obtained by synthesizing images of such colors and projected on a screen through a projection lens.

Additionally, examples of electronic equipment, to which the present invention can be applied, are an engineering workstation, a pager or a portable telephone, a word processor, a television set, a viewfinder type or direct-view-type camcorder, an electronic pocket notebook, an electronic desk calculator, a car navigation device, a POS (point-of-service) terminal and various devices each having a touch panel.

As described above, the drive circuit of the present invention is configured so that a shift register is used as a circuit for latching image data input from an external circuit. Thus, the length of data lines between an input terminal for inputting image data and a shift register for latching the image data is reduced. Further, in the case of the drive circuit of the present invention, there is no need for considering the timing margin of clocks providing each of latch circuits with the latching timing, differently from the conventional drive circuit. Consequently, image data is input thereto from the external circuit at a high speed. Moreover, the present invention has advantageous effects in that the present invention provides a drive circuit for a liquid crystal display device, which can lower the driving ability of an IC for inputting image data and decrease the power consumption thereof.

Although the preferred embodiments of the present invention have been described above, it should be understood that the present invention is not limited thereto and that other modifications will be apparent to those skilled in the art without departing from the spirit of the invention.

The scope of the present invention, therefore, should be determined solely by the appended claims.

What is claimed is:

1. A drive circuit for an electro-optical device, to which N-bit digital image data is input (N is a positive integer), said drive circuit converting the digital image data to a voltage signal corresponding to one of 2^N gray scales and supply the voltage signal to a signal line, comprising:

a plurality of pairs of shift registers that latch signals respectively representing bits of the image data and for holding the latched signals;

a D/A converter that performs D/A conversion of the image data latched by said shift registers N-bits by N-bits, to generate voltage signals corresponding to 2^N gray scales and to supply the voltage signals to a signal line; and

a switch group that selectively supplies said D/A converter with the image data latched by one of the shift registers of each of the plurality of pairs of shift registers,

said plurality of pairs of shift registers repeatedly and alternatively performing an operation of supplying said D/A converter with image data held by one of the shift registers of each of said plurality of pairs of shift registers when image data is latched by an other one of the shift registers.

2. The drive circuit for an electro-optical device according to claim 1, among switches of said switch group, switches other than a switch for transferring image data held by said shift register closest to said D/A converter being placed between said plurality of pairs of shift registers.

3. The drive circuit for an electro-optical device according to claim 1, further comprising:

a third shift register, provided corresponding to each of said plurality of pairs of shift registers, for latching image data; and

switches provided between said third shift register and a digital image input terminal and between said third shift register and each of said plurality of pairs of shift registers,

said plurality of pairs of shift registers repeatedly and alternately performing an operation of transferring image data to one of the shift registers of each of said plurality of pairs of shift registers after the image data to be transferred is latched by said third shift register from said input terminal by controlling said switches, and supplies said D/A converter with image data held by the other of the shift registers of a corresponding pair during the transferring of image data to the one of the shift registers.

4. The drive circuit for an electro-optical device according to claim 1, further comprising a switch for selectively supplying a shifting clock signal to each of said plurality of pairs of shift registers.

5. A liquid crystal panel substrate comprising:

a drive circuit, to which N-bit digital image data is input (N is a positive integer), said drive circuit converting the digital image data to a voltage signal corresponding to one of 2^N gray scales and supplying the voltage signal to a signal line, said drive circuit having:

a plurality of pairs of shift registers that latch signals respectively representing bits of the image data and for holding the latched signals;

a D/A converter that D/A-converts the image data latch by said shift registers N-bits by N-bits, to generate voltage signals corresponding to 2^N gray scales and to supply the voltage signals to a signal line; and

a switch group that selectively supplies said D/A converter with the image data latched by one of the shift registers of each of the plurality of pairs of shift registers,

said plurality of pairs of shift registers repeatedly and alternately performing an operation of supplying said D/A converter with image data held by one of the shift registers of each of said plurality of pairs of shift registers when image data is latched by an other one of the shift registers; and

a pixel area having:

a plurality of pixel electrodes;

signal lines that supply voltages to be applied to said plurality of pixel electrodes; and

scanning lines for selecting pixels to which the voltages are applied,

said drive circuit supplying said signal lines with voltages respectively corresponding to image data.

6. The liquid crystal panel substrate according to claim 5, among switches of said switch group, switches other than a switch for transferring image data held by said shift register closest to said D/A converter being placed between said plurality of pairs of shift registers.

7. The liquid crystal panel substrate according to claim 5, further comprising:

a third shift register, provided corresponding to each of said plurality of pairs of shift registers, for latching image data; and

switches provided between said third shift register and a digital image input terminal and between said third shift register and each of said plurality of pairs of shift registers,

said plurality of pairs of shift registers repeatedly and alternately performing an operation of transferring image data to one of the shift registers of each of said plurality of pairs of shift registers after the image data to be transferred is latched by said third shift register from said input terminal by controlling said switches, and supplies said D/A converter with image data held by the other of the shift registers of a corresponding pair during the transferring of image data to the one of the shift registers.

8. The liquid crystal panel substrate according to claim 5, further comprising a switch for selectively supplying a shifting clock signal to each of said plurality of pairs of shift registers.

9. A liquid crystal device comprising:

a liquid crystal panel substrate having:

a drive circuit, to which N-bit digital image data is input (N is a positive integer), said drive circuit converting the digital image data to a voltage signal corresponding to one of 2^N gray scales and supplying the voltage signal to a signal line, said drive circuit having:

a plurality of pairs of shift registers that latch signals respectively representing bits of the image data and for holding the latched signals;

a D/A converter that D/A-converts the image data latched by said shift registers N-bits by N-bits, to generate voltage signals corresponding to 2^N gray scales and to supply the voltage signals to a signal line; and

a switch group that selectively supplies said D/A converter with the image data latched by one of the shift registers of each of the plurality of pairs of shift registers,

said plurality of pairs of shift registers repeatedly and alternately performing an operation of supplying said D/A converter with image data held by one of the shift registers of each of said plurality of pairs of shift registers when image data is latched by an other one of the shift registers; and

a pixel area having:

a plurality of pixel electrodes;

signal lines that supply voltages to be applied to said plurality of pixel electrodes; and

scanning lines for selecting pixels to which the voltages are applied,

said drive circuit supplying said signal lines with voltages respectively corresponding to image data; and

a transparent substrate having a counter electrode,

said liquid crystal panel substrate and said transparent substrate being placed at a distance from each other, and

a gap between said liquid crystal panel substrate and said transparent substrate being filled with liquid crystal.

10. The liquid crystal device according to claim 9, among switches of said switch group, switches other than a switch for transferring image data held by said shift register closest to said D/A converter being placed between said plurality of pairs of shift registers.

11. The liquid crystal device according to claim 9, further comprising:

a third shift register, provided corresponding to each of said plurality of pairs of shift registers, for latching image data; and

switches provided between said third shift register and a digital image input terminal and between said third shift register and each of said plurality of pairs of shift registers,

said plurality of pairs of shift registers repeatedly and alternately performing an operation of transferring image data to one of the shift registers of each of said plurality of pairs of shift registers after the image data to be transferred is latched by said third shift register from said input terminal by controlling said switches, and supplies said D/A converter with image data held by the other of the shift registers of a corresponding pair during the transferring of image data to the one of the shift registers.

12. The liquid crystal device according to claim 9, further comprising a switch for selectively supplying a shifting clock signal to each of said plurality of pairs of shift registers.

13. A projection display device, comprising:

a light source;

a liquid crystal panel; and

a projection optical device that collects light modulated by said liquid crystal panel and projecting the modulated light in an enlarged manner, said liquid crystal panel including:

a liquid crystal panel substrate having:

a drive circuit, to which N-bit digital image data is input (N is a positive integer), said drive circuit converting the digital image data to a voltage signal corresponding to one of 2^N gray scales and supplying the voltage signal to a signal line, said drive circuit having:

a plurality of pairs of shift registers that latch signals respectively representing bits of the image data and for holding the latched signals;

a D/A converter that D/A-converts the image data latched by said shift registers N-bits by N-bits, to generate voltage signals corresponding to 2^N gray scales and to supply the voltage signals to a signal line; and

a switch group that selectively supplies said D/A converter with the image data latched by one of the shift registers of each of the plurality of pairs of shift registers,

said plurality of pairs of shift registers repeatedly and alternately performing an operation of supplying said D/A converter with image data held by one of the shift registers of each of said plurality of pairs of shift registers when image data is latched by an other one of the shift registers; and

a pixel area having:

a plurality of pixel electrodes;

signal lines that supply voltages to be applied to said plurality of pixel electrodes; and

scanning lines for selecting pixels to which the voltages are applied,

said drive circuit supplying said signal lines with voltages respectively corresponding to image data; and

a transparent substrate having a counter electrode,

said liquid crystal panel substrate and said transparent substrate being placed at a distance from each other, and

a gap between said liquid crystal panel substrate and said transparent substrate being filled with liquid crystal.

14. The projection display device according to claim 13, among switches of said switch group, switches other than a switch for transferring image data held by said shift register closest to said D/A converter being placed between said plurality of pairs of shift registers.

15. The projection display device according to claim 13, further comprising:

a third shift register, provided corresponding to each of said plurality of pairs of shift registers, for latching image data; and

switches provided between said third shift register and a digital image input terminal and between said third shift register and each of said plurality of pairs of shift registers,

said plurality of pairs of shift registers repeatedly and alternately performing an operation of transferring image data to one of the shift registers of each of said plurality of pairs of shift registers after the image data to be transferred is latched by said third shift register from said input terminal by controlling said switches, and supplies said D/A converter with image data held by the other of the shift registers of a corresponding pair during the transferring of image data to the one of the shift registers.

16. The projection display device according to claim 13 further comprising a switch for selectively supplying a shifting clock signal to each of said plurality of pairs of shift registers.

17. An electro-optical device having a liquid crystal panel for displaying an image thereon, said liquid crystal panel comprising:

a liquid crystal panel substrate having:

a drive circuit, to which N-bit digital image data is input (N is a positive integer), said drive circuit converting the digital image data to a voltage signal corresponding to one of 2^N gray scales and supplying the voltage signal to a signal line, said drive circuit having:

a plurality of pairs of shift registers that latch signals respectively representing bits of the image data and for holding the latched signals;

a D/A converter that D/A-converts the image data latched by said shift registers N-bits by N-bits, to generate voltage signals corresponding to 2^N gray scales and to supply the voltage signals to a signal line; and

a switch group that selectively supplies said D/A converter with the image data latched by one of the shift registers of each of the plurality of pairs of shift registers,

said plurality of pairs of shift registers repeatedly and alternately performing an operation of supplying said D/A converter with image data held by one of the shift registers of each of said plurality of pairs of shift registers when image data is latched by an other on of the shift registers; and

a pixel area having:

a plurality of pixel electrodes;

signal lines that supply voltages to be applied to said plurality of pixel electrodes; and

scanning lines for selecting pixels to which the voltages are applied,

said drive circuit supplying said signal lines with voltages respectively corresponding to image data; and

a transparent substrate having a counter electrode,

said liquid crystal panel substrate and said transparent substrate being placed at a distance from each other, and

a gap between said liquid crystal panel substrate and said transparent substrate being filled with liquid crystal.

18. The electro-optical device according to claim **17**, among switches of said switch group, switches other than a switch for transferring image data held by said shift register closest to said D/A converter being placed between said plurality of pairs of shift registers.

19. The electro-optical device according to claim **17**, further comprising:

a third shift register, provided corresponding to each of said plurality of pairs of shift registers, for latching image data; and

switches provided between said third shift register and a digital image input terminal and between said third shift register and each of said plurality of pairs of shift registers,

said plurality of pairs of shift registers repeatedly and alternately performing an operation of transferring image data to one of the shift registers of each of said plurality of pairs of shift registers after the image data to be transferred is latched by said third shift register from said input terminal by controlling said switches, and supplies said D/A converter with image data held by the other of the shift registers of a corresponding pair during the transferring of image data to the one of the shift registers.

20. The electro-optical device according to claim **17** further comprising a switch for selectively supplying a shifting clock signal to each of said plurality of pairs of shift registers.

21. Electronic equipment including an electro-optical device, said electro-optical device having a liquid crystal panel for displaying an image thereon, said liquid crystal panel comprising:

a liquid crystal panel substrate having:

a drive circuit, to which N-bit digital image data is input (N is a positive integer), said drive circuit converting the digital image data to a voltage signal corresponding to one of 2^N gray scales and supplying the voltage signal to a signal line, said drive circuit having:

a plurality of pairs of shift registers that latch signals respectively representing bits of the image data and for holding the latched signals;

a D/A converter that D/A-converts the image data latched by said shift registers N-bits by N-bits, to generate voltage signals corresponding to 2^N gray scales and to supply the voltage signals to a signal line; and

a switch group that selectively supplies said D/A converter with the image data latched by one of the shift registers of each of the plurality of pairs of shift registers,

said plurality of pairs of shift registers repeatedly and alternately performing an operation of supplying said D/A converter with image data held by one of the shift registers of each of said plurality of pairs of shift registers when image data is latched by an other on of the shift registers; and

a pixel area having:

a plurality of pixel electrodes;

signal lines that supply voltages to be applied to said plurality of pixel electrodes; and

scanning lines for selecting pixels to which the voltages are applied,

said drive circuit supplying said signal lines with voltages respectively corresponding to image data; and

a transparent substrate having a counter electrode,

said liquid crystal panel substrate and said transparent substrate being placed at a distance from each other, and

a gap between said liquid crystal panel substrate and said transparent substrate being filled with liquid crystal.

22. The electronic equipment according to claim **21**, among switches of said switch group, switches other than a switch for transferring image data held by said shift register closest to said D/A converter being placed between said plurality of pairs of shift registers.

23. The electronic equipment according to claim **21**, further comprising:

a third shift register, provided corresponding to each of said plurality of pairs of shift registers, for latching image data; and

switches provided between said third shift register and a digital image input terminal and between said third shift register and each of said plurality of pairs of shift registers,

said plurality of pairs of shift registers repeatedly and alternately performing an operation of transferring image data to one of the shift registers of each of said plurality of pairs of shift registers after the image data to be transferred is latched by said third shift register from said input terminal by controlling said switches, and supplies said D/A converter with image data held by the other of the shift registers of a corresponding pair during the transferring of image data to the one of the shift registers.

24. The electronic equipment according to claim **21**, further comprising a switch for selectively supplying a shifting clock signal to each of said plurality of pairs of shift registers.

* * * * *

US006111557A

United States Patent [19]

Koyama et al.

[11] Patent Number: 6,111,557

[45] Date of Patent: Aug. 29, 2000

[54] **DISPLAY DEVICE AND METHOD OF DRIVING DISPLAY DEVICE**

[75] Inventors: **Jun Koyama**; **Hisashi Ohtani**, both of Kanagawa, Japan

[73] Assignee: **Semiconductor Energy Laboratory Co., Ltd.**, Japan

[21] Appl. No.: **08/999,347**

[22] Filed: **Dec. 29, 1997**

[30] **Foreign Application Priority Data**

Dec. 30, 1996 [JP] Japan 8-358951

[51] **Int. Cl.**[7] **G09G 3/36**

[52] **U.S. Cl.** **345/89**; 345/147; 345/100

[58] **Field of Search** 345/89, 147, 148, 345/94, 95, 92, 100, 204, 971

[56] **References Cited**

U.S. PATENT DOCUMENTS

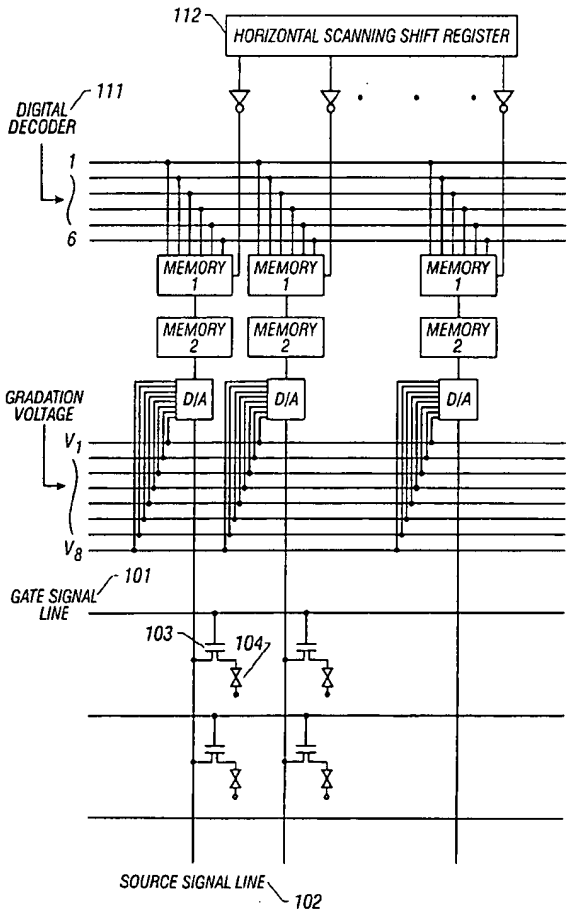
5,051,739	9/1991	Hayashida et al.	345/90
5,168,270	12/1992	Masumori	345/100
5,663,744	9/1997	Seike et al.	345/95
5,745,089	4/1998	Taguchi et al.	345/89
5,828,357	10/1998	Tamai et al.	345/89

Primary Examiner—Steven J. Saras
Assistant Examiner—Fritz Alphonse
Attorney, Agent, or Firm—Fish & Richardson P.C.

[57] **ABSTRACT**

A structure of an active matrix liquid crystal display device for carrying out gradation display with a digital picture signal being input is simplified. In order to carry out display of multilevel gradation, for example, 64 levels of gradation, eight kinds of gradation voltage in eight periods obtained by dividing one line period are selected. Here, information with regard to the eight kinds of gradation voltage and information with regard to the eight kinds of selection timing are supplied to digital decoders. Based on the information, gradation voltage is selected according to predetermined timing. By this, 64 levels of gradation can be displayed. Since, in this structure, there are only eight levels of gradation voltage in one timing, the structure of the circuit can be simplified.

17 Claims, 10 Drawing Sheets



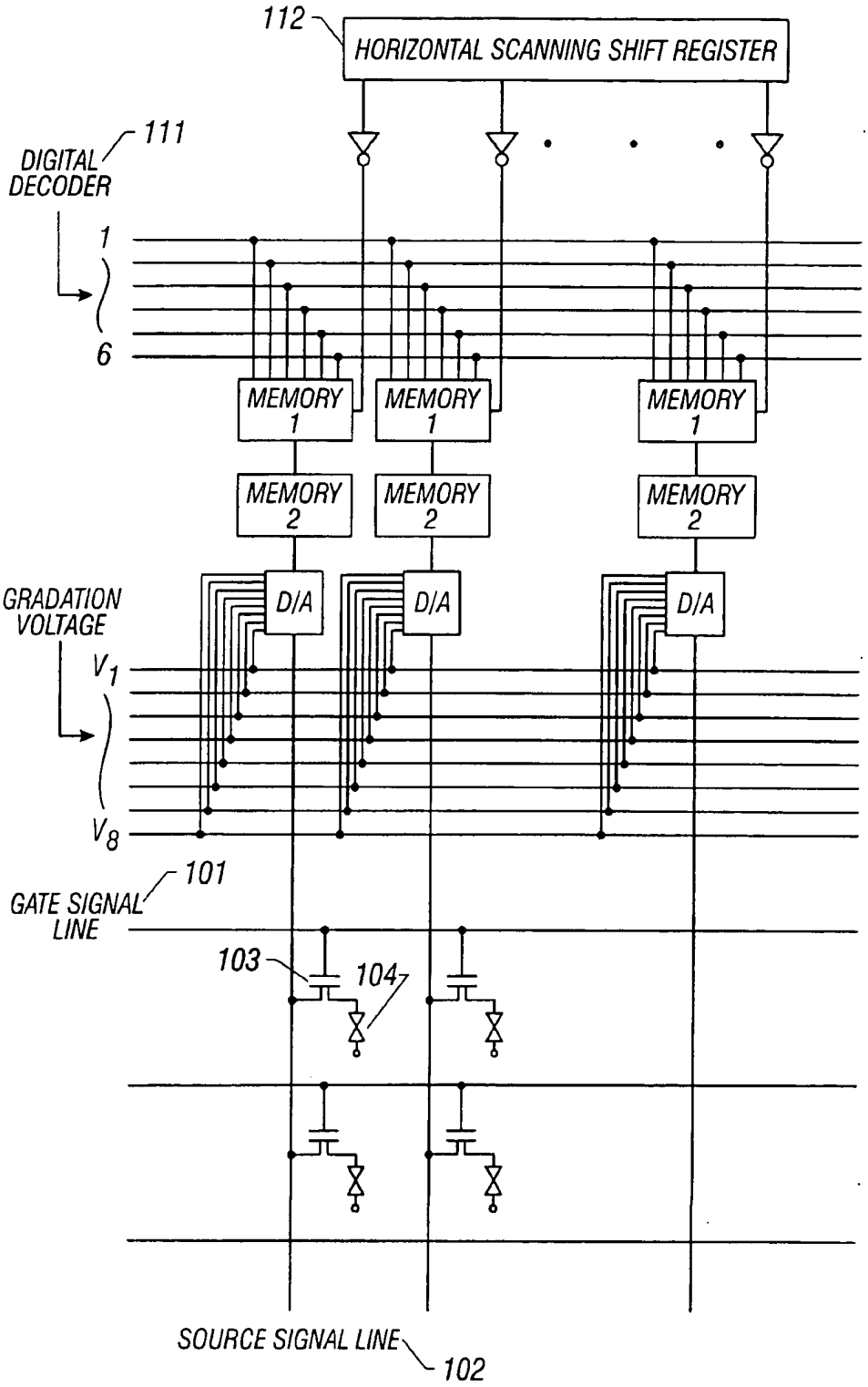

112
HORIZONTAL SCANNING SHIFT REGISTER
111
DIGITAL DECODER
1
6
MEMORY 1
MEMORY 1
MEMORY 1
MEMORY 2
MEMORY 2
MEMORY 2
D/A
D/A
D/A
GRADATION VOLTAGE
V_1
V_8
101
GATE SIGNAL LINE
103
104
SOURCE SIGNAL LINE
102

FIG. 1

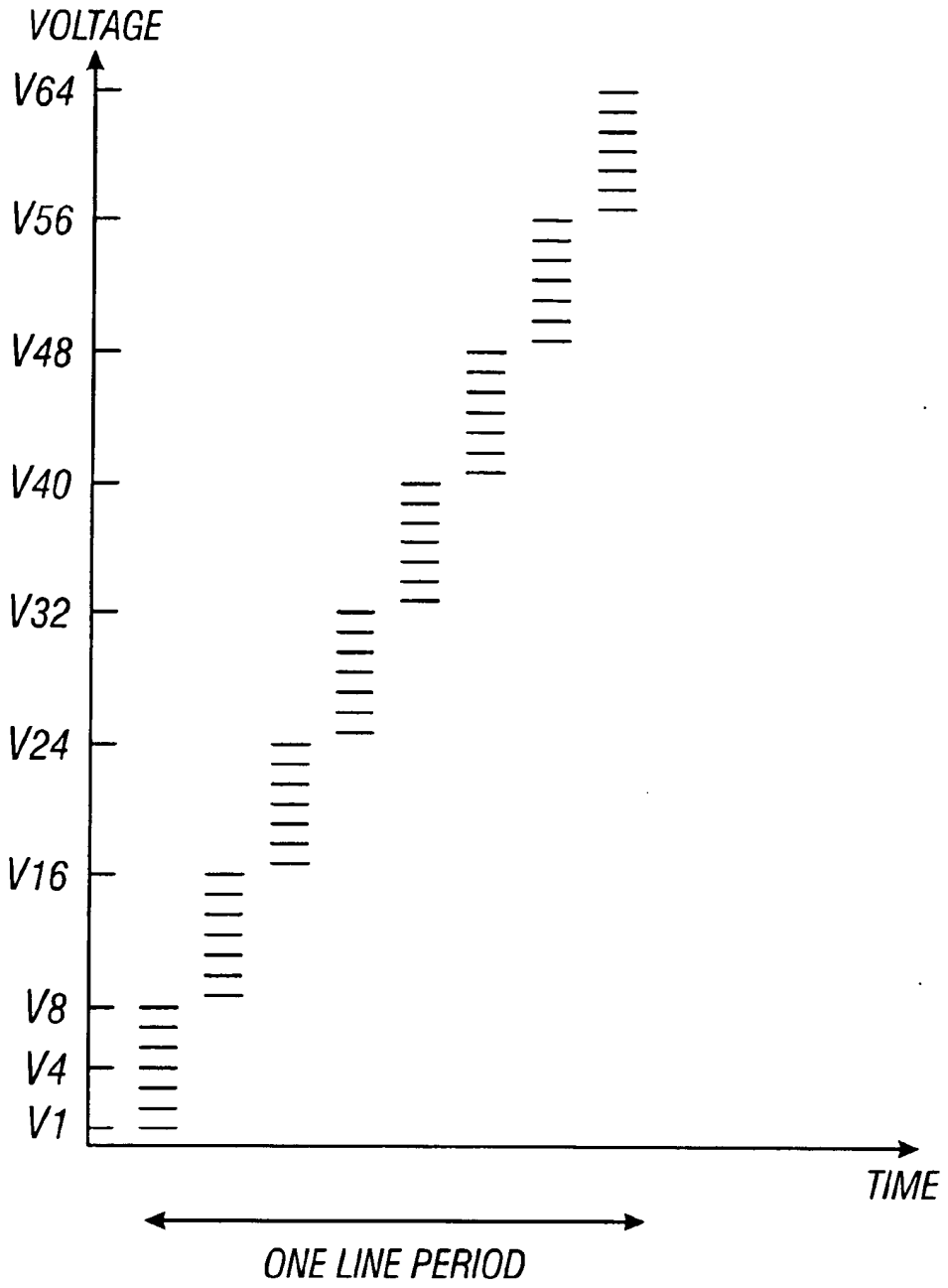

VOLTAGE
V64
V56
V48
V40
V32
V24
V16
V8
V4
V1
TIME
ONE LINE PERIOD

FIG. 2

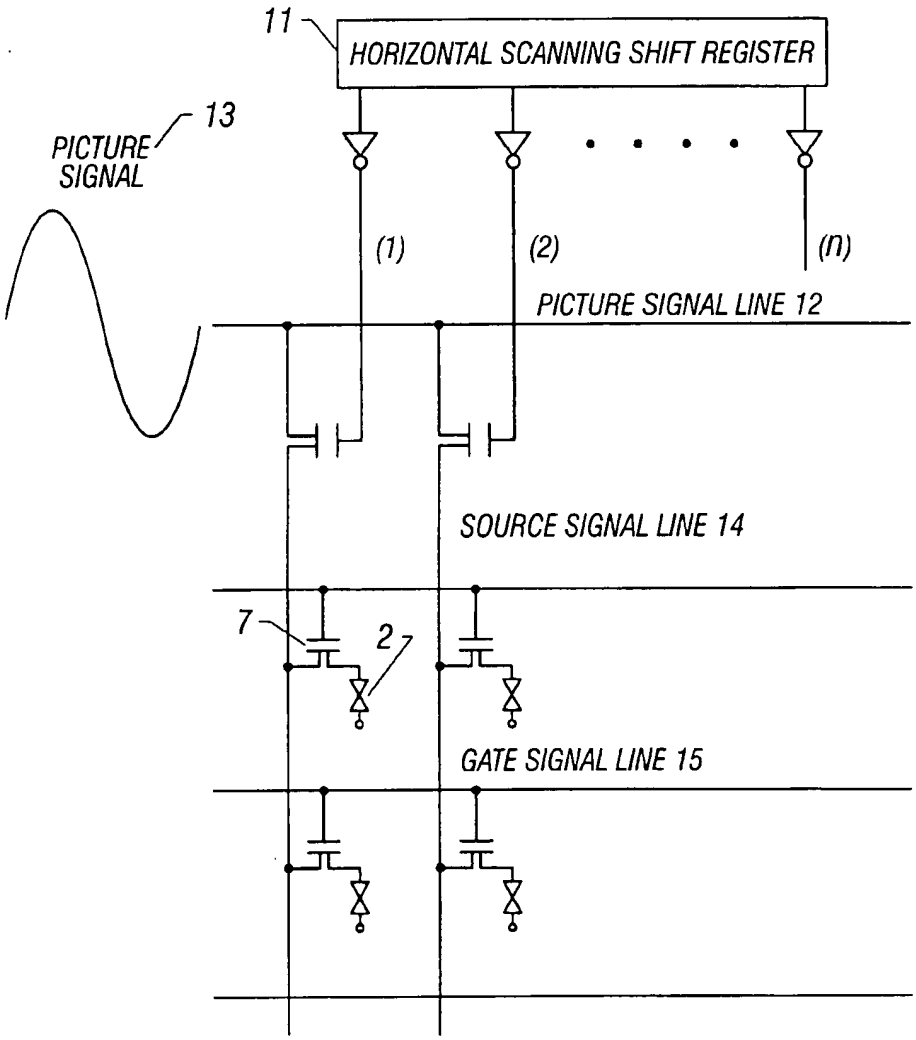

11
HORIZONTAL SCANNING SHIFT REGISTER
13
PICTURE SIGNAL
(1)
(2)
(n)
PICTURE SIGNAL LINE 12
SOURCE SIGNAL LINE 14
7
2
GATE SIGNAL LINE 15

FIG. 3A

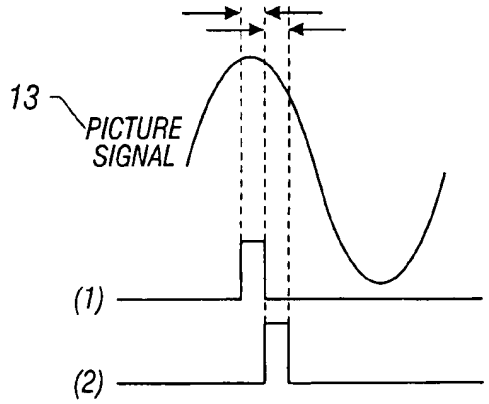

13
PICTURE SIGNAL
(1)
(2)

FIG. 3B

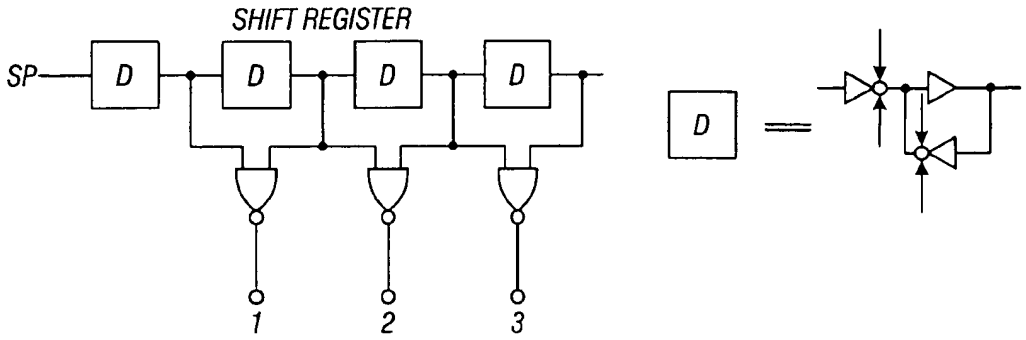

SHIFT REGISTER
SP
D
D
D
D
1
2
3
D

FIG. 4

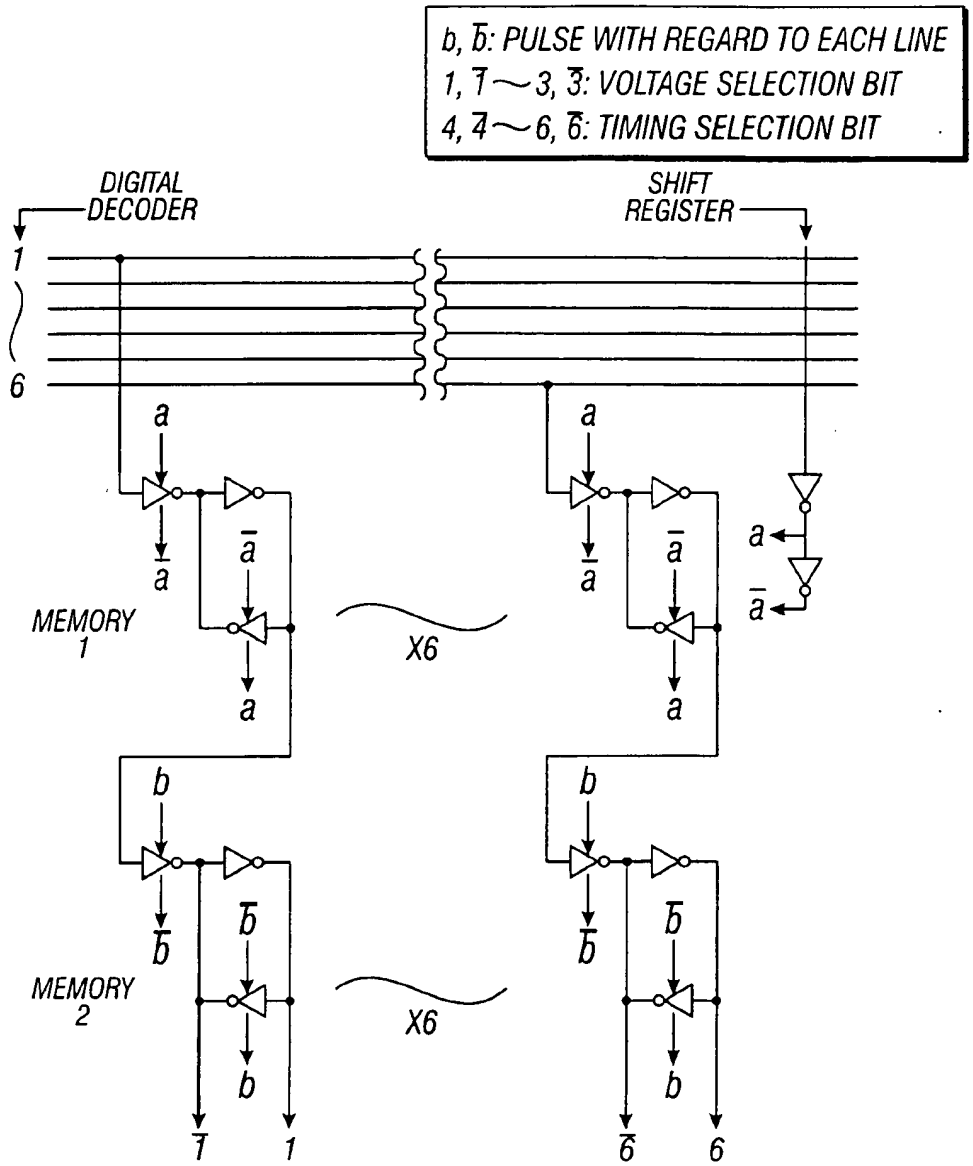

b, b̄: PULSE WITH REGARD TO EACH LINE
1, 1̄ ~ 3, 3̄: VOLTAGE SELECTION BIT
4, 4̄ ~ 6, 6̄: TIMING SELECTION BIT
DIGITAL DECODER
SHIFT REGISTER
1
6
a
ā
MEMORY 1
X6
b
b̄
MEMORY 2
X6
1̄
1
6̄
6

FIG. 5

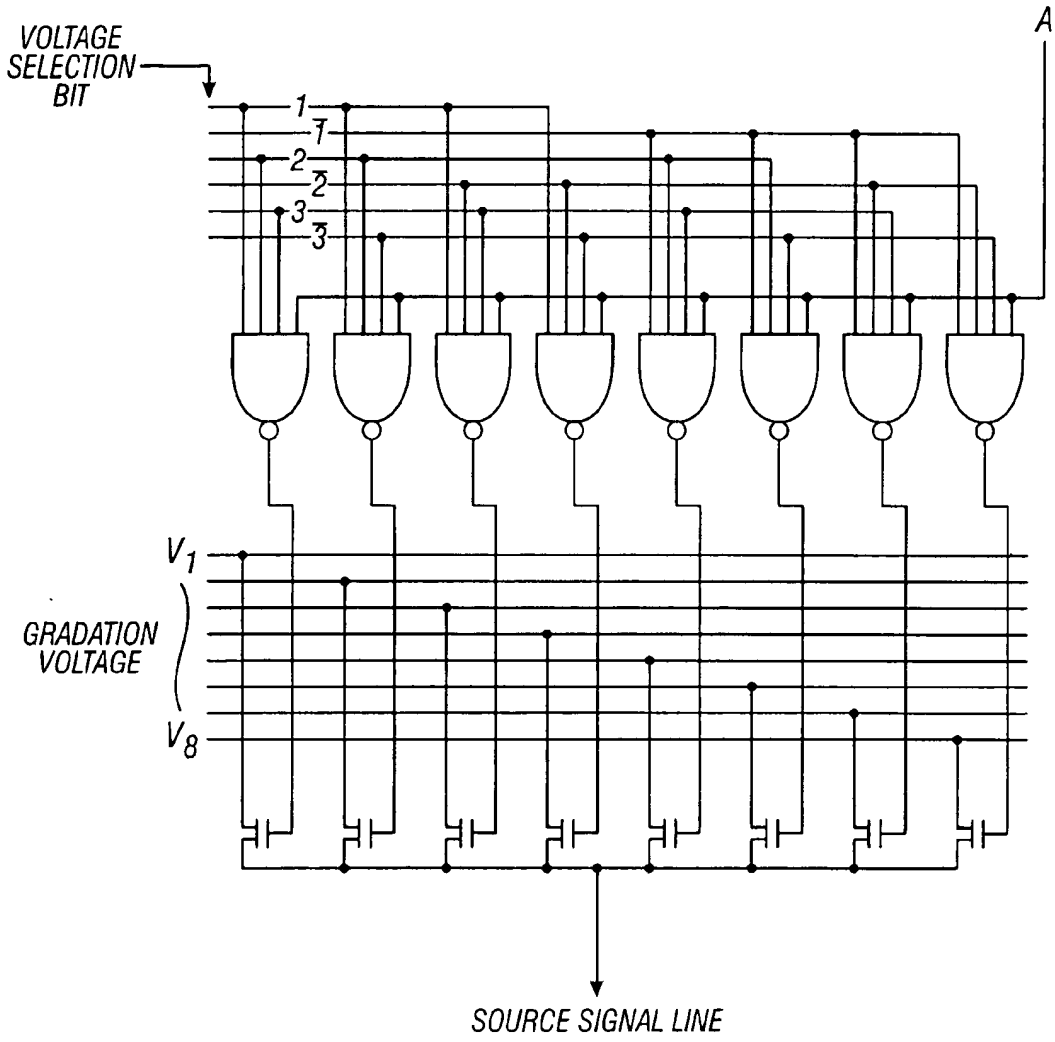

VOLTAGE SELECTION BIT
A
1
1̄
2
2̄
3
3̄
V1
GRADATION VOLTAGE
V8
SOURCE SIGNAL LINE

FIG. 6

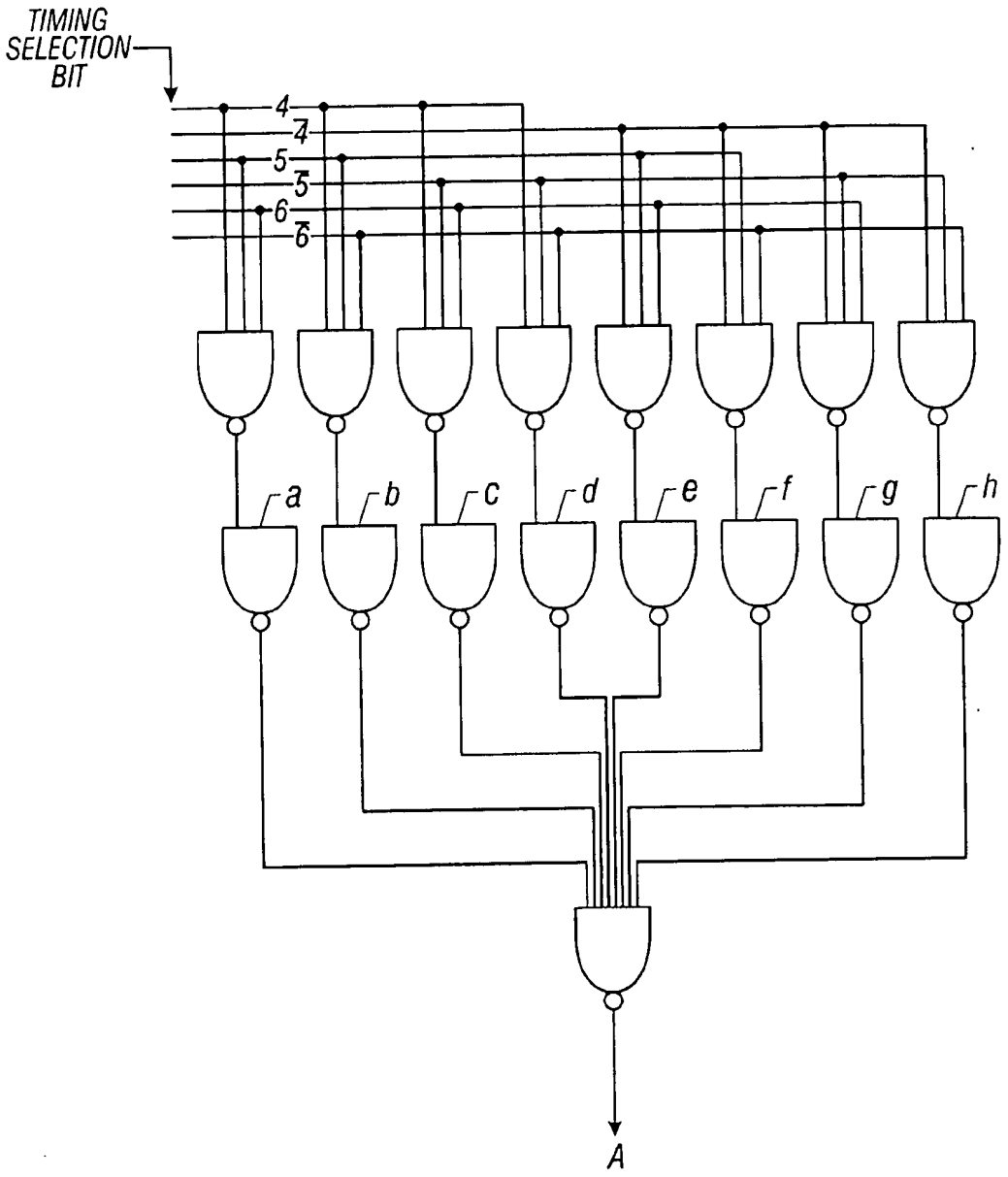

TIMING
SELECTION
BIT
4
$\overline{4}$
5
$\overline{5}$
6
$\overline{6}$
a
b
c
d
e
f
g
h
A

FIG. 7

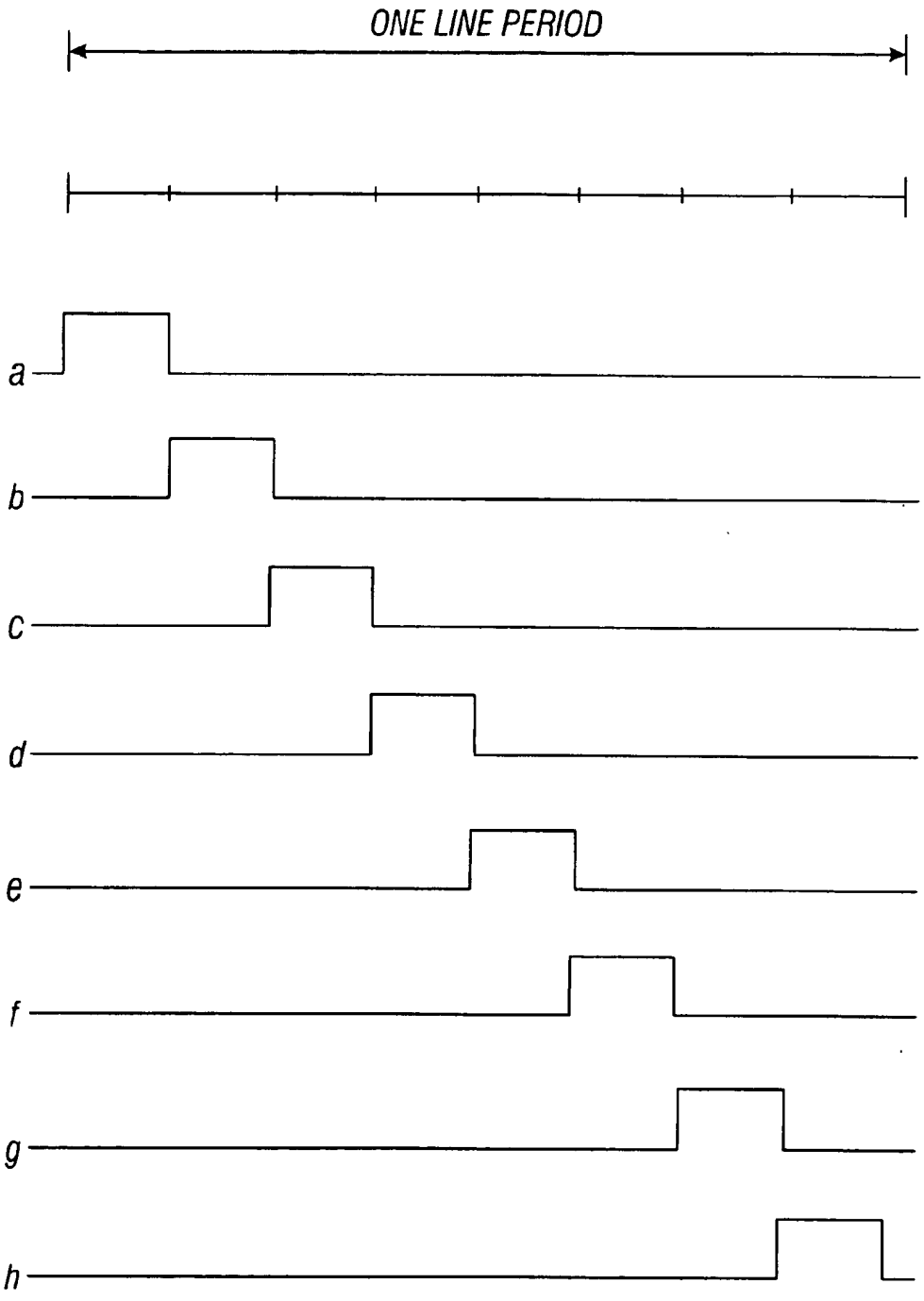


FIG. 8

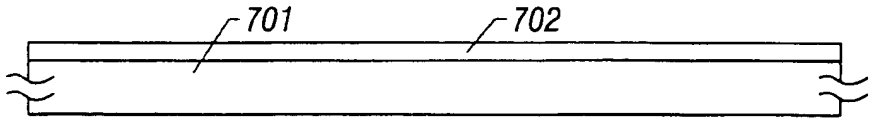


FIG. 9A

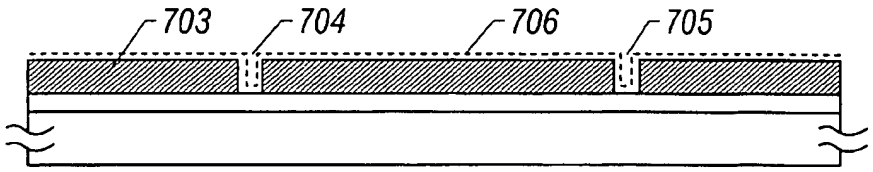


FIG. 9B

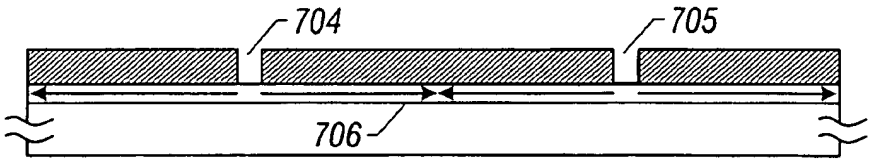


FIG. 9C

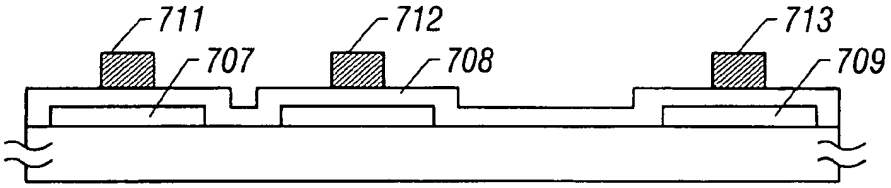


FIG. 9D

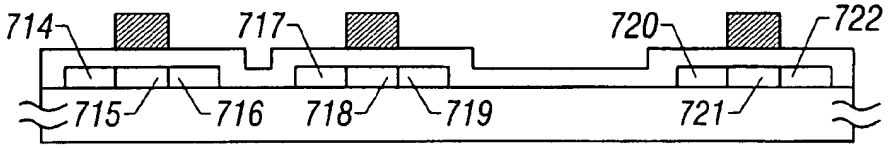


FIG. 9E

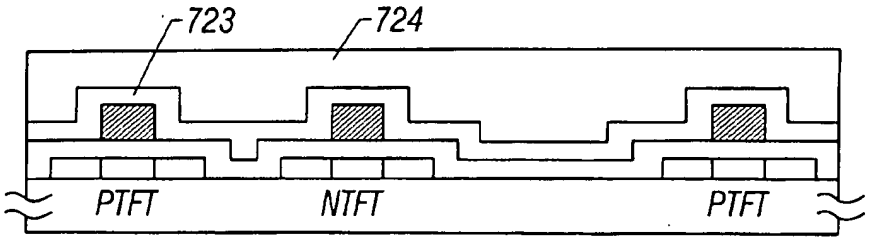


FIG. 9F

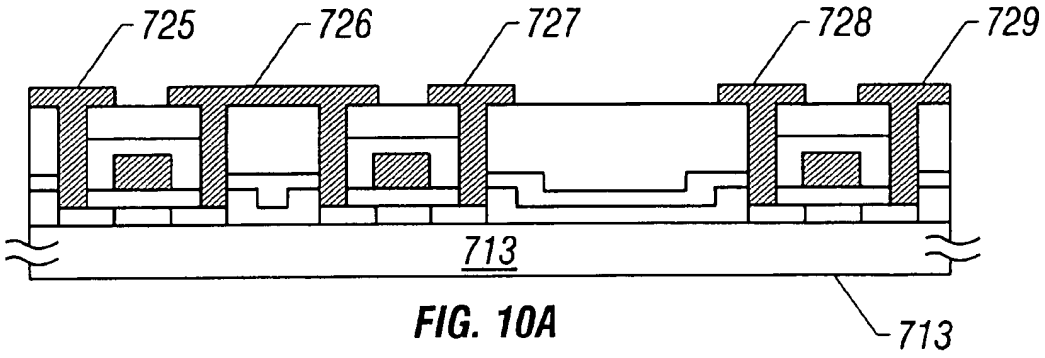


FIG. 10A

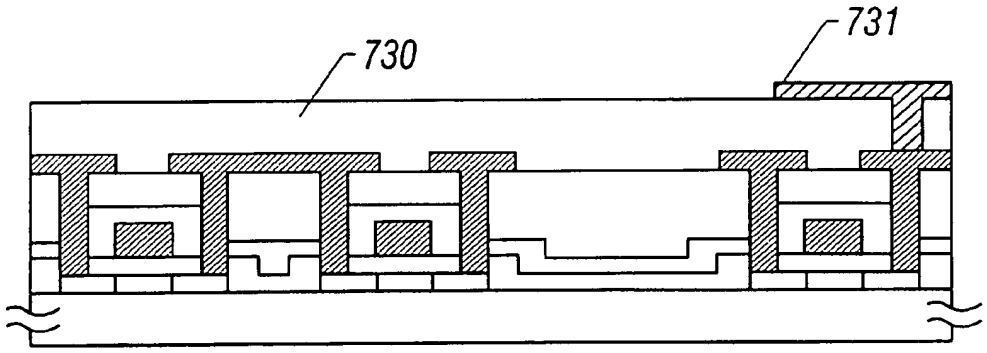


FIG. 10B

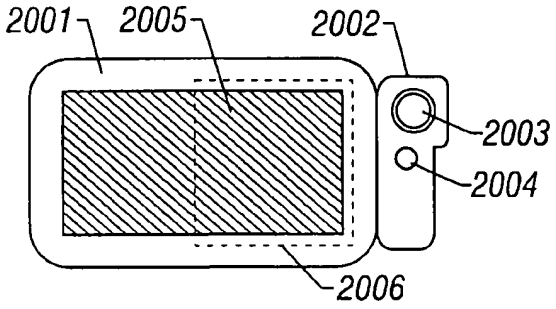


FIG. 11A

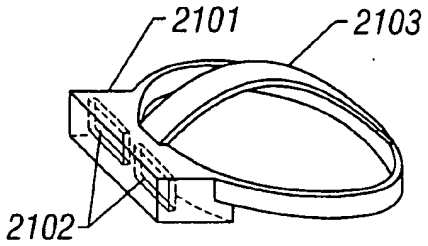


FIG. 11B

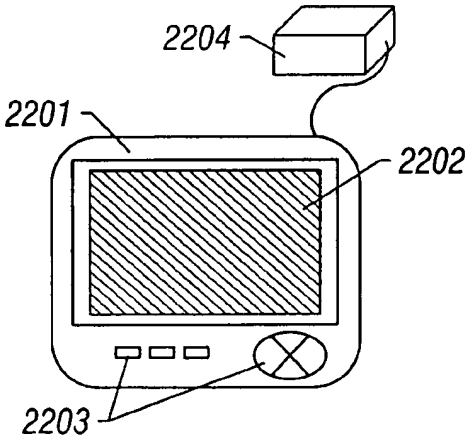


FIG. 11C

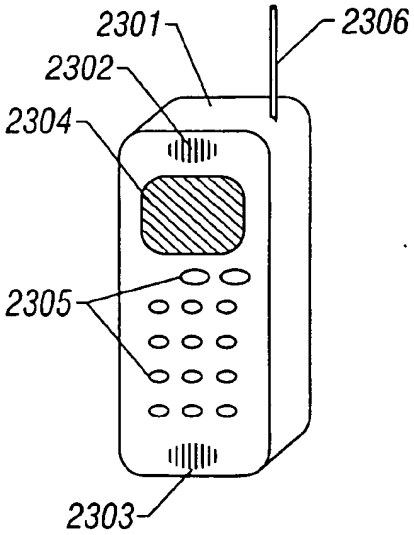


FIG. 11D

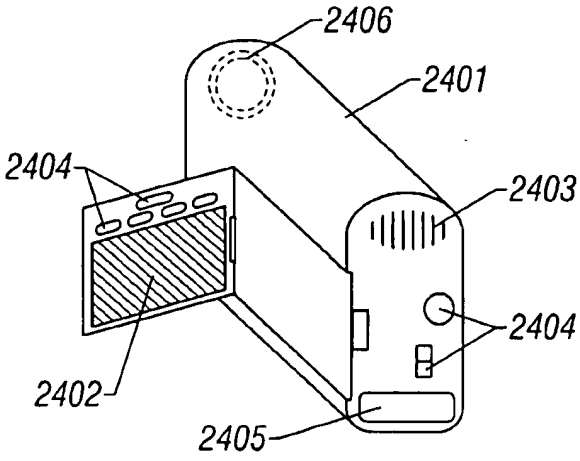


FIG. 11E

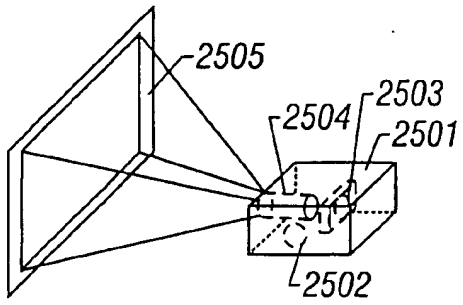


FIG. 11F

DISPLAY DEVICE AND METHOD OF DRIVING DISPLAY DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a display device which displays an image by pixels disposed so as to be in a matrix. For example, the invention disclosed herein is applicable to an active matrix liquid crystal display device and an EL (electro-luminescent) display.

2. Description of the Related Art

Conventionally, active matrix liquid crystal display devices have been known. Such a display device is structured such that thin film transistors for switching are disposed for respective pixel electrodes disposed in a matrix of several hundreds x several hundreds or more, and that electric charge retained at the respective pixel electrodes is controlled by the thin film transistors.

In order to display a picture of high quality, how finely gradation display can be carried out is important.

FIG. 3 illustrates a structure of a classical active matrix liquid crystal display device. A shift register and a buffer circuit generally referred to as a peripheral driving circuit are formed by disposing exterior type IC circuits on a substrate.

Further, thin film transistors **1** utilizing amorphous semiconductor formed on a glass substrate are disposed with regard to the respective pixels in the active matrix circuit. A liquid crystal cell **2** comprising a pixel electrode, liquid crystal, and a counter electrode is connected with each of the thin film transistors **1**.

Another structure is also known in which quartz is utilized as a substrate and a thin film transistor is formed with a crystalline semiconductor film. In this case, both the peripheral driving circuit and the active matrix circuit comprising thin film transistors formed on a quartz substrate.

Still a technique is also known that a thin film transistor is formed with a crystalline semiconductor film on a glass substrate by utilizing such as laser annealing. Such a technique makes it possible to integrate the active matrix circuits and the peripheral driving circuit on a glass substrate.

In a structure as shown in FIG. **3**, by a signal from a shift register circuit **11** of a source driver (a shift register for horizontal scanning), a picture signal **13** to be supplied to a picture signal line **12** is selected according to timing shown in FIG. **3**B. Then, a predetermined picture signal is supplied to a corresponding source signal line **14**.

The picture signal **13** supplied to the source signal line **14** is selected by the thin film transistor **1** to be written in a predetermined pixel electrode.

The thin film transistor is operated according to a selection signal supplied via a gate signal line **15** from a shift register of a gate driver (a shift register for vertical scanning) which is not shown.

By sequentially and repeatedly carrying out the abovementioned operation according to appropriately set timing based on signals from the shift register **11** of the source driver and from the shift register of the gate driver, information is sequentially written to the respective pixels disposed so as to be in a matrix.

After pixel information for one picture is written, pixel information for the subsequent picture is written. In this way, pictures are displayed one after another. Typically, writing of information for one picture is carried out 30 times or 60 times per second.

In such operation, in order to carry out gradation display, a picture signal is required to include a signal corresponding to the necessary gradation.

In case a signal supplied to the device is an analog signal, since the signal includes a signal necessary for gradation display, even the structure shown in FIG. **3**A can accommodate gradation display to some extent.

However, in case display is carried out based on a digital signal from a magnetic recording medium, a digital circuit or the like, a problem arises with the structure shown in FIG. **3**A.

In case the base signal is digital, an analog picture signal as shown in FIG. **3**B must be produced by a D/A converter.

The number of levels of gradation necessary for a portable information processing terminal or the like is 64 or more. However, if a picture signal including information for 64 levels of gradation is to be produced by a D/A converter, there is a problem that the structure of the D/A converter is required to be complicated, which leads to higher cost.

Especially in case the display device is highly integrated, the D/A converter is also required to be formed on a panel with a thin film transistor. However, it is very difficult to form the D/A converter for producing information for 64 levels of gradation as described above by using a thin film transistor.

For example, suppose the XGA standard (1024×768 pixels) is adopted to write a picture 60 times per second. In this case, it takes ((1/60)/768) sec, i.e., 21.7 μsec to sequentially supply a signal from the first to the 1024th source signal lines in one line.

Further, time period from a time when a shift register of the n th stage starts its operation to a time when a shift register of the (n+1) th stage starts its operation is 1/1024 thereof, i.e., 21.2 μnsec, which means that the operation speed of 47 MHz or more is required.

Even just to produce an analog signal corresponding to 64 levels of gradation at an operating speed of about 47 MHz is burdensome for a D/A converter. Thus, it goes without saying that it is very difficult to form a D/A converter having such ability with a thin film transistor.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the invention disclosed herein to provide a structure of an active matrix type display device for displaying a picture with a digital signal being as an input signal, which can carry out gradation display of 64 levels or more with a relatively simple circuit structure.

According to one aspect of the present invention, an active matrix type display device comprises:

- gate signal lines and source signal lines disposed so as to be lattice;
- at least one thin film transistor disposed around intersections of the gate signal lines and source signal lines; and
- means for selecting gradation voltage to be supplied to the source signal lines provided for each of the source signal lines,
- wherein selection of gradation voltage by the means for selecting gradation voltage is carried out by selecting one among a plurality of divided periods obtained by dividing one line period and by selecting gradation voltage set in each of the divided periods.

A specific example of the structure as described above is shown in FIG. **1**. In the structure shown in FIG. **1**, as the means for selecting gradation voltage, a memory **1** and a

memory 2 for taking in information on gradation voltage to be selected and then supplied to a digital decoder, and a D/A converter for selecting voltage are shown.

In the structure as described above, gradation voltage to be supplied to the source signal lines is selected among the product of the number N of the divided periods of one line period and the number M of gradation voltage levels set in each divided period of one line period (N×M).

For example, FIG. 2 shows timing for supplying gradation voltage to be selected by a D/A converter in case one line period is divided into eight periods and voltage to be supplied to the source signal line is selected among eight levels of gradation voltage set in each divided period.

In case the timing for supplying gradation voltage shown in FIG. 2 is adopted, 8×8=64 levels of gradation display can be displayed.

In the structure as described above, the time required for the thin film transistor disposed in the pixel to write information to the pixel electrode must be shorter than the length of one divided period.

In the structure as described above, the means for selecting gradation voltage is controlled by:

information with regard to which period is to be selected among the periods set by dividing one line period; and

information with regard to which gradation voltage level is to be selected among the plurality of gradation voltage levels set in the selected divided period, and

selection of a predetermined level of gradation voltage according to predetermined timing.

According to another aspect of the present invention, an active matrix type display device comprises:

gate signal lines and source signal lines disposed so as to be lattice;

at least one thin film transistor disposed around intersections of the gate signal lines and source signal lines; and

means for selecting gradation voltage to be supplied to the source signal lines provided for each of the source signal lines, wherein:

selection of gradation voltage by the means is carried out by selecting one period set by dividing one line period into N sections and by selecting among M gradation voltage levels set in the period;

gradation voltage to be supplied to the source signal lines is selected among the product of the number N of the divided periods of one line period by the number M of gradation voltage levels set in one period set by dividing one line period into N portions (N×M);

the thin film transistor has a function to write picture information to a pixel electrode; and

the time required for the thin film transistor to write information is shorter than the length of one period set by dividing one line period into N sections.

In the structure as described above, the means for selecting gradation voltage is controlled by:

information with regard to which period is to be selected among the periods set by dividing one line period into N sections; and

information with regard to which gradation voltage level is to be selected among M gradation voltage levels set in the period set by the division into N sections.

According to still another aspect of the present invention, a method of driving a display device with a pixel matrix comprising a plurality of gate signal lines and a plurality of source signal lines disposed so as to be lattice over a substrate, and further, at least one thin film transistor disposed, over the substrate, around intersections of the gate signal lines and source signal lines is characterized in that selection of gradation voltage to be supplied to the plurality of source lines is carried out by selecting one period set by dividing one line period into a plurality of sections and by selecting a voltage level set in the one period.

In the structure as described above, the operating time of the thin film transistor must be shorter than the length of the one period set by dividing the one line period into a plurality of sections.

This is because the time required to write necessary gradation information to a pixel electrode is limited within a period obtained by dividing one line period.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a schematic structure of an active matrix liquid crystal display device as an embodiment of the present invention;

FIG. 2 illustrates relationship between supplied gradation voltage and timing for supplying it;

FIGS. 3A–3B illustrates a schematic structure of a conventional active matrix liquid crystal display device;

FIG. 4 schematically illustrates a shift register circuit;

FIG. 5 schematically illustrates memory circuits;

FIG. 6 schematically illustrates a D/A converter circuit;

FIG. 7 schematically illustrates the D/A converter circuit;

FIG. 8 illustrates timing for supplying a signal to the D/A converter circuit;

FIGS. 9A–9F illustrates a manufacturing process of a thin film transistor;

FIGS. 10A–10B illustrates the manufacturing process of a thin film transistor; and

FIGS. 11A–11F illustrates examples of units utilizing an active matrix liquid crystal display device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the present invention is now described taking as an example an active matrix liquid crystal device shown in FIG. 1.

Information supplied to digital decoders 1–6 which is a combination of a selection signal with regard to eight levels of gradation and a selection signal with regard to eight kinds of timing (8^2=64 kinds of information) is sequentially written to a group of memories 1 according to a signal from a horizontal scanning shift register.

One line period is defined as a time period until one cycle of writing of the information to the group of memories 1 is ended. In other words, one line period is defined as a time period from the point when writing of information from the digital decoders to the leftmost memory 1 in FIG. 1 is started to the point when writing of information from the digital decoders to the rightmost memory 1 in FIG. 1 is ended.

The 64 kinds of information supplied to the digital decoders are supplied at appropriate times according to timing of writing to the respective memories 1.

After writing of information to the group of memories 1 is ended, information written to the group of memories 1 is simultaneously transferred to a group of memories 2 according to timing of operation of the shift register.

To the group of memories 1 in which the information has been transferred to the group of memories 2, information supplied to the digital decoders is sequentially written again according to a signal from the horizontal scanning shift register.

In this second cycle of one line period, gradation voltage is selected according to the information which is written to the group of memories **1** in the first cycle of one line period and which is transferred to the group of memories **2** when the second cycle of one line period is started.

As shown in FIG. **2**, gradation voltage obtained by dividing voltage corresponding to eight levels of gradation into eight (8×8) in one line period is supplied. Accordingly, 64 kinds of gradation voltage are supplied in one line period.

One among the 64 kinds of gradation voltage shown in FIG. **2** is selected by a D/A converter based on the information written to each of the memories **2**.

In each of the memories **2**, information with regard to which gradation voltage is to be selected among the eight levels of gradation voltage in which period among the periods obtained by dividing one line period into eight is written.

Based on the information, a predetermined kind of gradation voltage is selected according to predetermined timing by the D/A converter. The selected kind of gradation voltage is supplied to a source signal line.

The gradation voltage supplied to the source signal line is selected by a thin film transistor which operates according to a signal from a vertical scanning shift register which is not shown. In this way, information corresponding to a predetermined level of gradation is written to a predetermined pixel.

It is to be noted that writing of information to a pixel electrode by a thin film transistor must be completed within a period obtained by dividing one line period into eight.

Timing of supplying gradation voltage to a source line depends on which of the gradation levels shown in FIG. **2** is selected. In other words, timing of supplying gradation voltage to a source signal line depends on which of the periods obtained by dividing one line period into eight includes the gradation level to be selected.

For example, if attention is paid to a predetermined line of pixel group (in FIG. **1**, a predetermined line of pixel row), writing of information to this line of pixel group is carried out according to eight kinds of timing according to the gradation levels.

Therefore, different from the case of the conventional structure shown in FIG. **3**, timing of supplying gradation voltage to source signal conductors is not to supply gradation voltage sequentially according to signals from a horizontal scanning shift register.

(Embodiment 1)

FIG. **1** schematically illustrates an active matrix liquid crystal display device as Embodiment 1. In a matrix circuit, a gate signal line **101** is formed for each row and a source signal line **102** is formed for each columns. A thin film transistor **103** and a liquid crystal cell **104** comprising a pixel electrode, liquid crystal, and a counter electrode are formed for each pixel.

(Outline of operation)

First, a signal to be supplied to a digital decoder **111** is selected according to a signal from a shift register circuit **112** of a source driver (a shift register for horizontal scanning) to be stored in the memories **1**.

After picture information corresponding to one line is stored in the memories **1** disposed so as to correspond to the respective source signal lines **102**, information stored in the group of memories **1** is simultaneously transferred to the group of memories **2**, utilizing timing of start of writing information for the subsequent line to the memories **1**.

Based on the information stored in the group of memories **2**, one among the 64 kinds of signal voltage with regard to gradation voltage shown in FIG. **2** is selected by the D/A converter, and is supplied to a source signal line **102**.

The signal voltage corresponding to a predetermined level of gradation and supplied to the source signal line is selected by a thin film transistor which is disposed in each pixel (pixel transistor) and which operates according to a signal from a shift register of a gate driver (a shift register for horizontal scanning) which is not shown. In this way, picture information corresponding to a predetermined level of gradation is written to each pixel.

(Detailed operation)

Detailed operation is described in the following. In FIG. **1**, six digital decoder lines **1–6** are shown.

A signal with regard to which of the eight levels of gradation voltage (2^3=8) is to be selected is supplied to three of the digital decoder lines.

A signal with regard to which of periods obtained by dividing one line period into eight (2^3) is to be selected is supplied to the remaining three digital decoder lines.

By combining these signals supplied to the digital decoder lines, $2^3 \times 2^3$=64 kinds of information can be obtained (64 levels of gradation voltage sequentially sent according to the timing shown in the figure are selected based on these 64 kinds of information, which will be described in the following).

One line period is time necessary to write information to all pixels in a column (a horizontal line). This one line period equals to time necessary for the shift register of source driver (the horizontal scanning shift register) to operate sequentially from one end to another.

Eight signal lines to which gradation voltage is supplied are supplied with signal voltage as shown in FIG. **2**. More specifically, one line period is divided into eight, and signal voltage corresponding to eight levels of gradation is supplied to the respective eight signal lines in each ⅛ of one line period. Accordingly, in one period obtained by dividing one line period into eight, signal voltage for only eight levels of gradation is supplied.

For example, gradation voltage is supplied, as shown in FIG. **2**, such that gradation voltage V_1–V_8 is supplied in the first eighth of one line period, and such that gradation voltage V_9–V_{16} corresponding eight levels of gradation is supplied in the second eighth of one line period.

In this way, signal voltage for eight levels of gradation is allotted to each of the eight periods obtained by dividing one line period as shown in FIG. **2**.

By combining eight levels of signal voltage and eight kinds of timings obtained by the division of one line period, signal voltage corresponding to 64 levels of gradation is supplied in one line period.

In actual operation, the digital decoders **1–6** takes in, based on a signal from the horizontal scanning shift register, information with regard to which signal is to be selected among signals for the 64 levels of gradation shown in FIG. **2** for the memories **1** corresponding to the respective source signal lines.

More specifically, first, the digital decoders **1–6** takes in information with regard to which signal is to be selected among the above signals for the 64 levels of gradation for the first memory **1**. Next, the digital decoders **1–6** takes in information with regard to which signal is to be selected among the above signals for the **64** levels of gradation for the second memory **1**. Such operation is sequentially carried out according to a signal from the horizontal scanning shift register.

Predetermined information to be written to a predetermined memory **1** is sequentially supplied to the digital

decoder lines so as to correspond to timing of operation of the shift register.

In this way, information with regard to which signal voltage is to be selected among the signal voltage for the 64 levels of gradation shown in FIG. 2 is taken in the group of memories 1 according to the operation of the shift register.

After writing of information for one line period to the group of memories 1 is ended, information written to the group of memories 1 is simultaneously transferred to the group of memories 2 just before writing of information for the subsequent one line period is started. Then, with regard to the group of memories 1, the operation as described above is repeated once again, and information for the subsequent one line period is written.

In this state, each of the memories 2 stores information with regard to which signal is to be selected among the signals for the 64 levels of gradation shown in FIG. 2.

According to the information, the D/A converters select gradation voltage. More specifically, gradation voltage supplied in a state as shown in FIG. 2 is selected at appropriate times according to necessary timing.

In other words, signal voltage for one among the 64 levels of gradation supplied according to the timing shown in FIG. 2 is selected by the D/A converters based on the information written to the memories 2.

In one line period, signal voltage corresponding to one among the 64 levels of gradation is supplied to each of the source signal lines. Therefore, depending on which signal voltage for eight levels of gradation is selected by the D/A converters according to which timing is selected among the eight portions obtained by dividing one line period, necessary signal voltage is supplied to a predetermined source signal line.

Here, there are eight kinds of timing according to which signal voltage is supplied to the respective source lines with regard to each source line, so as to correspond to the timing shown in FIG. 2 according to which signal voltage is supplied. This is different from the conventional operation shown in FIG. 3 where signal voltage is sequentially supplied to the source signal lines according to the operation of the shift register.

In the operation shown in the present embodiment, it is necessary for the operation of the thin film transistors in the respective pixels to be fast to some extent.

This is because time period during which a gradation voltage signal is supplied to a source signal line is only ⅛ of one line period.

For example, if the XGA standard (1024×768 pixels) is adopted to write a picture 60 times per second, time period for supplying signal voltage for one among the eight levels of gradation to a source signal line according to the timing shown in FIG. 2 obtained by dividing one line period into eight is on the order of 2.7 μsec.

More specifically, writing for one picture takes 1/60 sec, one line period is ((1/60)/768) sec, and by dividing this into eight, on the order of 2.7 μsec is found.

Therefore, if writing of information to a pixel electrode is not completed within the period of on the order of 2.7 μsec, necessary writing of gradation information to the pixel electrode can not be carried out.

For example, in order to complete writing of information within on the order of 2.7 μsec, switching time of the thin film transistor is required to be 1 μsec or less. In other words, the thin film transistor is required to have operating speed of switching in 1 μsec or less.

Operating speed of switching in 1 μsec or less means, in short, operating speed of 1 MHz or more. Actually, since operating margin is necessary, a thin film transistor disposed in a pixel is required to have operating speed of still higher frequency.

Further, the shift register of the source driver (horizontal scanning shift register), a circuit for supplying a signal to the digital decoders, a circuit for supplying gradation voltage, the memories 1, the memories 2, and the D/A converters are required to have operating performance to operate within a period obtained by dividing one line period by the number of horizontal pixels.

For example, suppose the XGA standard (1024×768 pixels) is adopted. In this case, one line period is ((1/60)/768) sec.

Therefore, the horizontal scanning shift register circuit is required to operate within a time period of that time divided by the number of horizontal pixels, that is, 1024. In other words, it is required to operate within on the order of 0.02 μsec. This means, if converted into frequency, on the order of 48 MHz or higher.

However, since information dealt with by a D/A converter when attention is paid to a predetermined point of time is information for the eight levels of gradation, this is not so burdensome for the D/A converters. In other words, the D/A converters are not required to have complicated structure, and thus, may be ones having performance which can be attained with a thin film transistor.

As is described in the following, utilizing a novel crystalline semiconductor film developed by the present inventors makes it possible to form a shift register, an A/D converter, and a memory having the above characteristic.

It is to be noted that in a structure shown in the present embodiment, though time period during which information is retained in a pixel varies, since this is shorter than the length of one line period, this is not a particular problem.

For example, suppose the XGA standard (1024×768 pixels) is adopted to write a picture 60 times per second. In this case, one line period is ((1/60)/768) sec, i.e., on the order of 22 μsec.

On the other hand, if the OFF current of the thin film transistor is sufficiently small, time period during which information is retained in a pixel is on the order of (1/60) sec, i.e., on the order of 0.016667 sec.

The ratio of the two values is almost 760, which can be completely neglectable in case of display of 64 levels of gradation.

Though FIG. 1 shows an example of a liquid crystal display device displaying 64 levels of gradation, the present embodiment is applicable to display of 256 or 1024 levels of gradation. Even in case of display of 256 or 1024 levels of gradation, the principle of operation is similar to the case of display of 64 levels of gradation.

For example, in case of 256 levels of gradation, eight digital decoder lines and 16 gradation voltage lines for supplying gradation voltage are used. Signal voltage corresponding to 16 levels of gradation is allotted to each gradation voltage line in each period obtained by dividing one line period into sixteen, and voltage signal lines of 16×16=256 levels of gradation are supplied to the gradation voltage lines in one line period. A signal with regard to which of the sixteen (2^4) gradation voltage lines is to be selected is supplied to four of the digital decoder lines. A signal designating which of the periods obtained by dividing one line period into sixteen is to be selected is supplied to the remaining four digital decoder lines.

In case of 1024 levels of gradation, 32 (2^5) gradation voltage lines for supplying gradation voltage are used, for example. Ten digital decoder lines are used, and a signal

with regard to which of the thirty-two (2^5) gradation voltage lines is to be selected is supplied to five of the digital decoder lines, while a signal designating which of the periods obtained by dividing one line period into thirty two is to be selected is supplied to the remaining five digital decoder lines.

Accordingly, in case of 2^x levels of gradation, x digital decoder lines and 2(x/2) gradation voltage lines for supplying gradation voltage are used.

(Example of circuits structured as shown in FIG. 1)

Here, a specific example of circuits forming the active matrix liquid crystal display device shown in FIG. **1** is shown.

(Shift register circuit)

FIG. **4** illustrates a specific example of the shift register circuit **112**. SP means a start pulse. By inputting a start pulse signal, the shift register starts operation according to predetermined timing.

The shift register circuit **112** has a function to sequentially produce, according to predetermined timing, signals determining timing of operation for the circuits corresponding to the source signal lines **102** (memory circuits **1**).

(Memory circuit)

FIG. **5** schematically illustrates structure of the memories **1** and **2** shown in FIG. **1**. FIG. **5** shows circuit blocks of the memories **1** and **2** corresponding to the source signal lines **102**.

Predetermined information is written to the memories **1** from the digital decoder lines according to a signal from the shift register **112**.

Information written to the memories **1** is information with regard to eight levels of gradation voltage (hereinafter referred to as voltage selection bits) and information with regard to eight kinds of timing for selecting gradation voltage (hereinafter referred to as timing selection bits).

The information is simultaneously written to the memories **2** according to a signal supplied with regard to every one line period. The signal supplied with regard to every one line period (pulse per one line) is in synchronous with the start pulse inputted to the horizontal scanning shift register.

Information written to the memories **2** is outputted from the memories **2** as voltage selection bits (2^3=8 choices) and timing selection bits (2^3=8 choices).

(D/A converter)

The D/A converters shown in FIG. **1** has a structure as shown in FIGS. **6** and **7**. It is to be noted that signals a–h in FIG. **7** are repeatedly supplied with regard to each line according to timing as shown in FIG. **8**.

In the circuit shown in FIG. **7**, a signal with regard to timing according to which gradation voltage is selected (shown as A in the figure) is supplied to the circuit shown in FIG. **6** according to information supplied to the timing selection bits and the signals a–h supplied according to the timing shown in FIG. **8**.

In the circuit shown in FIG. **6**, based on a signal supplied from FIG. **7**, a signal for selecting information with regard to the eight kinds of supply voltage to be supplied to the voltage selection bits (there are eight kinds of voltage selected according to the same timing) according to predetermined timing.

The signal is, as shown in FIG. **6**, outputted from eight NAND circuits. According to the signal, one among the gradation voltage signals as shown in FIG. **2** is selected to be supplied to the source signal lines.

(Method of manufacturing thin film transistor)

Here, a method of manufacturing a thin film transistor (also referred to as TFT) which can operate at on the order of 50 MHz at 3.3 V–5 V.

The thin film transistor has a characteristic that it can operate ten or more times as fast as a conventionally known low-temperature crystalline semiconductor TFT or a high-temperature crystalline semiconductor TFT.

Here, a process is described for simultaneously forming in parallel on the same quartz substrate a CMOS circuit utilized for forming a shift register circuit, a memory, and a D/A converter circuit, and an N-channel type thin film transistor utilized as a thin film transistor.

FIGS. **9** and **10** schematically illustrate the manufacturing process.

First, the surface of a quartz substrate **701** which is sufficiently flat is cleaned. Then, an amorphous semiconductor film **702** is formed at a thickness of 500 Å on the quartz substrate **701** by low-pressure thermal CVD. In this way, a state shown in FIG. **9**A is obtained.

Next, a mask **703** is formed using a silicon oxide film formed at a thickness of 700 Å by plasma CVD.

The mask has openings at portions **704** and **705**, where the amorphous semiconductor film **702** is exposed (FIG. **9**B).

The openings are shaped to be slit-like the longitudinal direction of which is perpendicular to the plane of the figure.

After the mask **703** which is a silicon oxide film is formed, nickel acetate solution including 10 p.p.m. (weight base) of nickel element is uniformly applied by spin coating. By the process, a state where nickel element is retained in contact with the whole surface as shown by **704** of FIG. **9**B is obtained.

Here, the obtained state is that nickel element is retained selectively in contact with a part of the amorphous semiconductor film **702**. More specifically, nickel element is in contact with the amorphous semiconductor film **702** in the regions of the openings **704** and **705** as described above. In this way, nickel element is introduced.

Alternatively, nickel element may be introduced by ion implantation. In this case, compared with the case where nickel element solution is applied, the positions where nickel element is introduced can be controlled more precisely. Therefore, this is especially effective in case, for example, the width of regions where nickel element is to be introduced is quite narrow such as several μm or less, or, the shape of the regions where nickel element is to be introduced is complicated.

After nickel element is introduced in this way, heat treatment is carried out.

The heat treatment is carried out in a nitrogen atmosphere at 500° C.–630° C., for example at 600° C. for eight hours. In this heat treatment, crystal growth **706** in the direction in parallel with the substrate proceeds as shown in FIG. **9**C. The crystal growth can be made over a length of 100 μm or more.

The semiconductor film formed by the crystal growth means as described above has a specific crystal structure where bar-like or columnar crystals extend along the direction of the crystal growth.

After the crystallization is completed, heat treatment is carried out in an oxygen atmosphere containing halogen element, for example, in an oxygen atmosphere containing 3 volume % of HCl at 950° C. for 20 minutes to form a thermal oxide film at a thickness of 200 Å.

Here, the thickness of the semiconductor film is decreased from 500 Å to 400 Å. By the action of the halogen element, in this case, chlorine, nickel element in the semiconductor film is drawn out into the thermal oxide film, and thus, the thermal oxide film contains relatively high density of nickel element.

In the process of forming the thermal oxide film, annealing of detects in the film is carried out, and the crystallinity is greatly improved.

Next, the thermal oxide film is removed. In this way, nickel element in the semiconductor film can be decreased.

In case nickel element is utilized, the density of nickel which finally remains in the semiconductor film is, under the present conditions, on the order of 1×10^{14} atoms/cm^3–5×10^{18} atoms/cm^3. The lower the density is, the more preferable it is. With the gettering conditions of the thermal oxide film being fixed, the upper limit of the density can be decreased as low as 5×10^{17} atoms/cm^3. The density can be measured utilizing SIMS (secondary ion mass spectrometer).

Next, patterns **707**, **708**, and **709** to be an active layer of the thin film transistor are formed as shown in FIG. 9D.

After the patterns of the active layer are formed, a silicon oxide film forming a gate insulating film is formed at a thickness of 400 Å by plasma CVD.

Further, a thermal oxide film is again formed at a thickness of 300 Å. The thermal oxide film is formed in an oxygen atmosphere containing 0.1–10 volume %, for example, 3 volume %, of HCl at 950° C. for 30 minutes.

Here, the thermal oxide film is formed on the surface of the active layer. In this way, a gate insulating film **710** having a thermal oxide film at a thickness of 300 Å and the laminated CVD silicon oxide film at a thickness of 400 Å is obtained. It is to be noted that the final thickness of the active layer is 250 Å.

In the present embodiment, the patterns are disposed such that the direction of the crystal growth is the direction of movement of carriers when the thin film transistor is operated.

In this way, a thin film transistor which can operate at 1 GHz at the level of a ring oscillator and at 100 MHz at the level of a shift register at driving voltage of 3.3–5V can be manufactured.

After the gate insulating film **710** is obtained, gate electrodes **711**, **712**, and **713** are formed as shown in FIG. 9D with material the main component of which is aluminum.

As the material of the gate electrodes, other than material the main component of which is aluminum, tantalum (Ta), crystalline semiconductor to which phosphorus (P) is heavily doped, wolfram silicide (WSi), or a structure where crystalline semiconductor subjected to phosphorus-doping and wolfram silicide are laminated or mixed may be used.

With regard to the gate electrodes **711**, **712**, and **713**, the material the main component of which is aluminum forming the gate electrodes may be anodized by weak acid solution to provide a dense anodic oxide film only on the side faces, or, on the upper and the side faces of the gate electrodes. In this case, as the material of the gate electrodes, other than aluminum, tantalum may be used.

In case the anodic oxide film is provided on the side and upper faces, occurrence of hillocks may be prevented in a subsequent heat process. In case the anodic oxide film is provided only on the side faces, since there is no hard anodic oxide film on the upper faces, contacts with wirings to be connected are easily formed.

Further, since the anodic oxide film is on the side faces of the gate electrodes, in a subsequent impurity ion implantation process, by using the gate electrodes and the anodic oxide film on the side faces as a mask, offset regions the thickness of which is substantially equal to the thickness of the anodic oxide film is formed in channels forming regions of the thin film transistor are formed, and leakage current can be decreased.

Here, the gate electrode **711** is for a P-channel type thin film transistor (PTFT) forming the CMOS. The gate electrode **712** is for an N-channel type thin film transistor (NTFT) forming the CMOS. The gate electrode **713** is for an N-channel type thin film transistor (NTFT) forming the CMOS.

Next, P (phosphorus) is doped by plasma doping. In the process, a source region **714**, a channel region **715**, and a drain region **716** of the PTFT forming the CMOS are formed in a self-aligning manner.

Next, B (boron) is doped by plasma doping. In the process, a source region **719**, a channel region **718**, and a drain region **717** of the NTFT forming the CMOS are formed in a self-aligning manner. Further, a source region **720**, a channel region **721**, and a drain region **722** of the NTFT disposed in a pixel are formed in a self-aligning manner. In this way, a state shown in FIG. 9E is obtained.

In the doping process as described above, in case P (phosphorus) is doped, regions where B (boron) is to be doped are masked with resist, while, in case B (boron) is doped, regions where P (phosphorus) is to be doped are masked with resist. In this way, the PTFT and NTFT are formed.

After the doping as described above is completed, by laser light irradiation, activation of the regions where the doping was carried out and annealing of damaged crystal structure are carried out.

Next, as shown in FIG. 9F, a silicon nitride film **723** as an interlayer insulating film is formed at a thickness of 1500 Å by plasma CVD. Further, a film **724** made of polyimide resin is laminated. In this way, a state shown in FIG. 9F is obtained.

With the resin film, the upper face can be made flat, which is convenient for forming wirings, carrying out orientation treatment, and injecting liquid crystal in subsequent processes.

It is to be noted that, as the material of the resin, other than the polyimide resin, acrylic resin, polyamide resin, polyimideamide resin, or the like may be used.

Next, as shown in FIG. 10A, contact holes are formed in the interlayer insulating film to form source electrodes **725** and **727** of the CMOS, a drain electrode **726** common to the PTFT and NTFT, and a source electrode **728** and a drain electrode **729** of the pixel transistor (NTFT).

These electrodes are formed with a film formed by laminating a titanium film, an aluminum film, and a titanium film.

Here, the source electrodes **725** and **727** are formed such that necessary wirings (source wirings) extend therefrom. Further, the common drain electrode **726** is also formed such that necessary wirings (drain wirings) extend therefrom.

The source electrode **728** of the pixel TFT (NTFT) is formed as a part of source signal lines disposed in a pixel matrix. It is to be noted that the gate electrode **713** is formed as what (or a part of what) extends from gate signal lines disposed so as to be lattice together with the source signal lines.

Next, as shown in FIG. 10B, a second interlayer insulating film **730** is formed with polyimide resin. Then, a contact hole is formed to form a pixel electrode **731** made of ITO.

In this way, the CMOS forming various circuits and the thin film transistor to be disposed in a pixel can be integrated on the quartz substrate as shown in FIG. 10C.

A ring oscillator circuit formed with a thin film transistor made according to such a manufacturing method can oscillate at a frequency of 1 GHz or more.

Since operating frequency is set leaving a martin in designing an actual circuit, a circuit which can operate at a frequency of as high as 1 GHz can not be formed.

However, a shift register circuit, an arithmetic circuit, and the like which can operate at least at 100 MHz can be formed with this thin film transistor.

A thin film transistor utilizing a crystalline semiconductor film having such a specific crystal structure has a characteristic that, due to its crystal structure, the short-channel effect is difficult to appear. It also has characteristics that, since insulator is used as the substrate, it is free from the problem of capacity of the substrate, and, suitable for high-speed operation.

A MOS transistor utilizing a conventional single crystalline semiconductor wafer is under the scaling law, that is, if the size of a transistor is made smaller according to a predetermined formula, the performance of the transistor becomes higher according to a predetermined formula.

However, since the miniaturization has advanced greatly recently, it is now difficult to heighten the performance of a transistor according to the scaling law.

One reason for this is that the shorter the channel length becomes for the purpose of controlling the short-channel effect, the more careful devices become necessary such as doping of impurity beside the channel, and thus, difficulty in the manufacturing process is increased.

However, if the crystalline semiconductor film having such a specific crystal structure as described above is used, necessary characteristics can be obtained at a size which does not follow the scaling law as described above.

The reasons for this are considered to be:

(1) By making the direction of the columnar crystals the same as the direction of movement of carriers in the channel, the short-channel effect is controlled;

(2) By utilizing insulator as the substrate, the problem of capacity is greatly controlled; and

(3) Since aluminum can be utilized as the gate electrodes, the TFT is advantageous to high-speed operation.

With regard to (1), it can be considered as in the following. The columnar crystals are partitioned one by one by inactive grain boundary. Since the energy level is high in the grain boundary, movement of carriers is controlled to be in the direction of extension of the crystals. Similarly, spread of a depletion layer from a source region and a drain region to the inside of a channel is controlled. These are considered to be the reasons that the short-channel effect is controlled.

The following is a specific example which does not follow the scaling law.

For example, where, according to the conventional scaling law, the thickness of the gate insulating film should be 100 Å, if a crystalline semiconductor film as disclosed herein is used, the same characteristics can be obtained with the gate insulating film being 300 Å, and thus, a highly anti-static characteristic can be obtained.

This is understood to be due to (1)–(3) as described above.

Further, not only with regard to the gate insulating film thickness, predetermined characteristics can be obtained with less strict conditions (less strict by one rank) than the conventional scaling law also with regard to the channel length.

This is useful when semiconductor circuits capable of operating at a high speed are manufactured in a great area at a low cost.

(Embodiment 2)

The present embodiment is an example in case laser irradiation is also used in obtaining a crystalline semiconductor film.

In the present embodiment, after the crystallization by heating utilizing nickel shown in Embodiment 1, laser light is irradiated to improve the crystallinity. In the process, thermal oxidation is not carried out.

In such a case, since the process temperature is 600° C. or lower, glass can be used as the substrate.

However, the crystallinity of the obtained crystalline semiconductor film is lower compared with the method shown in Embodiment 1 utilizing thermal oxidation. Also, the characteristics of the obtained thin film transistor are inferior to those of Embodiment 1. Therefore, the present embodiment is useful in case the number of pixels is small or the number of levels of gradation is small.

(Embodiment 3)

The present embodiment shows examples of unit utilizing an active matrix liquid crystal panel utilizing the invention disclosed herein.

FIG. **11** shows outline of the unit. FIG. **11A** shows an information processing terminal with a main body **2001** provided with an active matrix liquid crystal display device **2005**.

The unit is provided with an integrated circuit inside and has a function to process and store necessary information. The unit is also provided with a camera portion **2002** which is actuated by a control switch **2004** and has a function to take necessary picture information inside.

The unit has a communication facility, and has a function to take in necessary information from a telephone line and to transmit necessary information to the outside via a telephone line.

In case of such a portable unit, in view of lowering power consumption, it is preferable to adopt a reflection type active matrix liquid crystal display device.

Alternatively, instead of an active matrix liquid crystal display device, active matrix EL (electro-luminescent) element may be adopted.

FIG. **11B** shows a unit called a head-mount display. The unit is provided with a band portion **2103** for mounting on a head. A main body **2101** of the unit is provided with active matrix liquid crystal display devices corresponding to both eyes.

FIG. **11C** shows a navigation unit provided in a car or other means for travelling. The unit is structured such that, based on radio waves from an artificial satellite taken in by an antenna (and a tuner portion) **2204**, navigation information is displayed on an active matrix liquid crystal device **2202** provided for a main body **2201**. The unit is operated by control switches **2203**.

FIG. **11D** shows a portable telephone. A main body **2301** of the unit is provided with a voice inputting portion **2303**, a voice outputting portion **2302**, control switches **2305**, antenna **2306**, and an active matrix liquid crystal display device **2304**.

FIG. **11E** shows a portable video camera. A main body **2401** of the unit is provided with an image receiving portion **2406**, an integrated circuit **2407**, control switches **2404**, an active matrix liquid crystal display device **2402**, a battery **2405**, and a voice inputting portion **2403**.

FIG. **11F** shows a projecting type projector. A main body **2501** of the unit is provided with a light source **2502**, a reflection type active matrix liquid crystal display device **2503**, and an optical system **2504**. Display is carried out by displaying a picture on a screen **2505**.

It is to be noted that, in case not a reflection type but a transmission type is used as the active matrix liquid crystal display device **2503**, the light source **2502** is provided on the rear side of the liquid crystal display device **2503**, such that light passing through the liquid crystal display device **2503** is projected on the screen **2505** to carry out display.

(Embodiment 4)

The present embodiment is formed by forming the structure shown in Embodiments 1 and 2 with a reverse-stagger type thin film transistor. Even if, in the structure shown in

each embodiment, a planar type thin film transistor is used instead to form a reverse-stagger type thin film transistor, similar effect can be obtained.

It is to be noted that, to use as a gate electrode of a reverse-stagger type thin film transistor material enhancing heat resistance, for example, crystalline semiconductor with heavily doped phosphorus, is effective in obtaining a high-performance thin film transistor.

By utilizing the invention disclosed herein, an active matrix type display device for displaying a picture with a digital signal being an input signal can be provided without complicating its structure.

For example, a structure capable of carrying out gradation display such as 64 levels of gradation can be provided as a circuit formed with a thin film transistor.

Although examples of an active matrix liquid crystal display device are shown here, the present invention may be utilized in other devices such as an active matrix type display device with an EL element, an active matrix plasma display device, and an active matrix type display device utilizing EC (electro-chromics).

What is claimed is:

1. An active matrix type display device for 2^x levels of gradation display, comprising an active matrix display portion and a peripheral circuit over a substrate, said peripheral circuit comprising:

gate signal lines and source signal lines disposed so as to form a lattice structure over a substrate;

at least one thin film transistor disposed around intersections of said gate signal lines and source signal lines; and

means for selecting gradation voltage to be supplied to said source signal lines provided for each of said source signal lines, said means for selecting gradation voltage comprising a plurality of digital decoder lines, a plurality of first memory circuits, a plurality of second memory circuits, a plurality of D/A converter circuits, and a plurality of gradation voltage lines,

wherein the number of said digital decoder lines is defined as x and the number of said gradation voltage lines is defined as $2^{(x/2)}$.

2. A display device according to claim 1, wherein selection of gradation voltage by the means for selecting gradation voltage is carried out by selecting one among $2^{(x/2)}$ divided periods obtained by dividing one line period and by selecting one gradation voltage out of $2^{(x/2)}$ gradation voltage levels set in each of said divided periods.

3. A display device according to claim 2, wherein:

said thin film transistor has a function to write picture information to a pixel electrode; and

a period required for said thin film transistor to write information to said pixel electrode is shorter than a length of each of said divided periods.

4. A display device according to claim 1, wherein:

the number of gradation voltage levels 2^x to be supplied to said source signal lines is the product of the number N of said divided periods and the number M of gradation voltage levels set in each of said divided periods (N×M);

said thin film transistor has a function to write picture information to a pixel electrode; and

a period required for said thin film transistor to write information is shorter than a length of each of said N divided periods.

5. A display device according to claim 1, wherein said means for selecting gradation voltage is controlled by:

information with regard to which period is to be selected among said divided periods; and

information with regard to which gradation voltage level is to be selected among said gradation voltage levels set in each of said divided periods.

6. An active matrix type digital display device comprising an active matrix display portion and a peripheral circuit over a substrate, said peripheral circuit comprising:

gate signal lines and source signal lines disposed so as to be lattice over a substrate;

at least one thin film transistor disposed around intersections of said gate signal lines and source signal lines over said substrate; and

means for selecting gradation voltage to be supplied to said source signal lines provided for each of said source signal lines, said means for selecting gradation voltage comprising a plurality of digital decoder lines, a plurality of first memory circuits, a plurality of second memory circuits, a plurality of D/A converter circuits, and a plurality of gradation voltage lines, wherein:

selection of gradation voltage by said means for selecting gradation voltage is carried out by selecting one period set by dividing one line period into N sections and by selecting among M gradation voltage levels set in said period;

the number of gradation voltage levels to be supplied to said source signal lines 2x is the product of the number N of said divided periods and the number M of gradation voltage levels set in each of said divided periods (N×M);

said thin film transistor has a function to write picture information to a pixel electrode; and

the time required for said thin film transistor to write information is shorter than a length of one period set by dividing one line period into N sections.

7. A display device according to claim 6, wherein said means for selecting gradation voltage is controlled by:

information with regard to which signal is to be selected among said periods set by dividing one line period into N sections; and

information with regard to which gradation voltage level is to be selected among M gradation voltage levels set in said period set by said division into N sections.

8. A display device according to claim 6, wherein the number of said digital decoder lines is defined as x and the number of said gradation voltage lines is defined as $2^{(x/2)}$.

9. A method of driving a pixel matrix display device for 2^x levels of gradation display comprising a plurality of gate signal lines and a plurality of source signal lines disposed so as to be lattice and at least one thin film transistor disposed around intersections of said gate signal lines and source signal lines, comprising the step of:

selecting a gradation voltage to be supplied to said plurality of source lines by selecting one period set by dividing one line period into $2^{(x/2)}$ sections and by selecting a voltage level out of $2^{(x/2)}$ voltage levels set in said one period.

10. A method according to claim 9, wherein an operating time of said thin film transistor is shorter than the length of said one period set by dividing one line period into $2^{(x/2)}$ sections.

11. A display device according to claim 1, wherein said device is an EL display device.

12. A display device according to claim 6, wherein said device is an EL display device.

13. A method according to claim 9, wherein an EL display is operated by said method.

14. A device according to claim 1, wherein said digital decoder lines and a shift register are connected with each of said first memory circuits, and each of said D/A converter circuits connected with said gradation voltage lines and each of said source signal lines.

15. A device according to claim 1, wherein both of said active matrix display portion and said peripheral circuit comprise a plurality of thin film transistors formed over said substrate.

16. A device according to claim 6, wherein said digital decoder lines and a shift register are connected with each of said first memory circuits, and each of said D/A converter circuits connected with said gradation voltage lines and each of said source signal lines.

17. A device according to claim 1, wherein both of said active matrix display portion and said peripheral circuit comprise a plurality of thin film transistors formed over said substrate.

* * * * *

US006411273B1

(12) **United States Patent**
Nakamura et al.

(10) **Patent No.: US 6,411,273 B1**
(45) **Date of Patent: Jun. 25, 2002**

(54) **DRIVE CIRCUIT FOR ACTIVE MATRIX LIQUID CRYSTAL DISPLAY**

(75) Inventors: **Mika Nakamura**, Hirakata; **Yutaka Nanno**, Takarazuka; **Naomi Kaneko**, Kyoto; **Masumi Izuchi**, Hirakata; **Hiroshi Tsutsu**, Osaka; **Katsumi Adachi**, Kashiba, all of (JP)

(73) Assignee: **Matsushita Electric Industrial Co., Ltd.** (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/194,721**

(22) PCT Filed: **Apr. 21, 1998**

(86) PCT No.: **PCT/JP98/01818**

§ 371 (c)(1),
(2), (4) Date: **Dec. 21, 1998**

(87) PCT Pub. No.: **WO98/48318**

PCT Pub. Date: **Oct. 29, 1998**

(30) **Foreign Application Priority Data**

Apr. 22, 1997 (JP) 9-104345
Nov. 27, 1997 (JP) 9-325728

(51) **Int. Cl.**[7] **G09G 3/36**
(52) **U.S. Cl.** **345/98**; 345/205
(58) **Field of Search** 345/87, 88, 89, 345/98, 100, 99, 94, 95, 96, 97, 211, 212, 213, 208, 209, 210, 204, 205, 206

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,644,338 A 2/1987 Aoki et al.
5,389,872 A 2/1995 Erhart et al.
5,563,426 A 10/1996 Zhang et al.
5,572,211 A 11/1996 Erhart et al.

FOREIGN PATENT DOCUMENTS

GB	2118386	10/1983
JP	55060333 A	5/1980
JP	63-223788	9/1988
JP	04143791 A	5/1992
JP	04195189 A	7/1992
JP	05061432 A	3/1993
JP	07325556	12/1995
JP	08046515 A	2/1996
JP	08084078 A	3/1996
JP	09127918 A	5/1997

Primary Examiner—Xiao Wu
(74) *Attorney, Agent, or Firm*—Parkhurst & Wendel, L.L.P.

(57) **ABSTRACT**

An object of the present invention is, by eliminating a driver IC from the components of an liquid crystal display, to achieve a cost reduction, to eliminate a manufacturing step of mounting the driver IC onto an array substrate, and to reduce a thickness of the liquid crystal display. A driver circuit for an active matrix liquid crystal display comprises a resistive dividing type digital-to-analog converter circuit (DAC). An analog output voltage from the DAC is amplified by a signal amplifier element, and a liquid crystal element is driven by the amplified analog output voltage. The driver circuit is characterized in that a resistance element R is formed in an n+ layer of p-Si on an array substrate of the liquid crystal display, and a switching element Tr and a signal amplifier element are also formed on the array substrate.

96 Claims, 60 Drawing Sheets

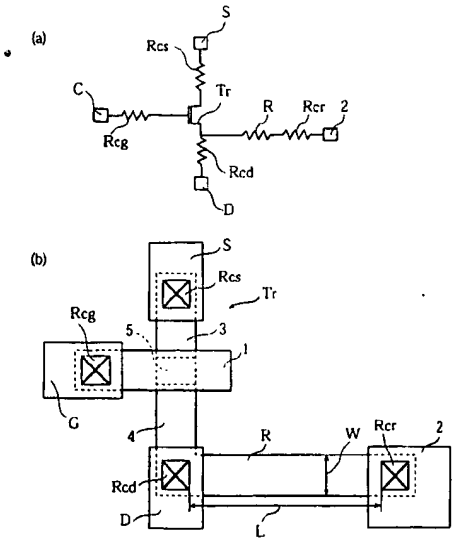


FIG. 1

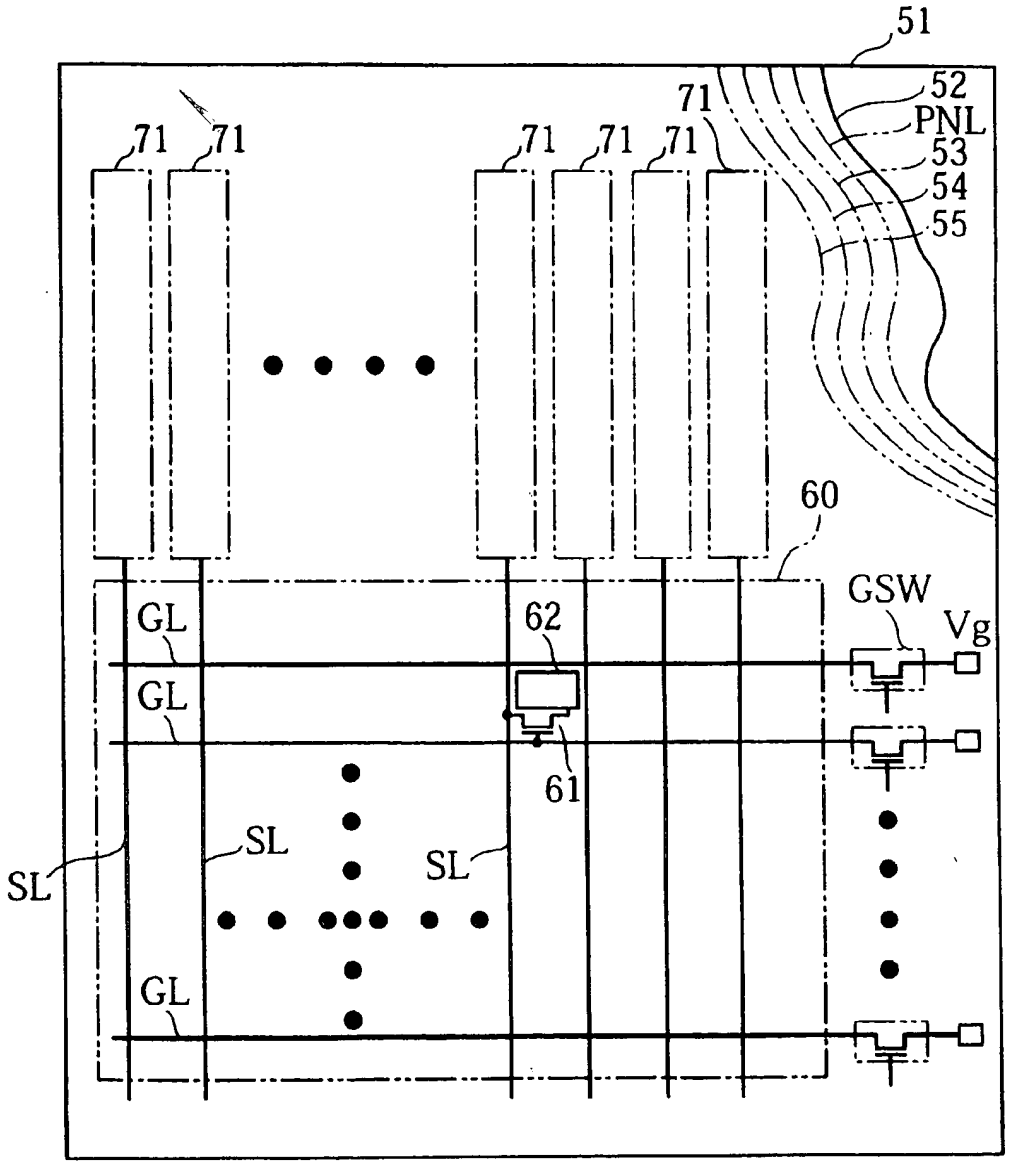

51
52
PNL
53
54
55
71
71
71
71
71
71
60
GSW
Vg
GL
GL
GL
62
61
SL
SL
SL
SL

FIG. 2

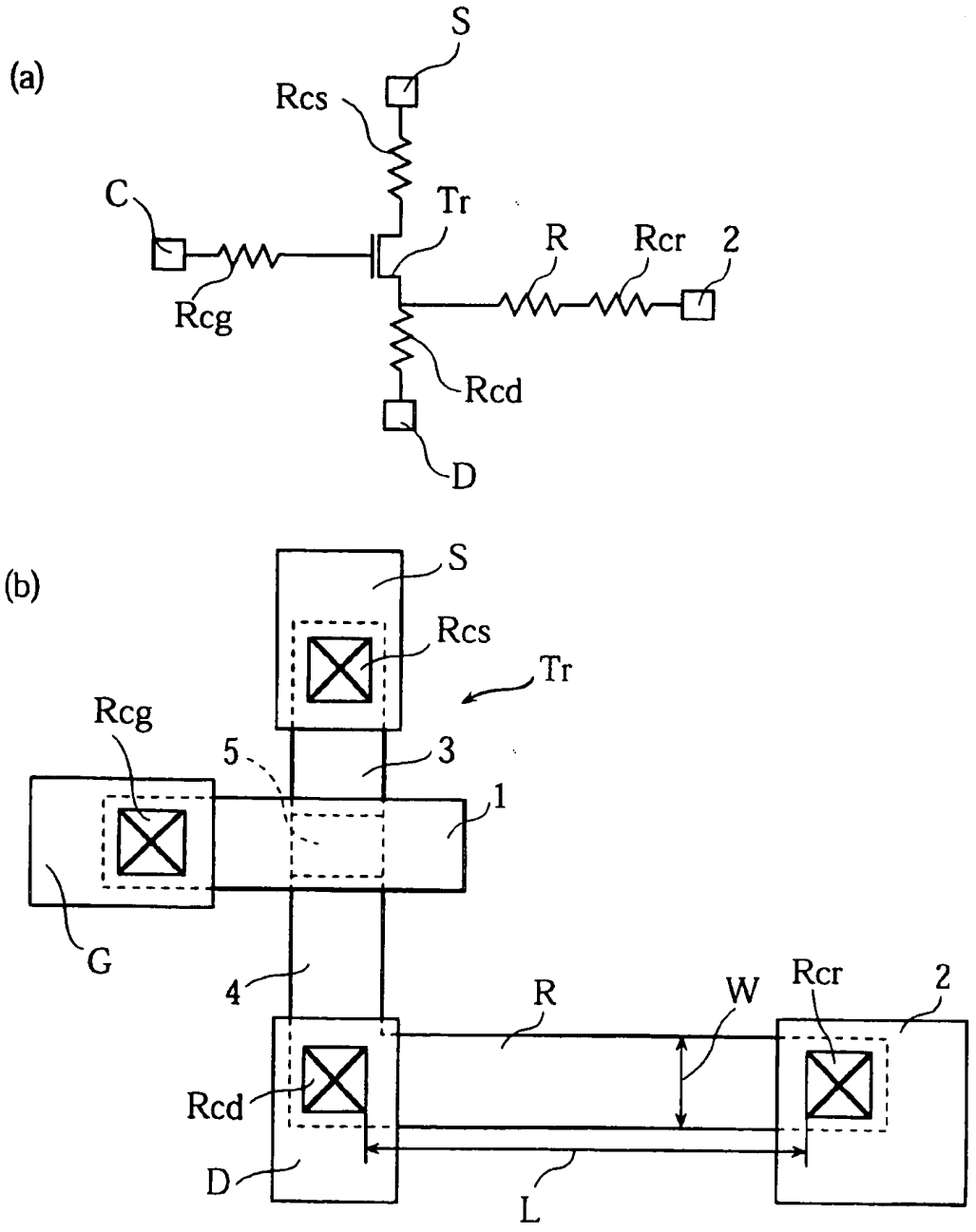


FIG. 3

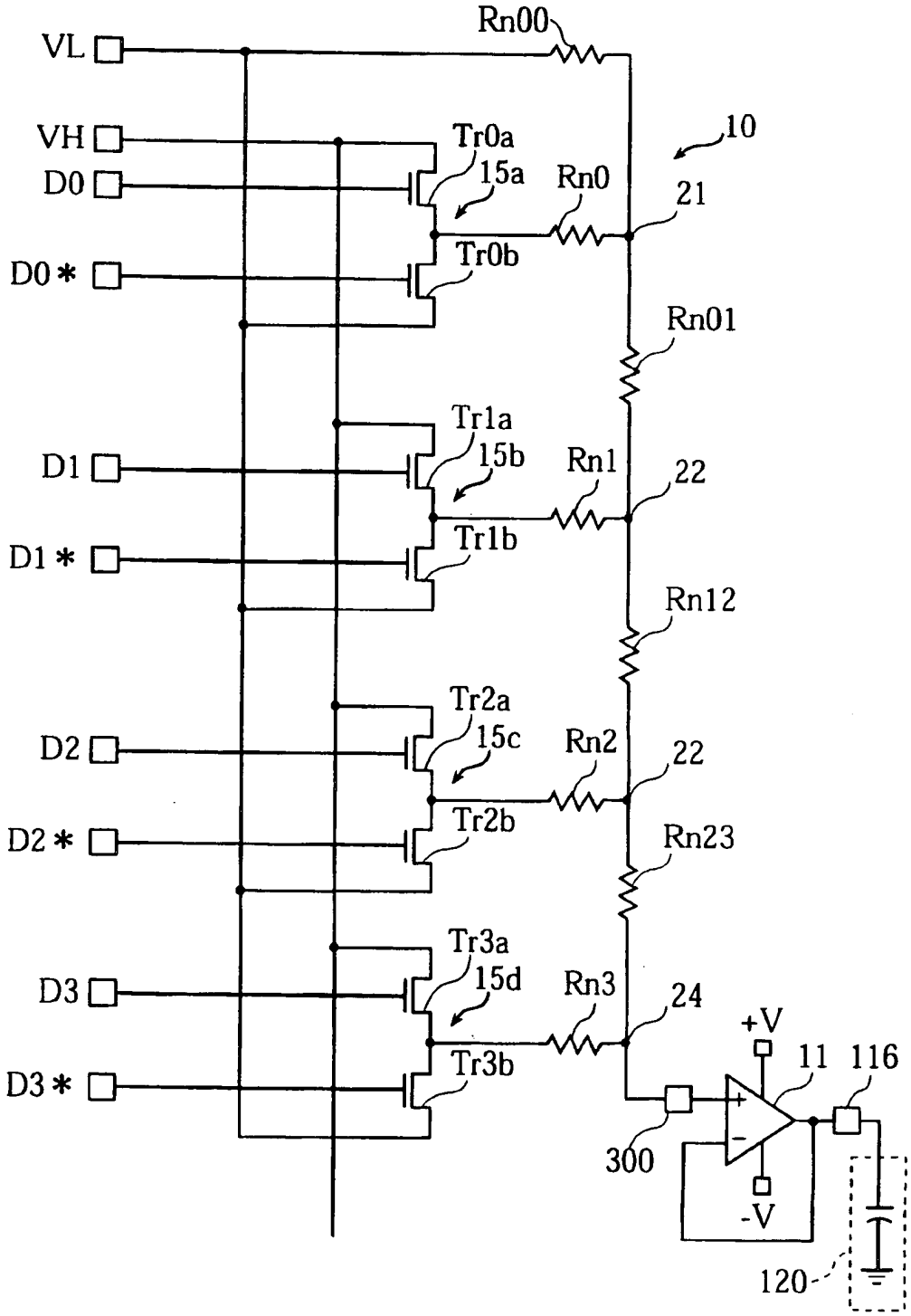

Rn00
VL
VH
D0
D0*
Tr0a
15a
Rn0
10
21
Tr0b
Rn01
Tr1a
15b
Rn1
22
D1
D1*
Tr1b
Rn12
Tr2a
15c
Rn2
22
D2
D2*
Tr2b
Rn23
Tr3a
15d
Rn3
24
D3
D3*
Tr3b
+V
11
116
300
-V
120

FIG. 4

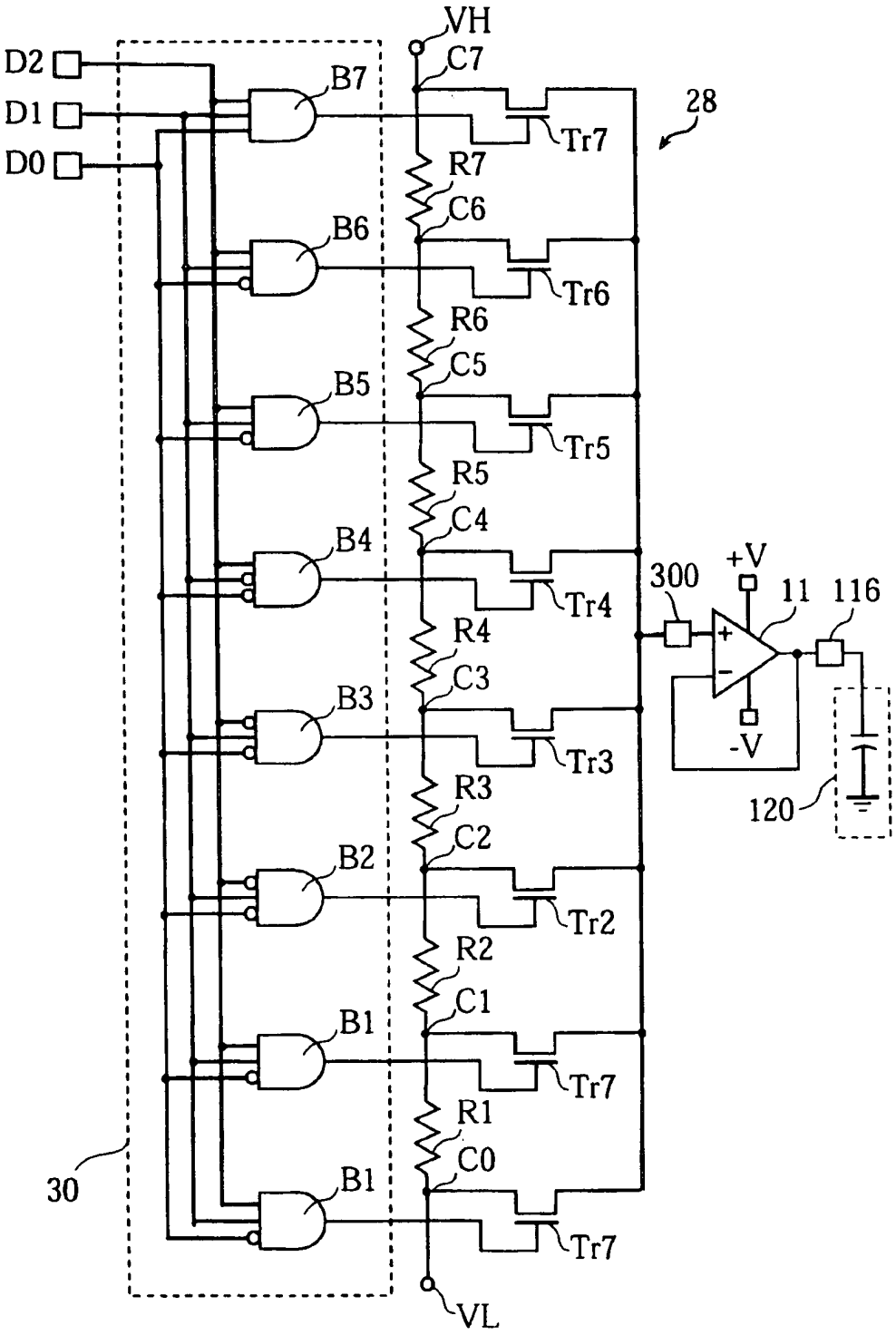

VH
D2
D1
D0
B7
C7
Tr7
28
R7
C6
B6
Tr6
R6
C5
B5
Tr5
R5
C4
B4
Tr4
300
+V
11
116
R4
C3
B3
Tr3
-V
R3
120
C2
B2
Tr2
R2
C1
B1
Tr7
R1
C0
30
B1
Tr7
VL

FIG. 5

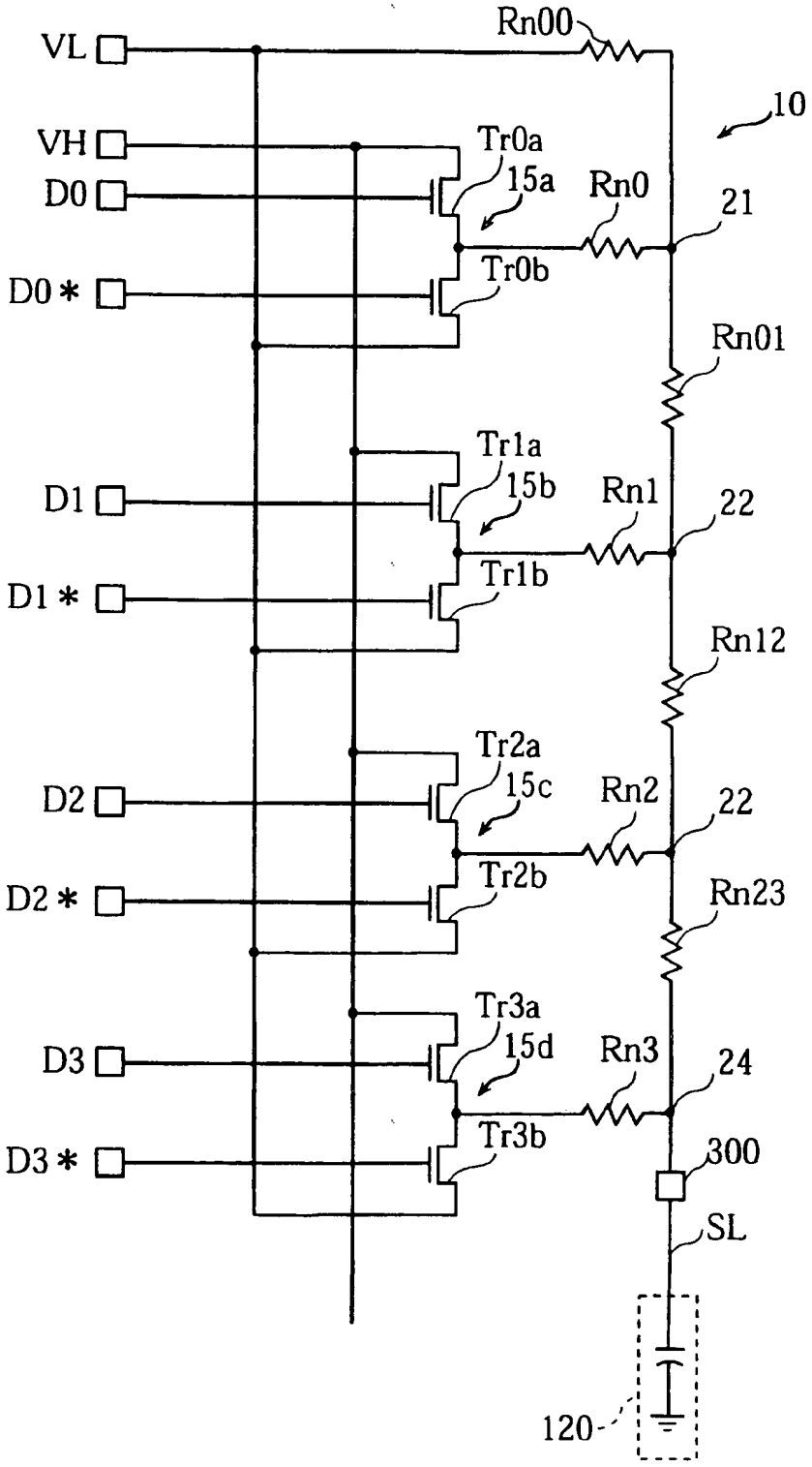

VL
VH
D0
D0*
D1
D1*
D2
D2*
D3
D3*
Rn00
10
Tr0a
15a
Rn0
21
Tr0b
Rn01
Tr1a
15b
Rn1
22
Tr1b
Rn12
Tr2a
15c
Rn2
22
Tr2b
Rn23
Tr3a
15d
Rn3
24
Tr3b
300
SL
120

FIG. 6

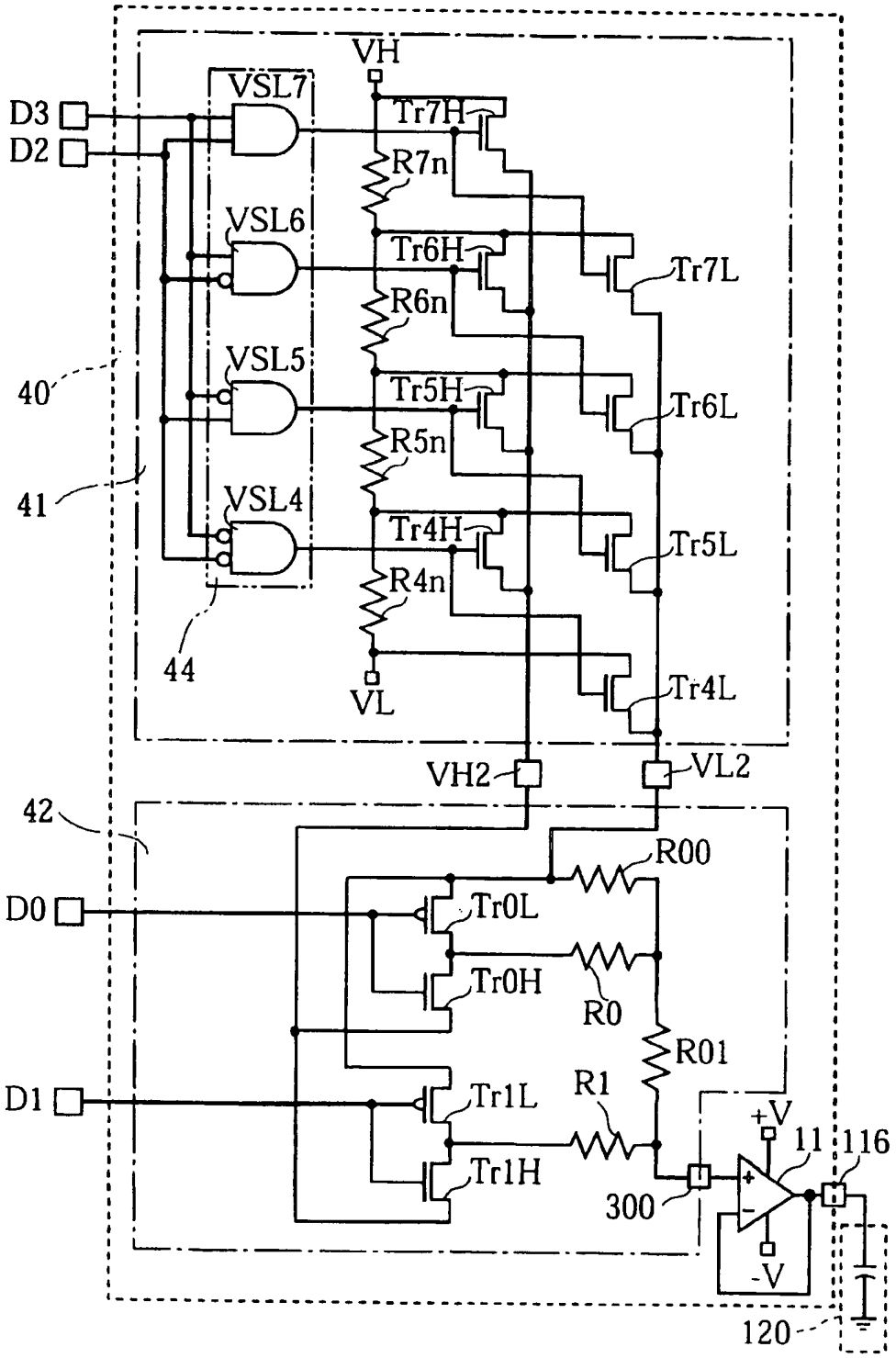

VH
VSL7
D3
D2
Tr7H
R7n
VSL6
Tr6H
Tr7L
R6n
VSL5
40
Tr5H
Tr6L
R5n
41
VSL4
Tr4H
Tr5L
R4n
44
VL
Tr4L
VH2
VL2
42
R00
D0
Tr0L
Tr0H
R0
R01
D1
Tr1L
R1
+V
11
116
Tr1H
300
-V
120

FIG. 7

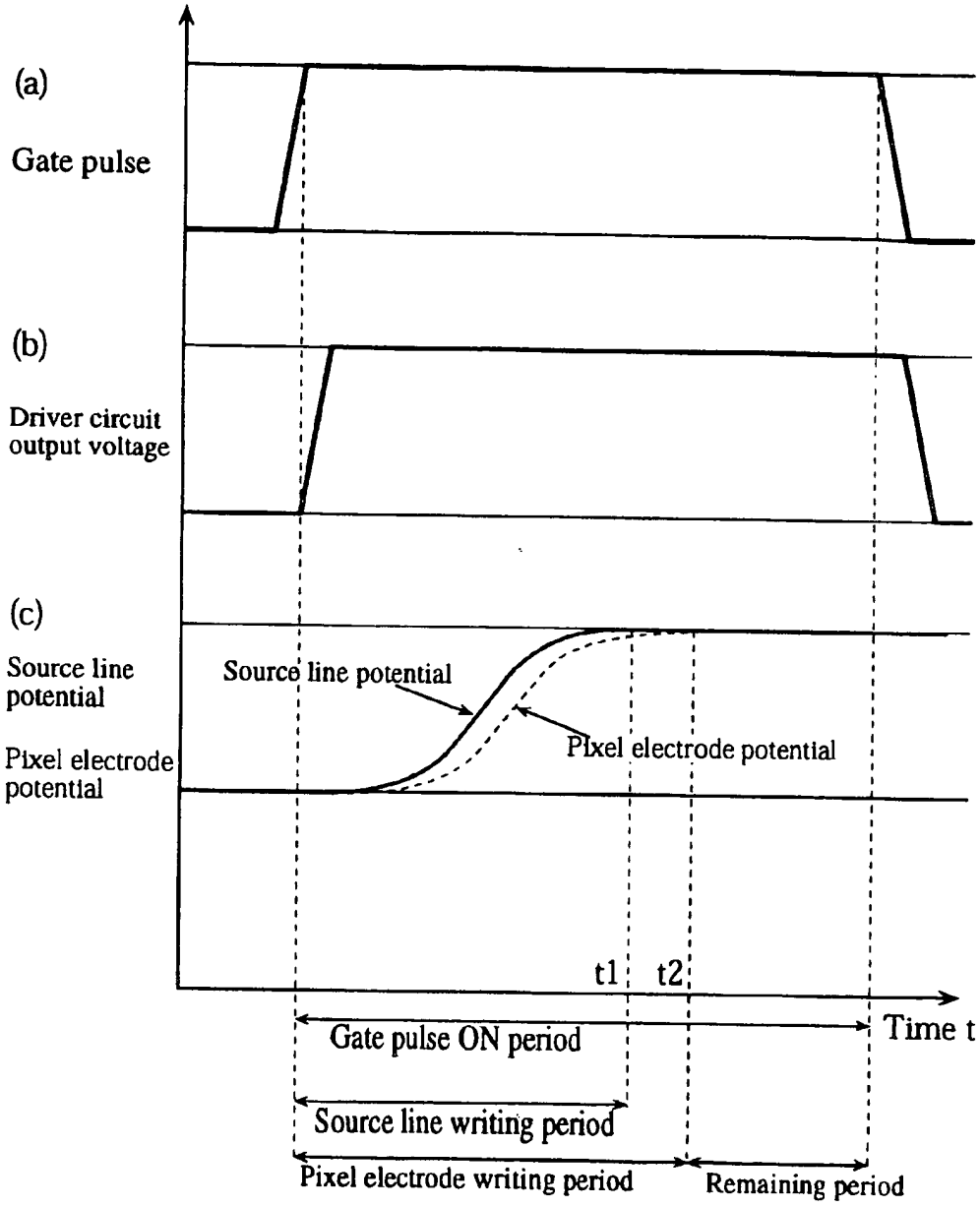
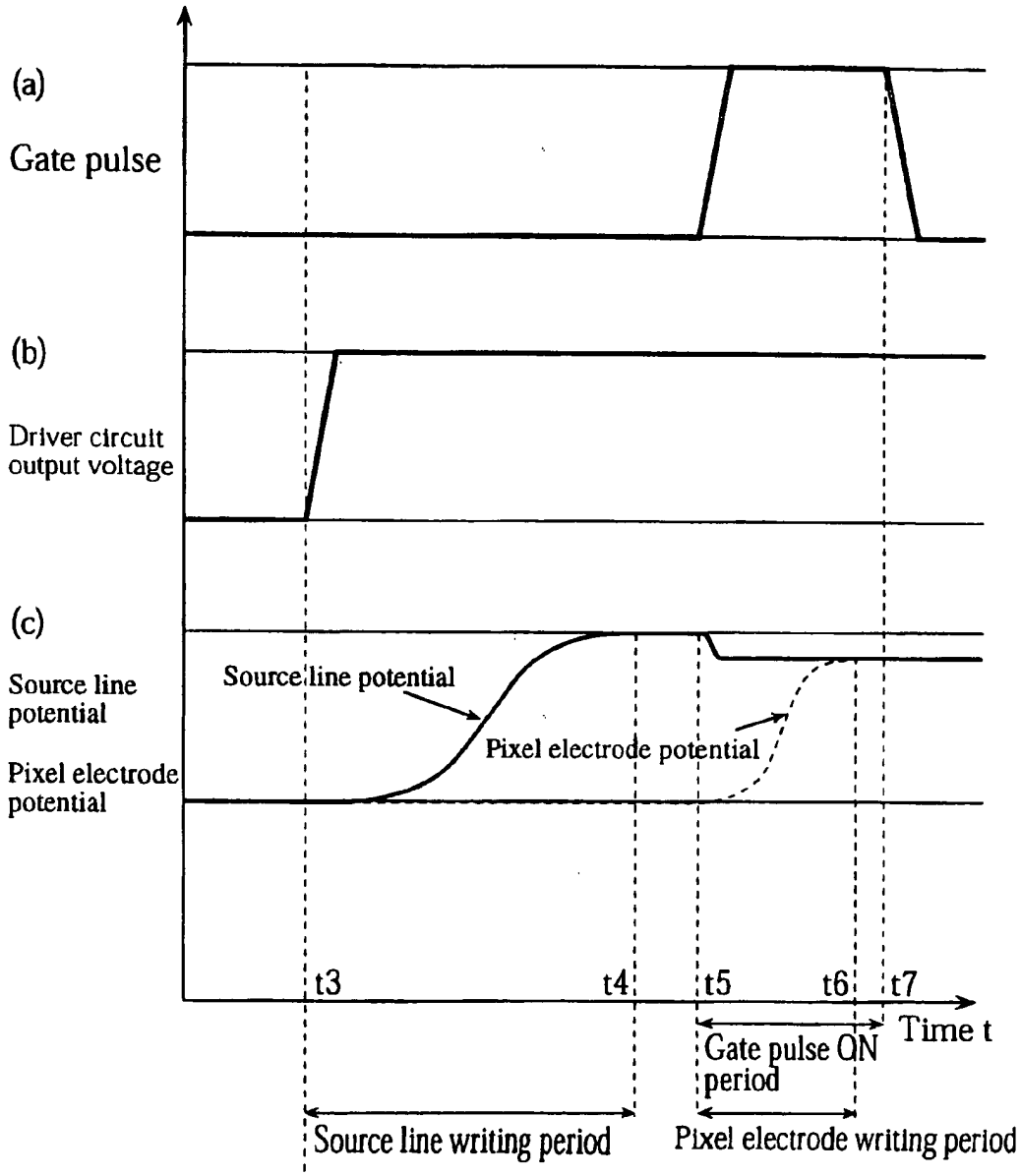

(a)
Gate pulse
(b)
Driver circuit output voltage
(c)
Source line potential
Pixel electrode potential
Source line potential
Pixel electrode potential
t1
t2
Time t
Gate pulse ON period
Source line writing period
Pixel electrode writing period
Remaining period

FIG. 8


(a)
Gate pulse
(b)
Driver circuit output voltage
(c)
Source line potential
Pixel electrode potential
Source line potential
Pixel electrode potential
t3
t4
t5
t6
t7
Time t
Gate pulse ON period
Source line writing period
Pixel electrode writing period

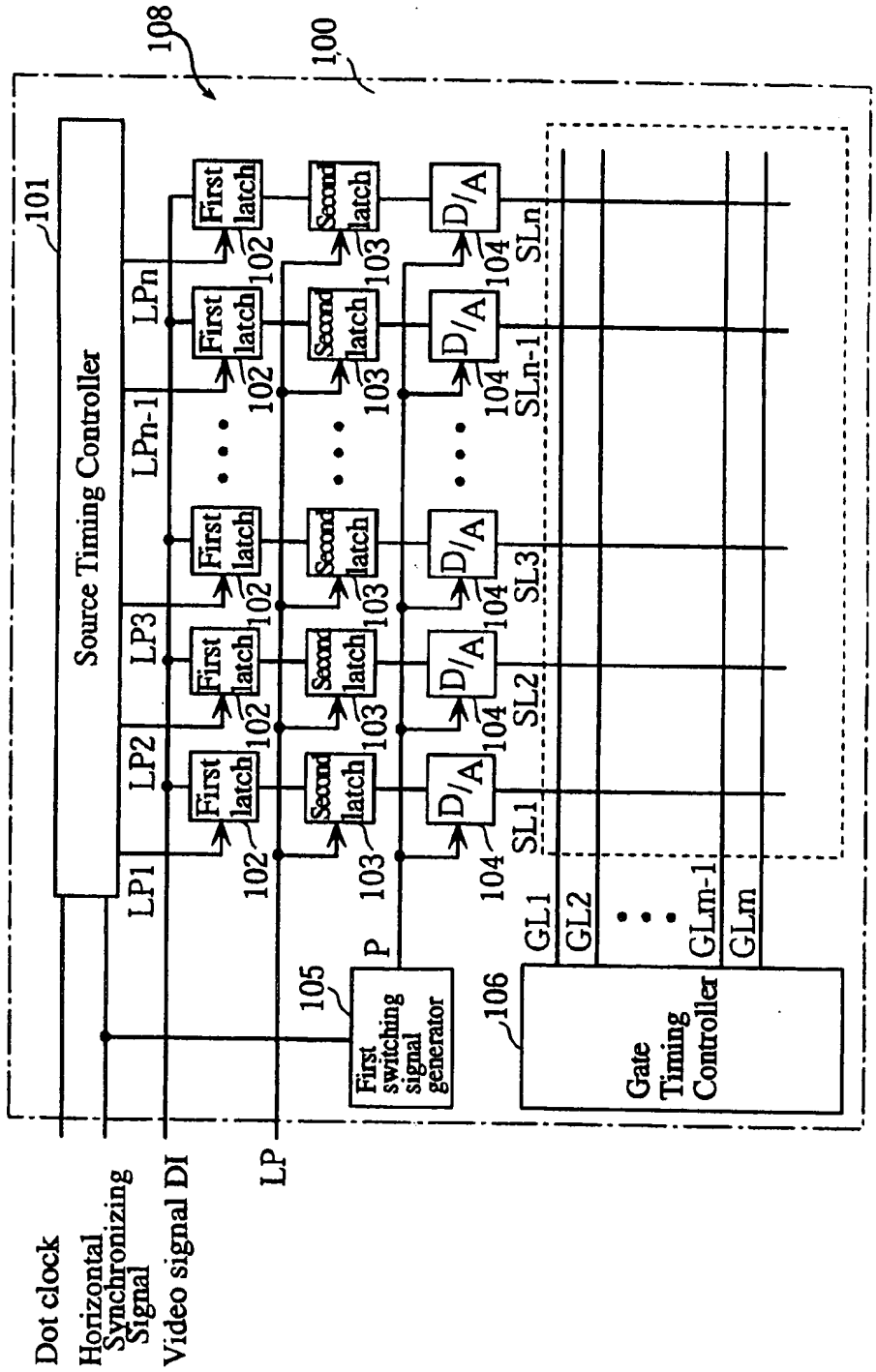

108
100
101
Source Timing Controller
LP1
LP2
LP3
LPn-1
LPn
First latch
Second latch
D/A
102
103
104
SL1
SL2
SL3
SLn-1
SLn
GL1
GL2
GLm-1
GLm
105
First switching signal generator
106
Gate Timing Controller
P
LP
Dot clock
Horizontal Synchronizing Signal
Video signal DI

FIG. 9

FIG. 10

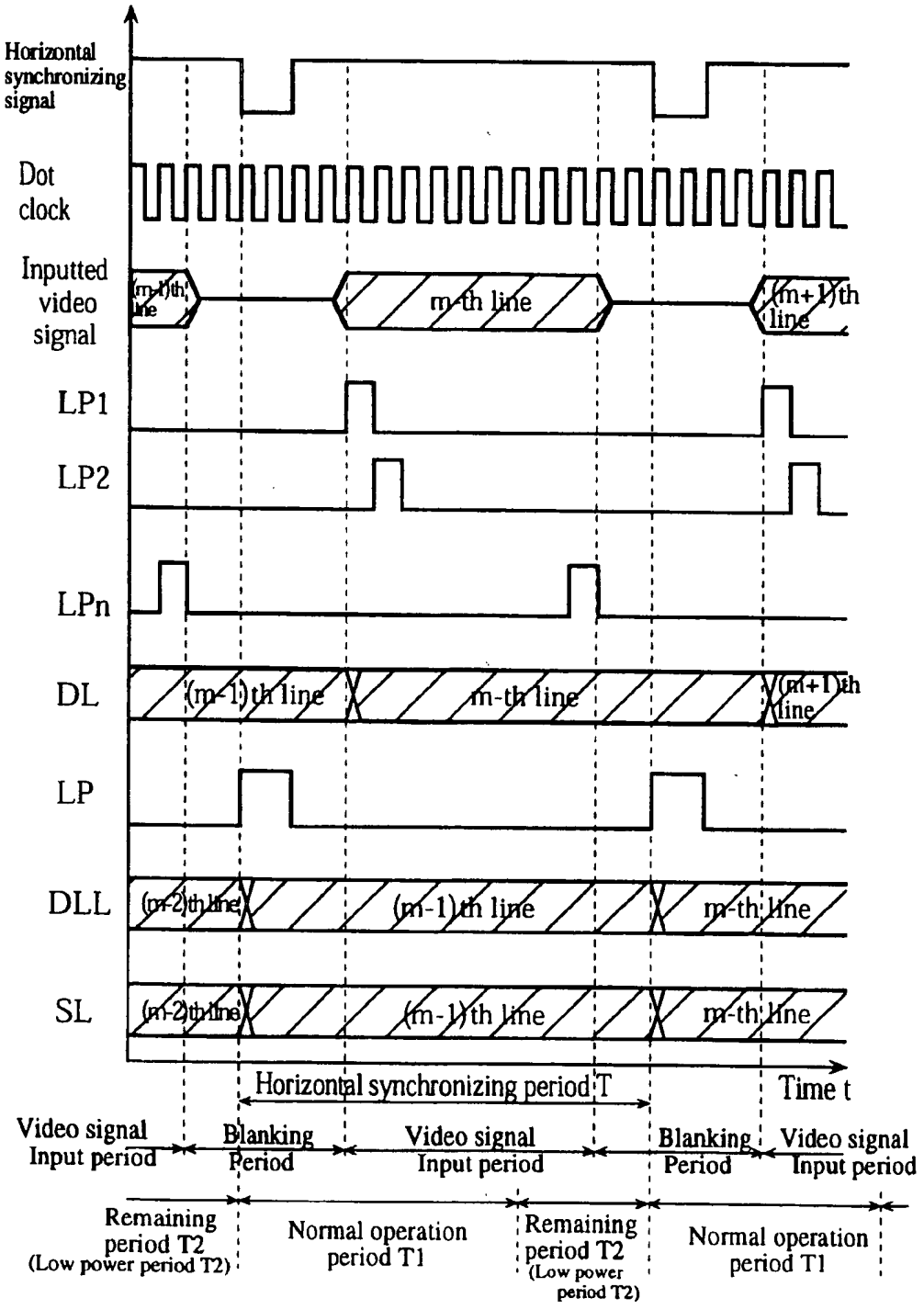

Horizontal synchronizing signal
Dot clock
Inputted video signal
(m-1)th line
m-th line
(m+1)th line
LP1
LP2
LPn
DL
(m-1)th line
m-th line
(m+1)th line
LP
DLL
(m-2)th line
(m-1)th line
m-th line
SL
(m-2)th line
(m-1)th line
m-th line
Horizontal synchronizing period T
Time t
Video signal Input period
Blanking Period
Video signal Input period
Blanking Period
Video signal Input period
Remaining period T2 (Low power period T2)
Normal operation period T1
Remaining period T2 (Low power period T2)
Normal operation period T1

FIG. 11

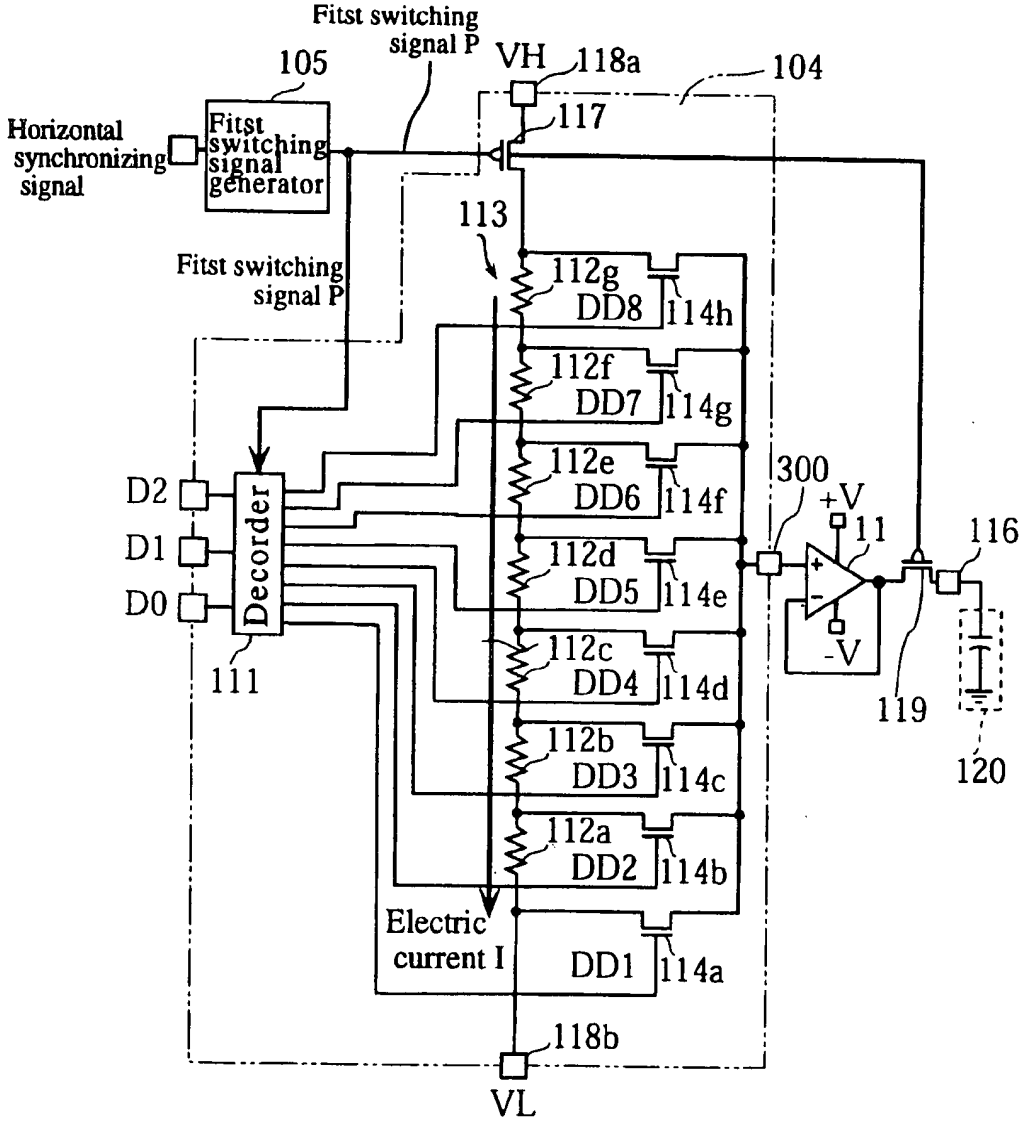

Fitst switching signal P
105
VH
118a
104
Horizontal synchronizing signal
Fitst switching signal generator
117
113
Fitst switching signal P
112g
DD8
114h
112f
DD7
114g
112e
DD6
114f
300
+V
11
116
D2
D1
D0
Decorder
112d
DD5
114e
112c
DD4
114d
-V
111
119
112b
DD3
114c
120
112a
DD2
114b
Electric current I
DD1
114a
118b
VL

Fig. 12

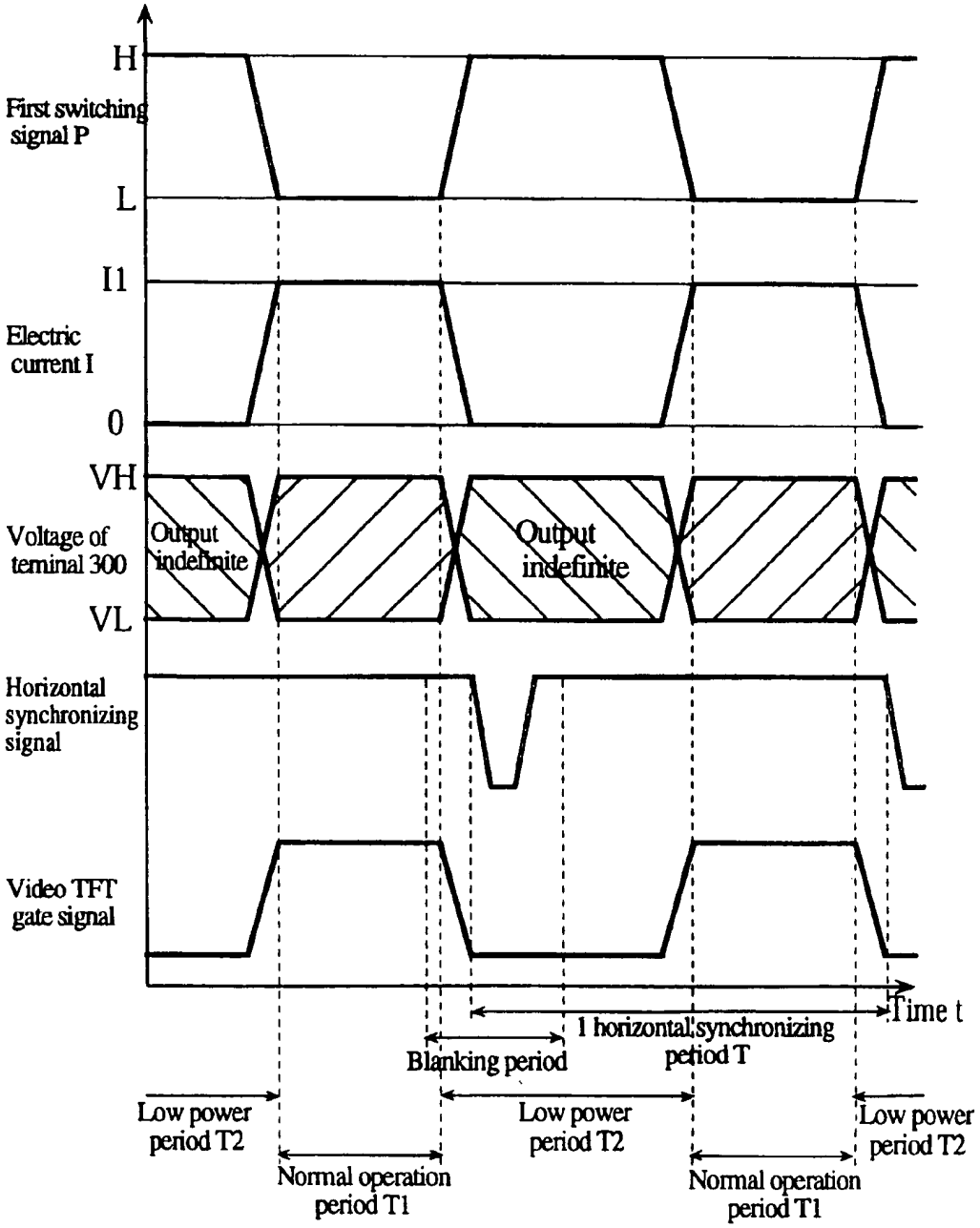

H
First switching signal P
L
I1
Electric current I
0
VH
Voltage of terminal 300
Output indefinite
Output indefinite
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
1 horizontal synchronizing period T
Blanking period
Low power period T2
Normal operation period T1
Low power period T2
Normal operation period T1
Low power period T2

FIG. 13

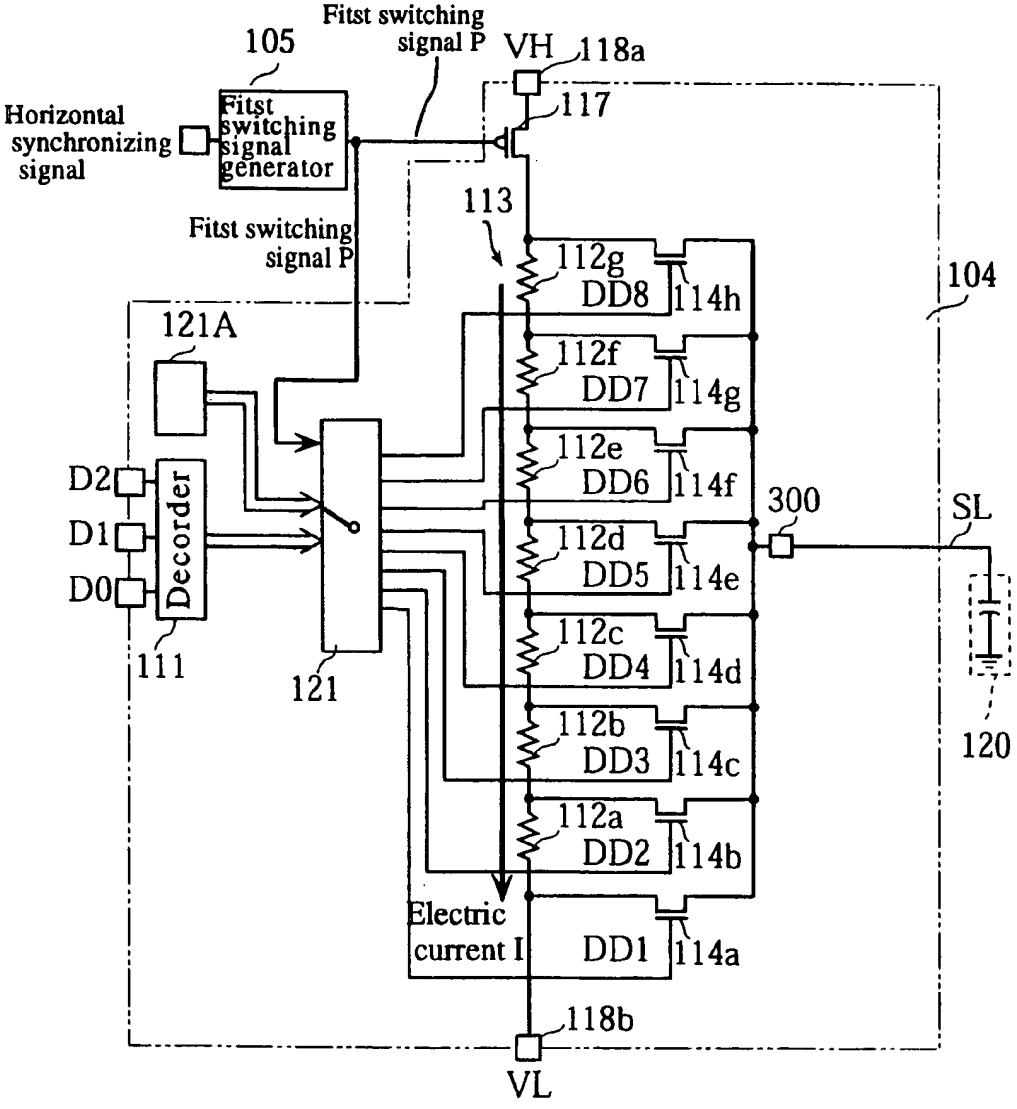

Fitst switching signal P
105
VH
118a
Horizontal synchronizing signal
Fitst switching signal generator
117
113
Fitst switching signal P
112g
DD8
114h
104
121A
112f
DD7
114g
112e
DD6
114f
D2
D1
D0
Decorder
300
SL
112d
DD5
114e
112c
DD4
114d
111
121
120
112b
DD3
114c
112a
DD2
114b
Electric current I
DD1
114a
118b
VL

FIG. 14

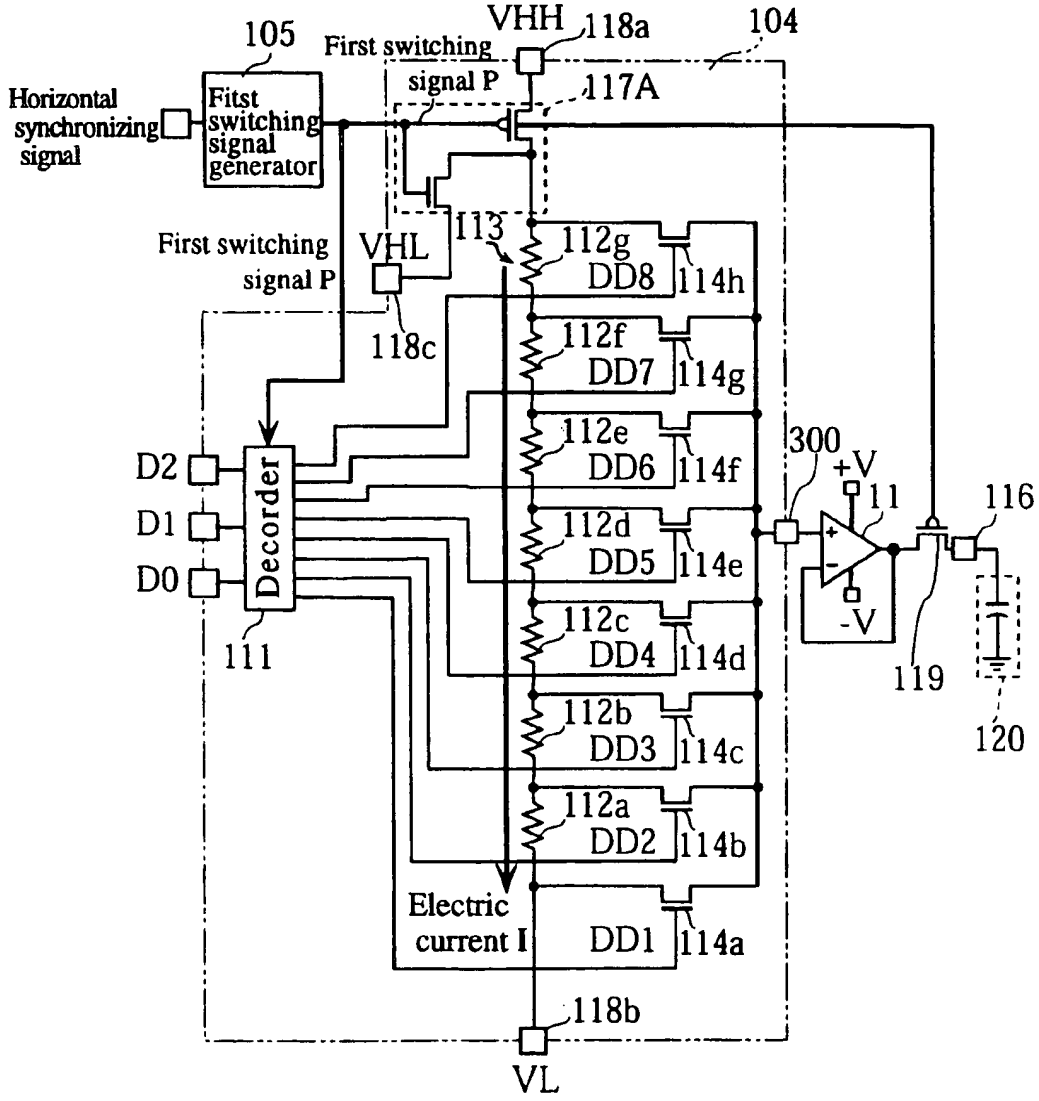

105
First switching signal P
VHH
118a
104
Horizontal synchronizing signal
Fitst switching signal generator
117A
First switching signal P
VHL
113
112g
DD8
114h
118c
112f
DD7
114g
112e
DD6
114f
300
+V
11
116
D2
D1
D0
Decorder
112d
DD5
114e
112c
DD4
114d
-V
119
111
112b
DD3
114c
120
112a
DD2
114b
Electric current I
DD1
114a
118b
VL

FIG. 15

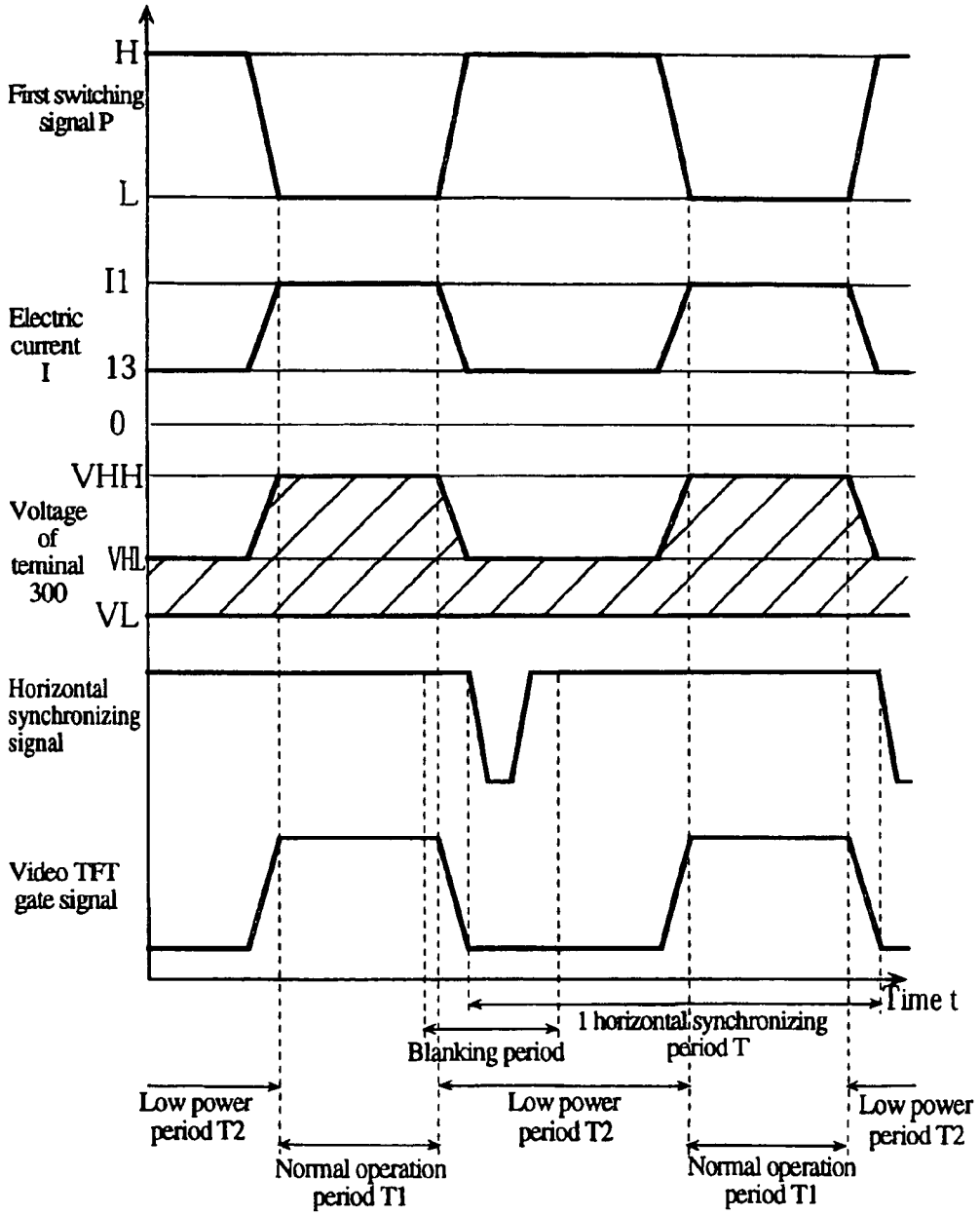
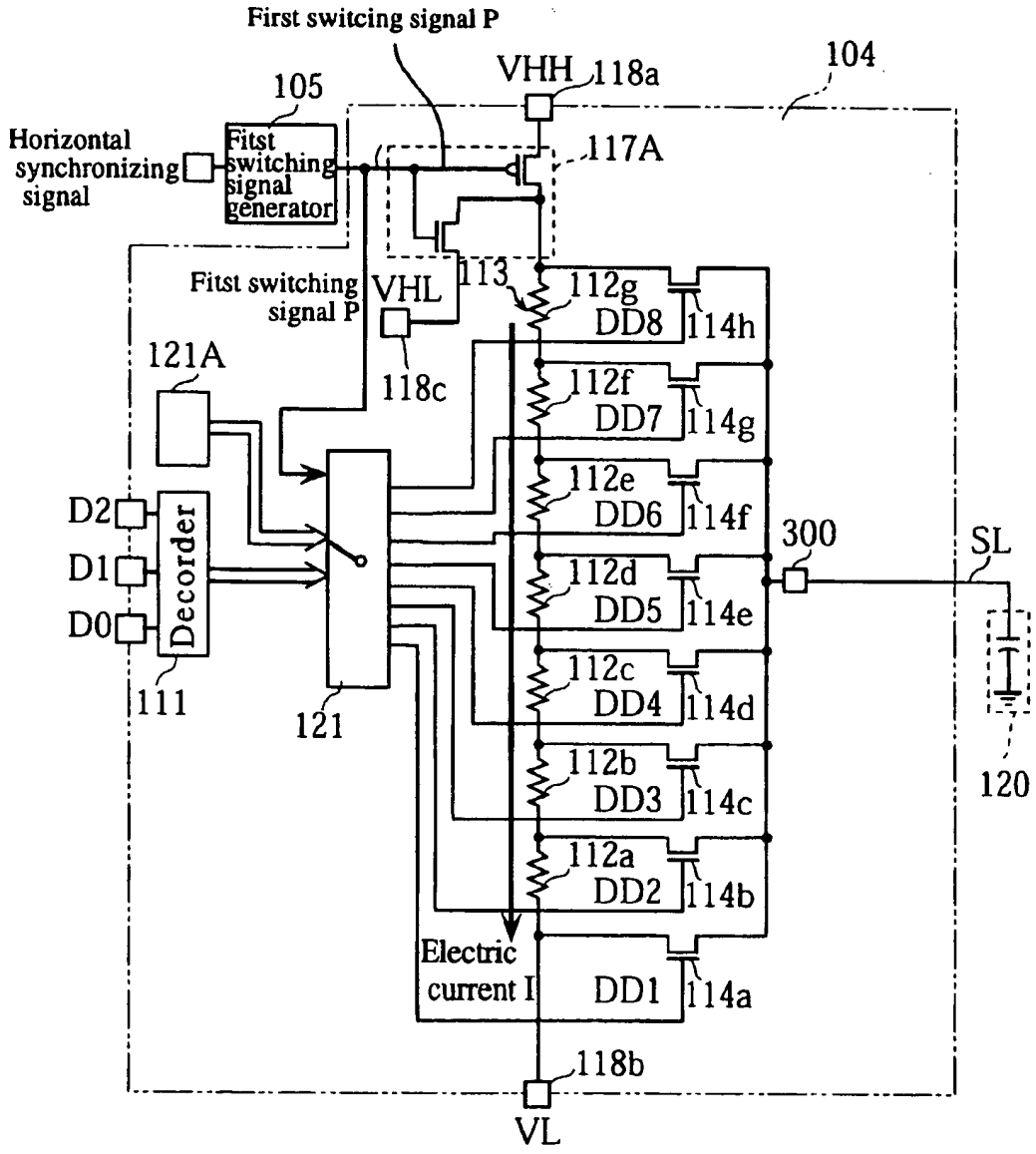

H
First switching signal P
L
I1
Electric current I
13
0
VHH
Voltage of terminal 300
VHL
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
1 horizontal synchronizing period T
Blanking period
Low power period T2
Normal operation period T1
Low power period T2
Normal operation period T1
Low power period T2

FIG. 16


First switcing signal P
VHH
118a
104
105
Horizontal synchronizing signal
Fitst switching signal generator
117A
Fitst switching signal P
VHL
113
112g
DD8
114h
121A
118c
112f
DD7
114g
112e
DD6
114f
D2
D1
D0
Decorder
300
SL
112d
DD5
114e
112c
DD4
114d
111
121
112b
DD3
114c
120
112a
DD2
114b
Electric current I
DD1
114a
118b
VL

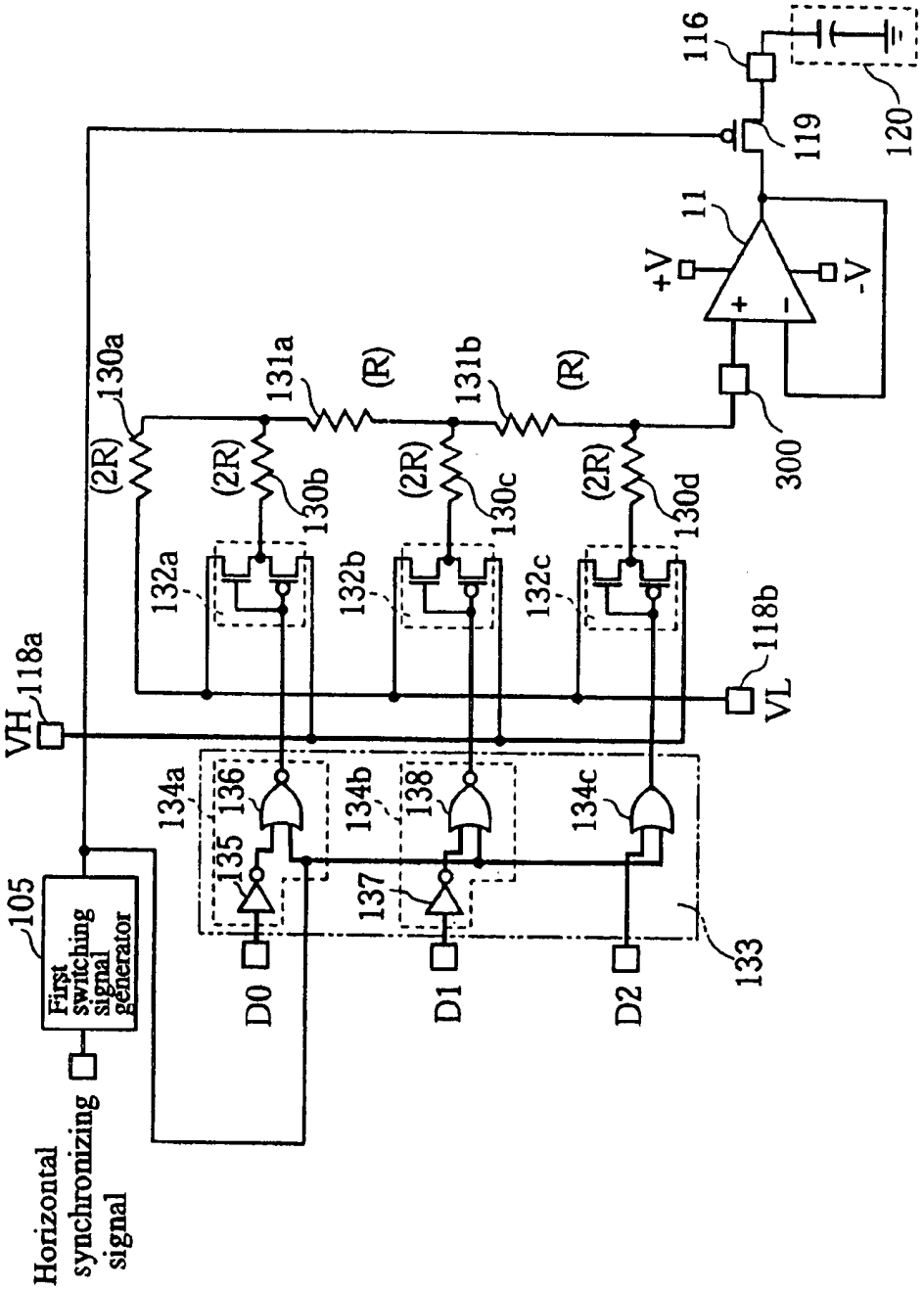

116
119
120
11
+V
-V
300
130a
131a
(R)
131b
(R)
(2R)
130b
130c
130d
132a
132b
132c
118a
VH
118b
VL
134a
134b
134c
136
138
135
137
133
105
First switching signal generator
Horizontal synchronizing signal
D0
D1
D2

FIG. 17

FIG. 18

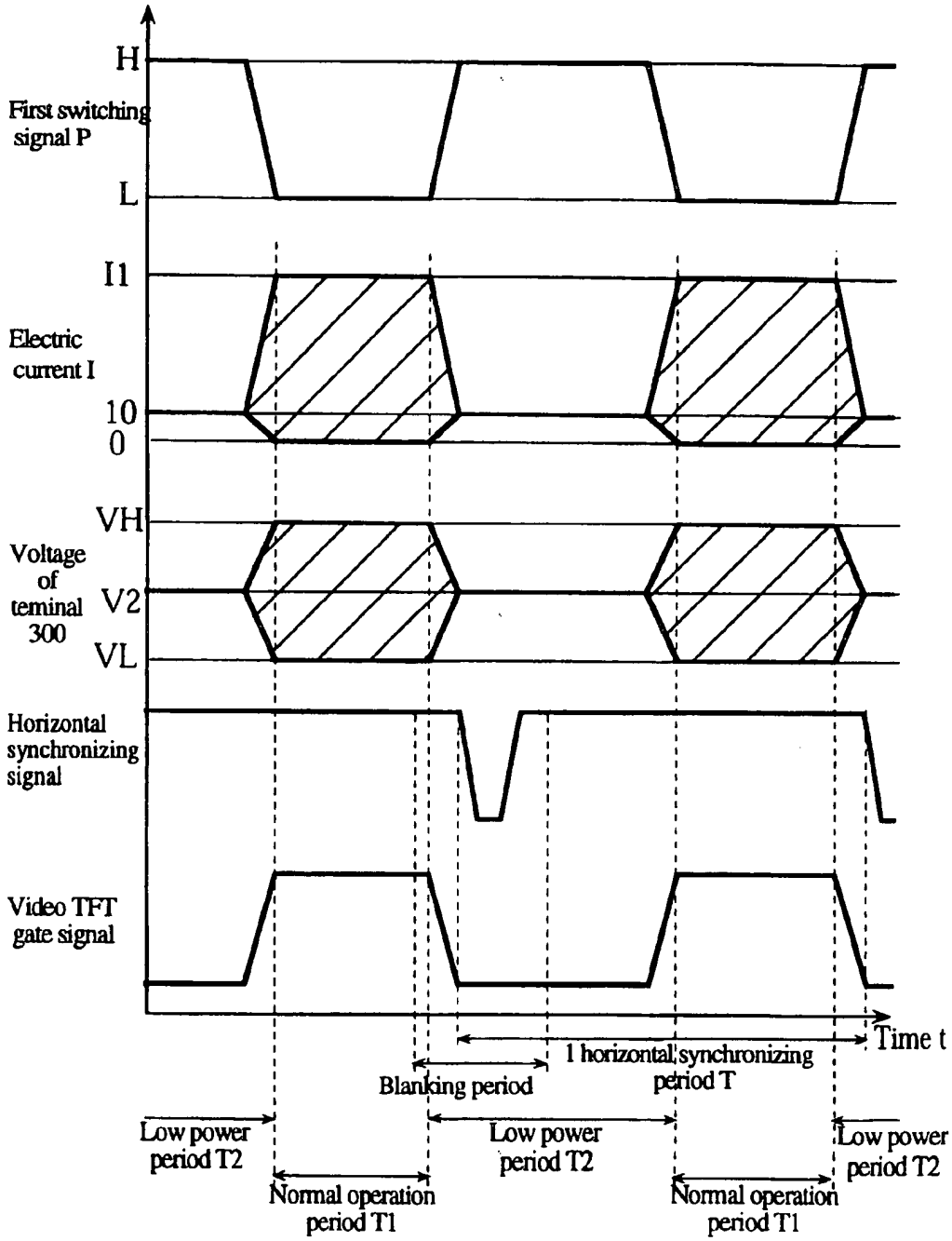
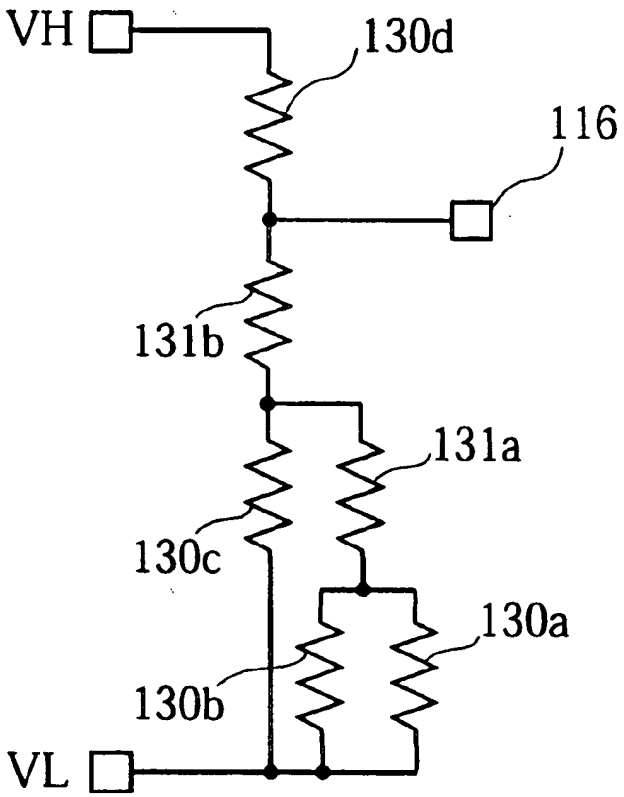

H
First switching signal P
L
I1
Electric current I
10
0
VH
Voltage of teminal 300
V2
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
1 horizontal synchronizing period T
Blanking period
Low power period T2
Normal operation period T1
Low power period T2
Normal operation period T1
Low power period T2

FIG. 19



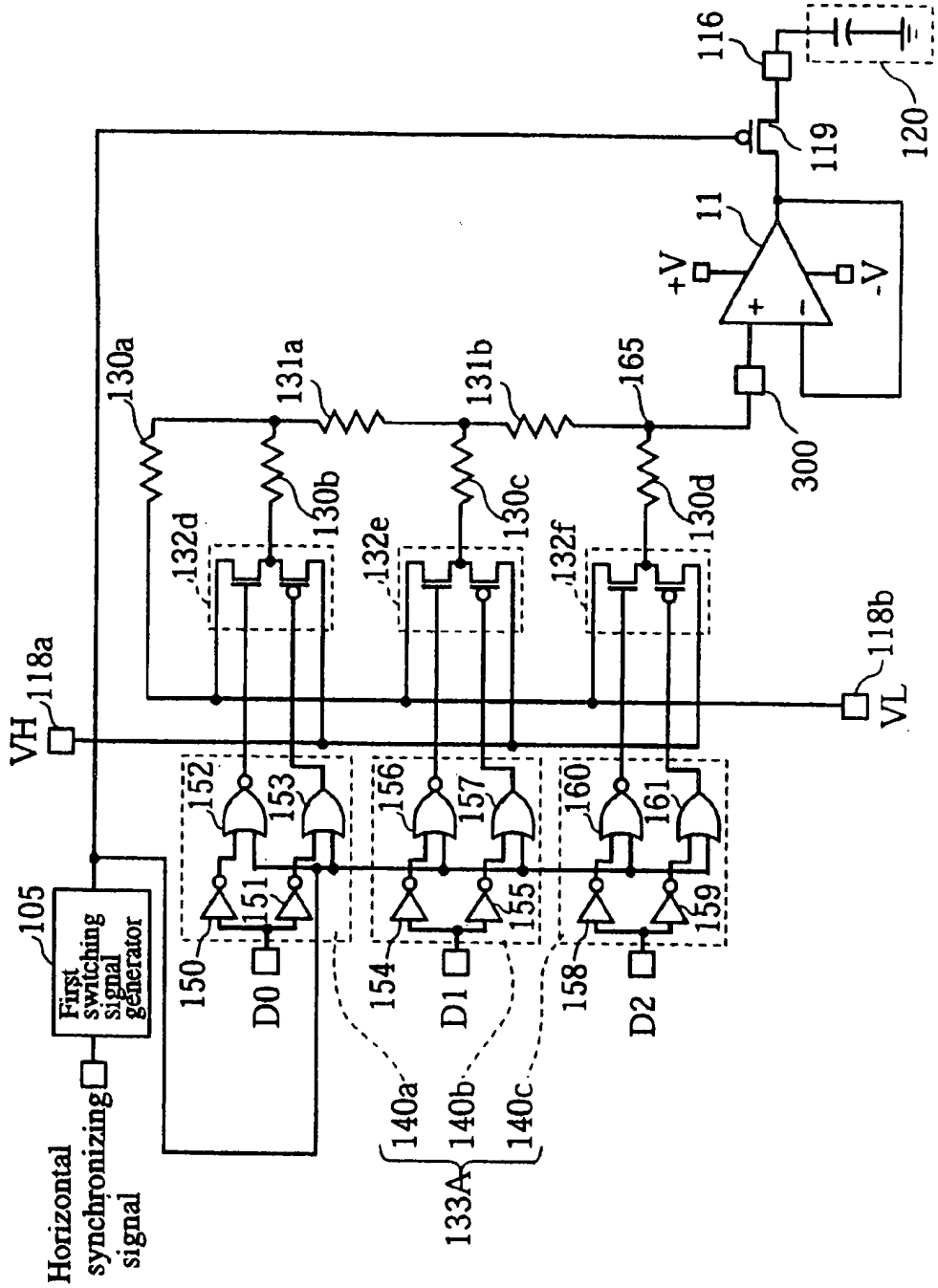

116
120
119
11
+V
-V
130a
131a
131b
165
300
130b
130c
130d
132d
132e
132f
118b
VL
118a
VH
152
153
156
157
160
161
151
155
159
105
First switching signal generator
150
154
158
D0
D1
D2
140a
140b
140c
133A
Horizontal synchronizing signal

FIG. 20

FIG. 21

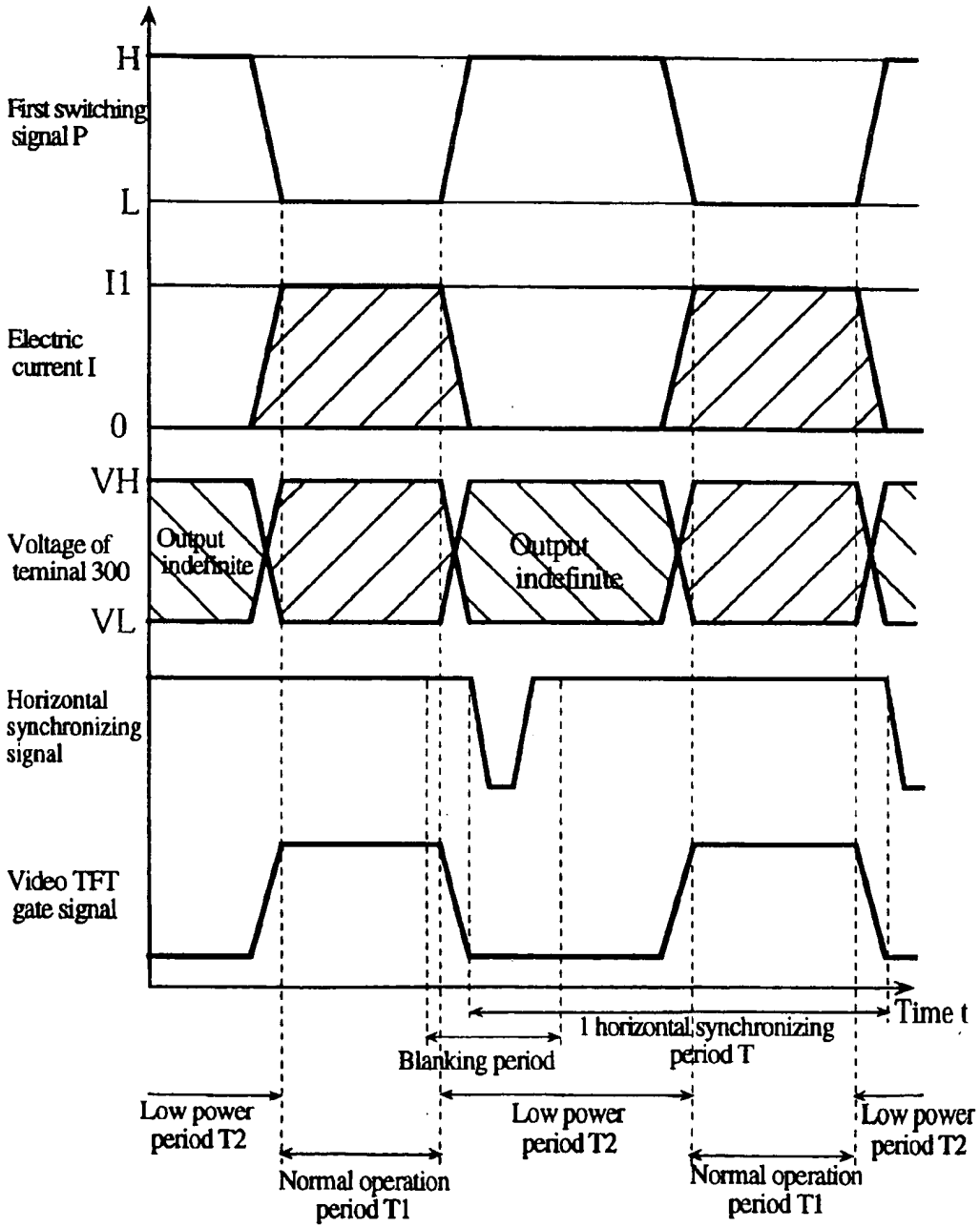

H
First switching signal P
L
I1
Electric current I
0
VH
Voltage of teminal 300
Output indefinite
Output indefinite
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
1 horizontal synchronizing period T
Blanking period
Low power period T2
Normal operation period T1
Low power period T2
Normal operation period T1
Low power period T2

FIG. 22

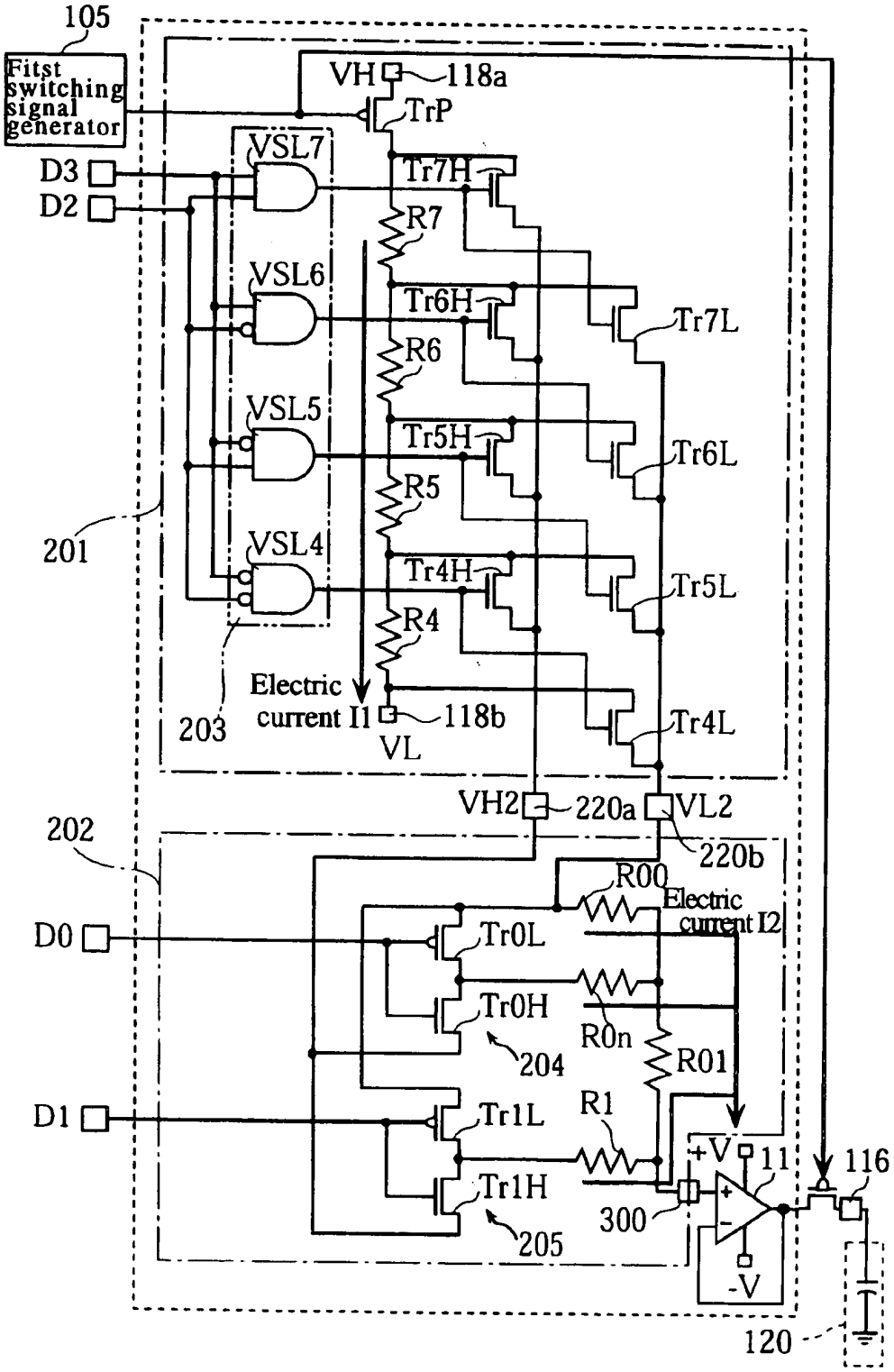

105
Fitst switching signal generator
VH
118a
TrP
VSL7
Tr7H
D3
D2
R7
VSL6
Tr6H
Tr7L
R6
VSL5
Tr5H
Tr6L
R5
201
VSL4
Tr4H
Tr5L
R4
Electric current I1
118b
VL
203
Tr4L
VH2
220a
VL2
220b
202
R00
Electric current I2
D0
Tr0L
Tr0H
R0n
R01
204
D1
Tr1L
R1
+V
11
116
Tr1H
300
205
-V
120

FIG. 23

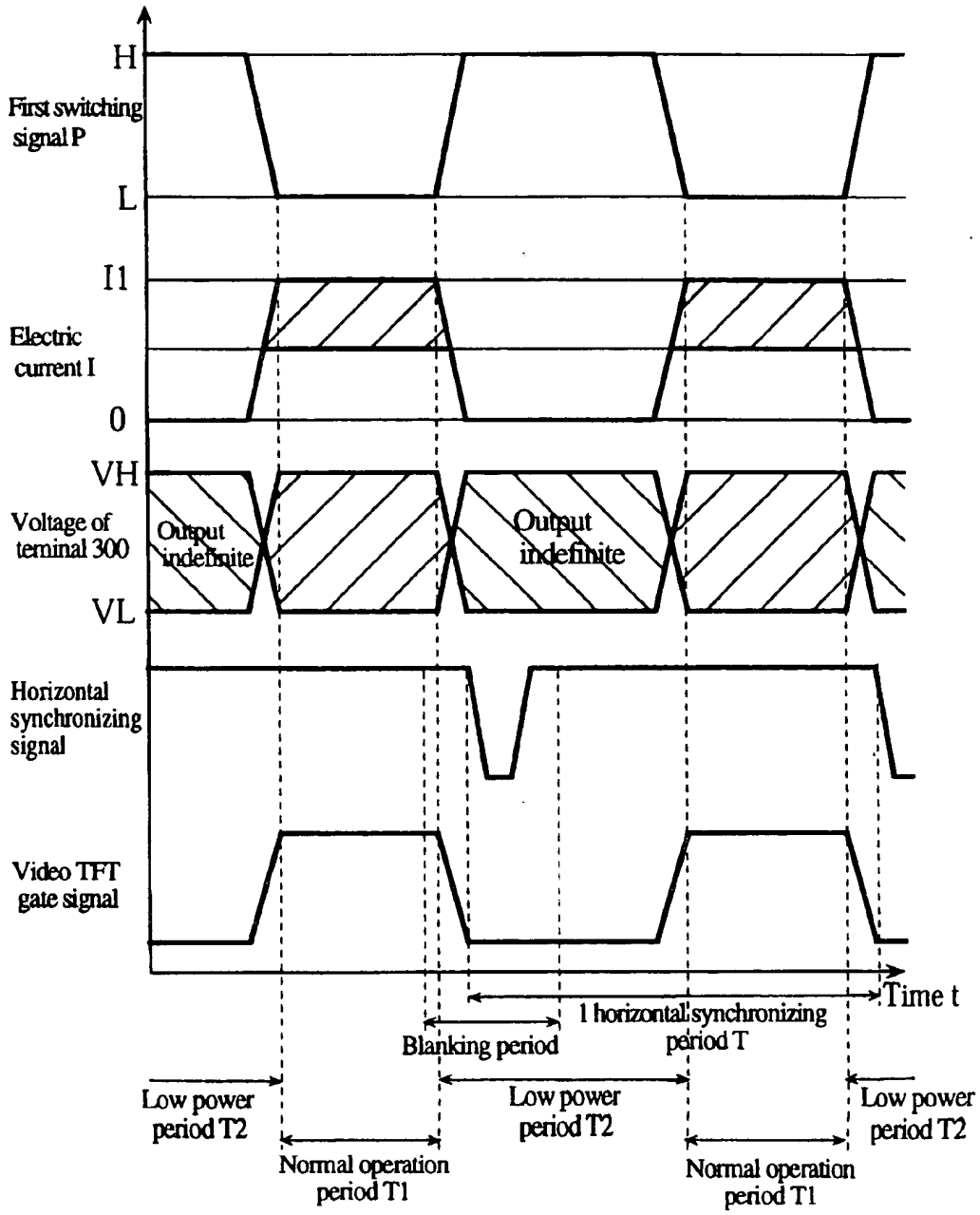

H
First switching signal P
L
I1
Electric current I
0
VH
Voltage of terminal 300
Output indefinite
Output indefinite
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
1 horizontal synchronizing period T
Blanking period
Low power period T2
Low power period T2
Low power period T2
Normal operation period T1
Normal operation period T1

FIG. 24

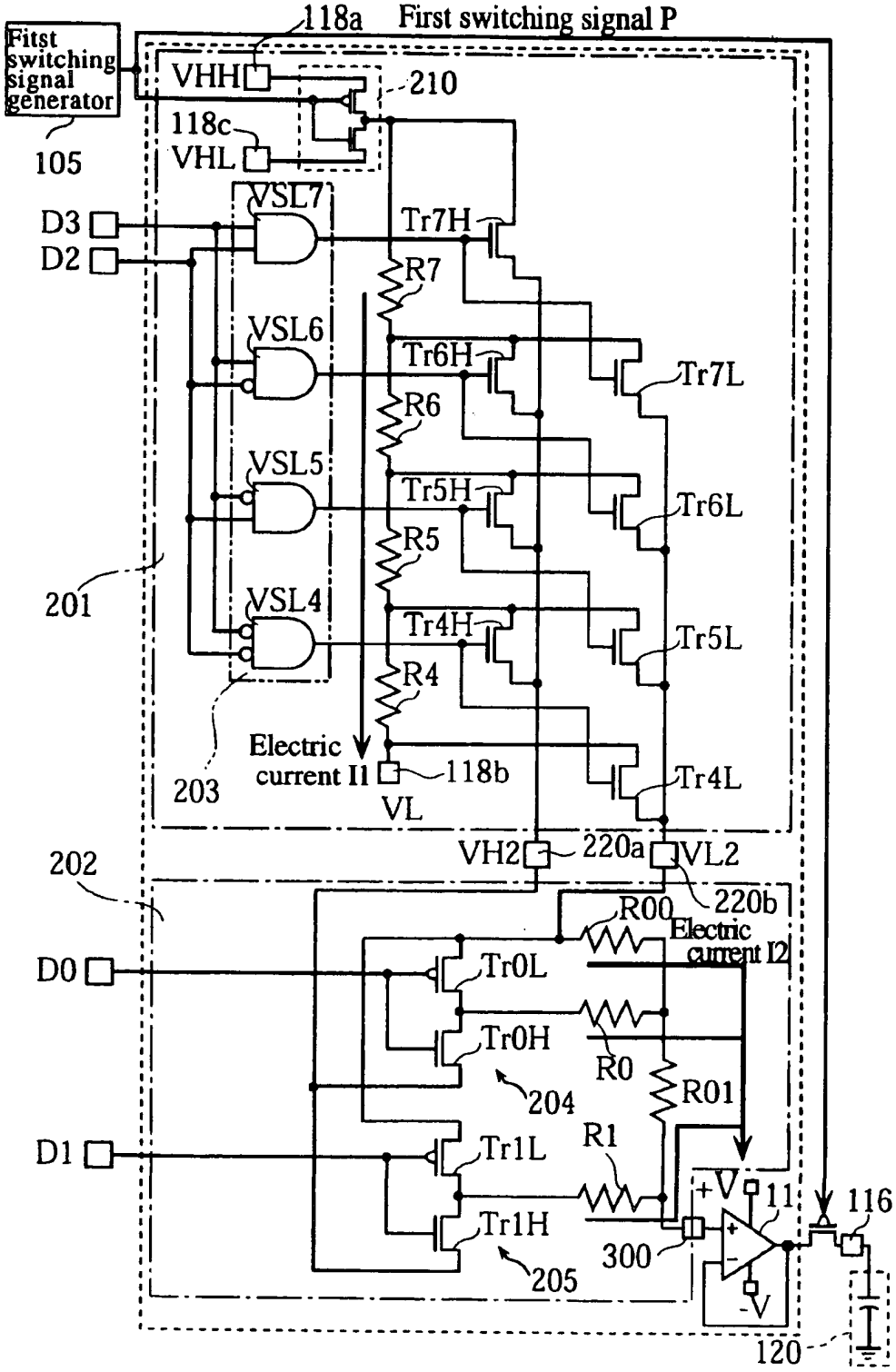

118a
First switching signal P
Fitst switching signal generator
105
VHH
210
118c
VHL
VSL7
Tr7H
D3
D2
R7
VSL6
Tr6H
Tr7L
R6
VSL5
Tr5H
Tr6L
R5
201
VSL4
Tr4H
Tr5L
R4
Electric current I1
118b
VL
203
Tr4L
VH2
220a
VL2
202
220b
R00
Electric current I2
D0
Tr0L
Tr0H
R0
R01
204
D1
Tr1L
R1
+V
11
116
Tr1H
300
205
-V
120

FIG. 25

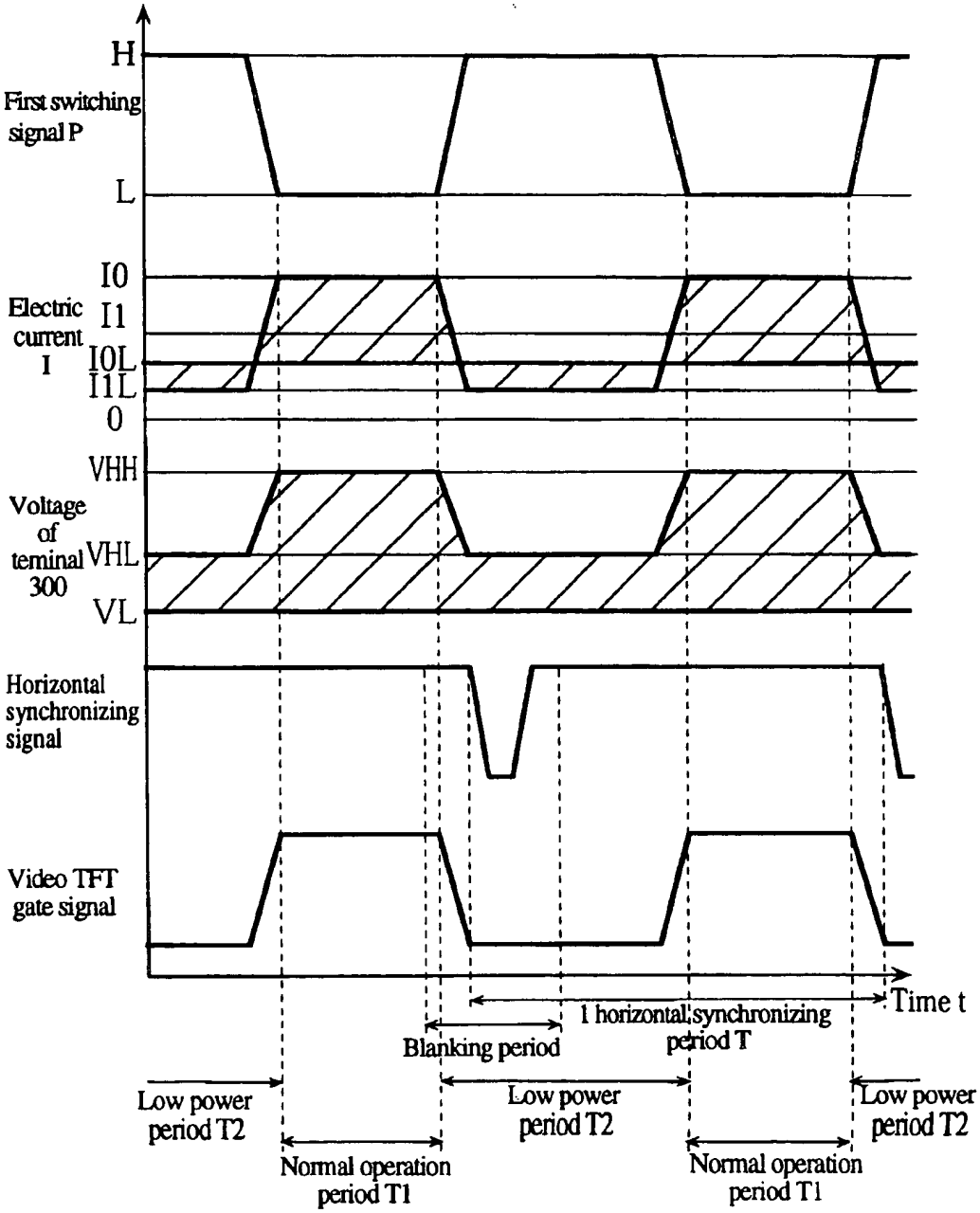

H
First switching signal P
L
I0
Electric current I
I1
I0L
I1L
0
VHH
Voltage of teminal 300
VHL
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
1 horizontal synchronizing period T
Blanking period
Low power period T2
Normal operation period T1
Low power period T2
Normal operation period T1
Low power period T2

FIG. 26

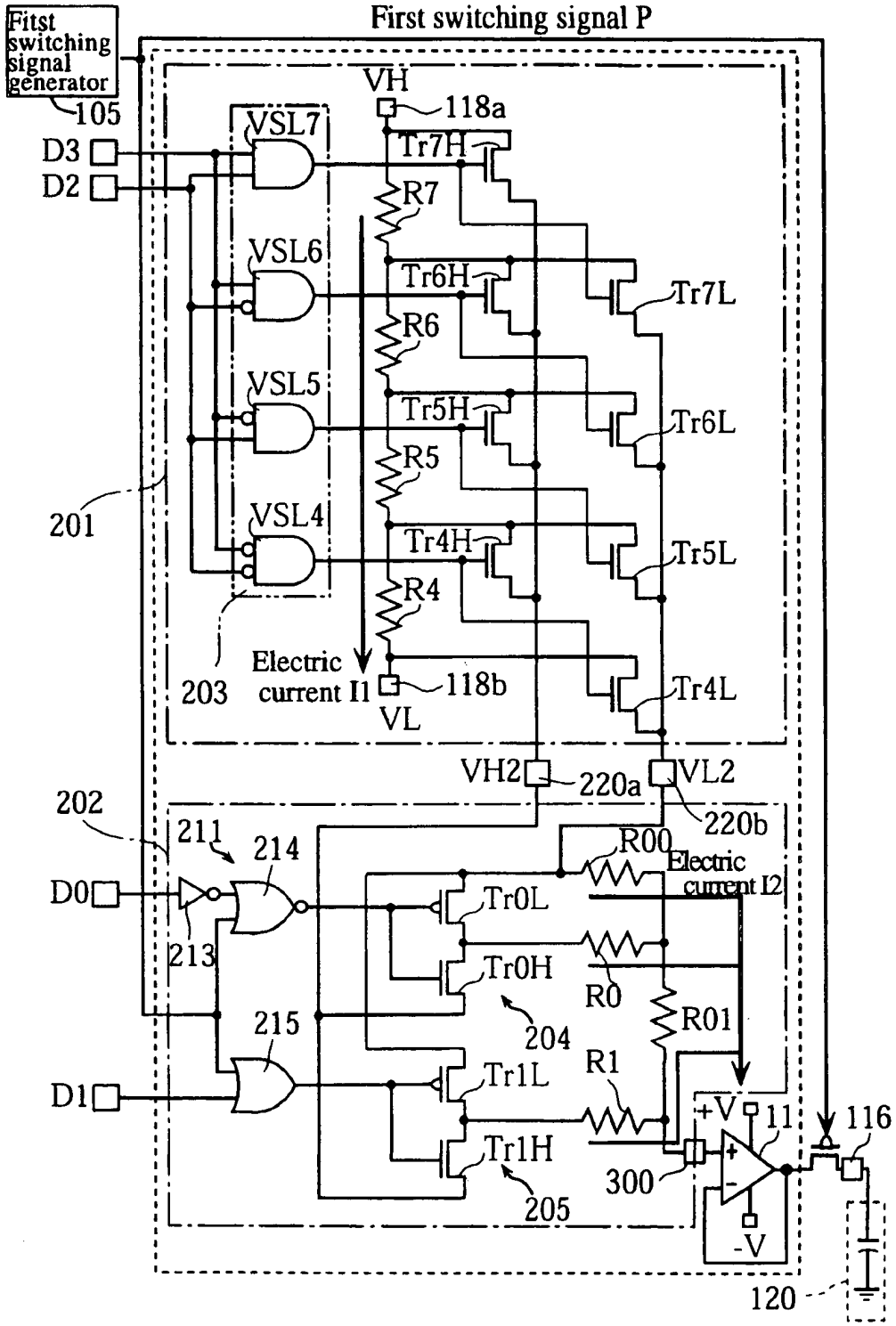

Fitst switching signal generator
105
First switching signal P
VH
118a
VSL7
Tr7H
D3
D2
R7
VSL6
Tr6H
Tr7L
R6
VSL5
Tr5H
Tr6L
R5
201
VSL4
Tr4H
Tr5L
R4
Electric current I1
203
118b
Tr4L
VL
VH2
220a
VL2
220b
202
211
214
R00
Electric current I2
D0
Tr0L
213
Tr0H
R0
R01
215
204
D1
Tr1L
R1
+V
11
116
Tr1H
300
205
-V
120

FIG. 27

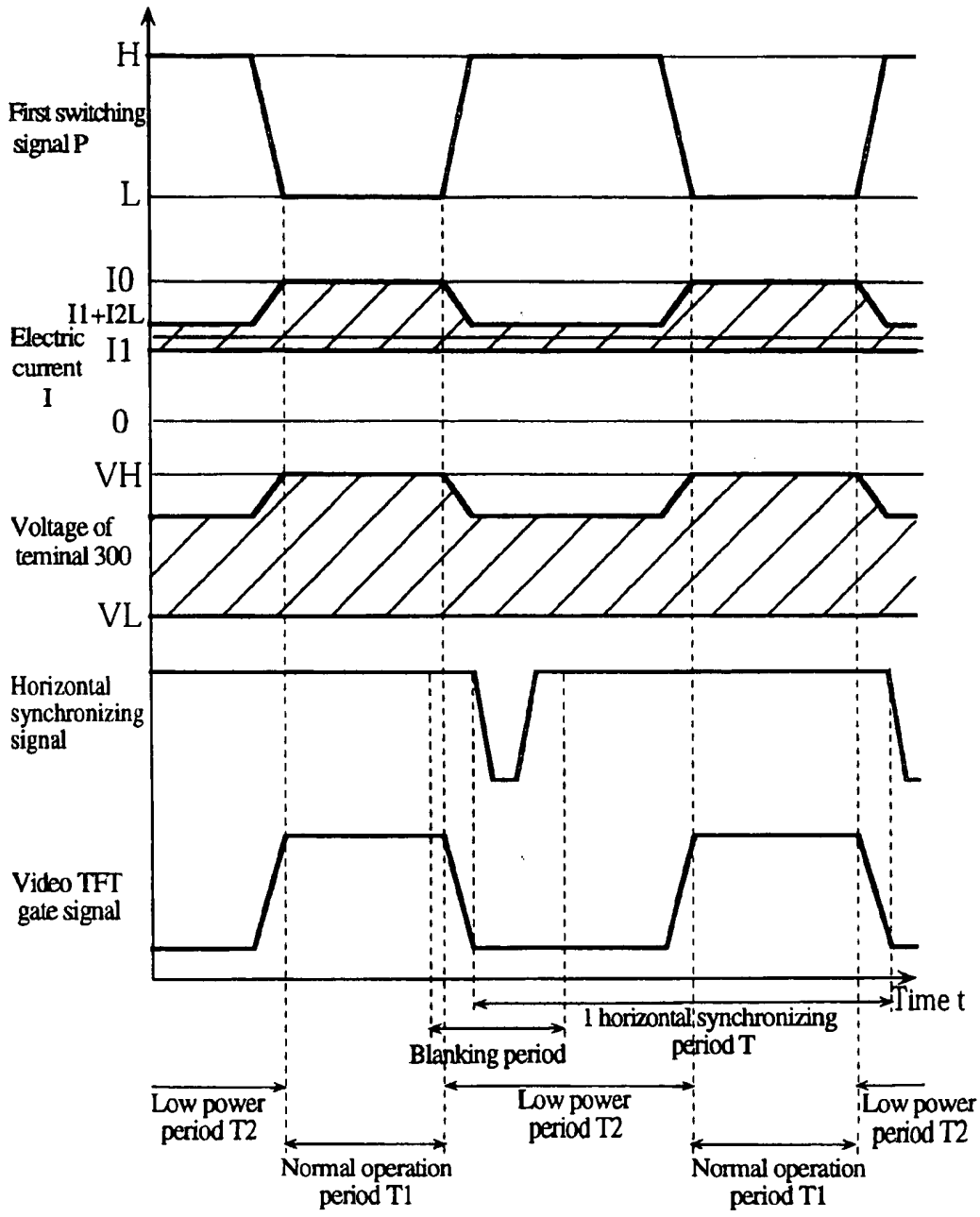

H
First switching signal P
L
I0
I1+I2L
Electric current I
I1
0
VH
Voltage of terminal 300
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
1 horizontal synchronizing period T
Blanking period
Low power period T2
Normal operation period T1
Low power period T2
Normal operation period T1
Low power period T2

FIG. 28

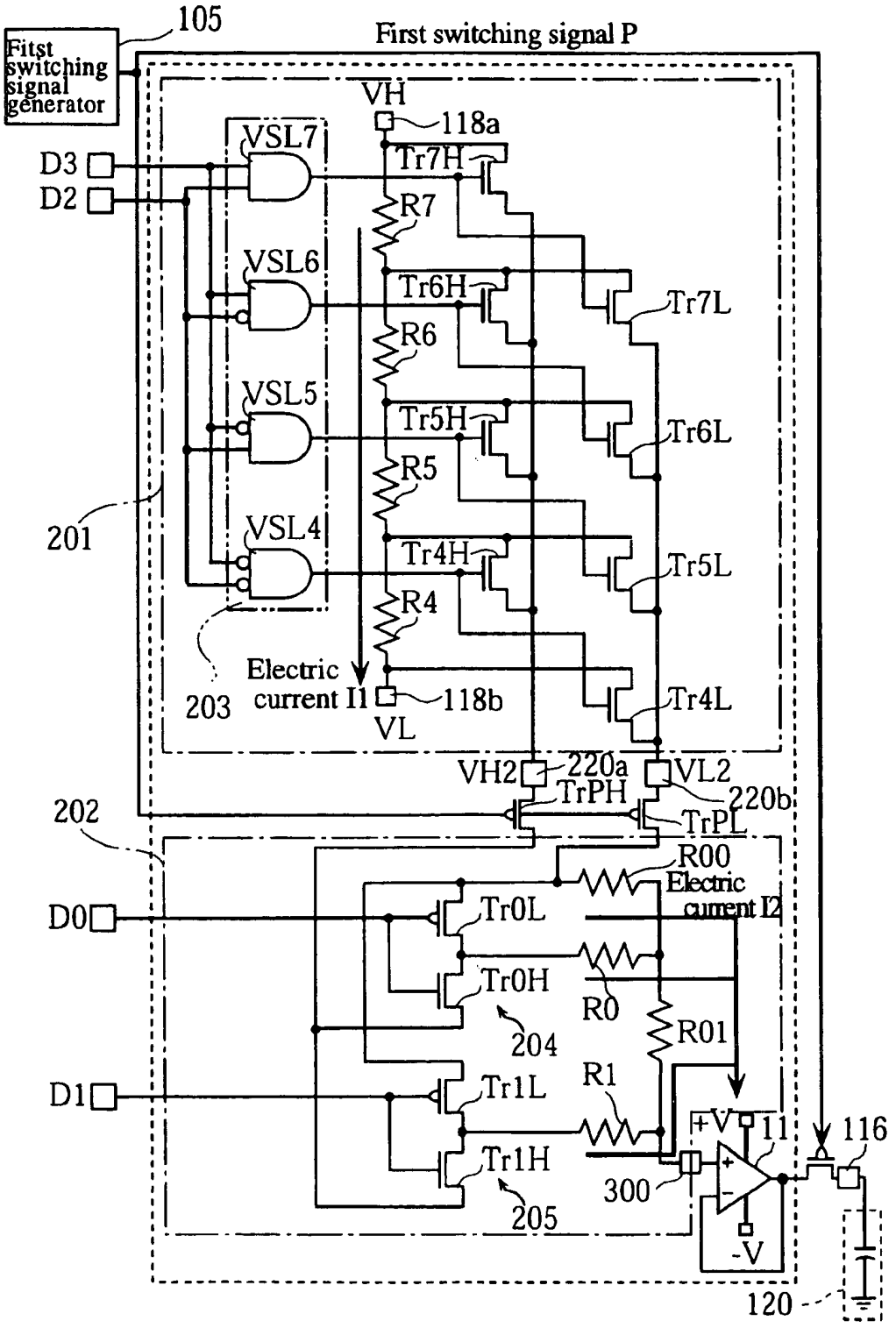

105
Fitst switching signal generator
First switching signal P
VH
118a
VSL7
Tr7H
D3
D2
R7
VSL6
Tr6H
Tr7L
R6
VSL5
Tr5H
Tr6L
R5
201
VSL4
Tr4H
Tr5L
R4
Electric current I1
203
118b
Tr4L
VL
VH2
220a
VL2
TrPH
220b
202
TrPL
R00
Electric current I2
D0
Tr0L
Tr0H
R0
R01
204
D1
Tr1L
R1
+V
11
116
Tr1H
300
205
-V
120

FIG. 29

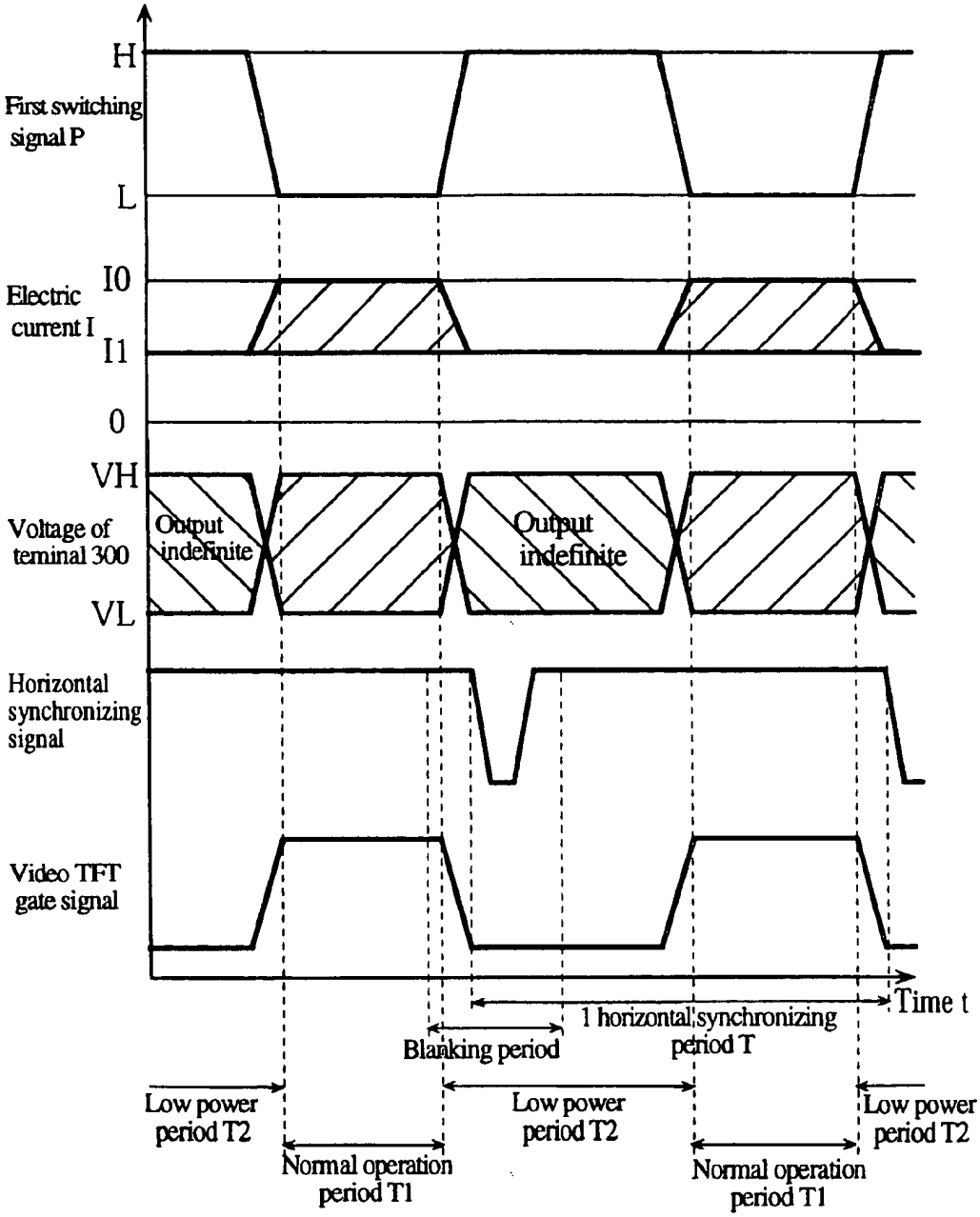

H
First switching signal P
L
Electric current I
I0
I1
0
VH
Voltage of terminal 300
Output indefinite
Output indefinite
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
1 horizontal synchronizing period T
Blanking period
Low power period T2
Low power period T2
Low power period T2
Normal operation period T1
Normal operation period T1

FIG. 30

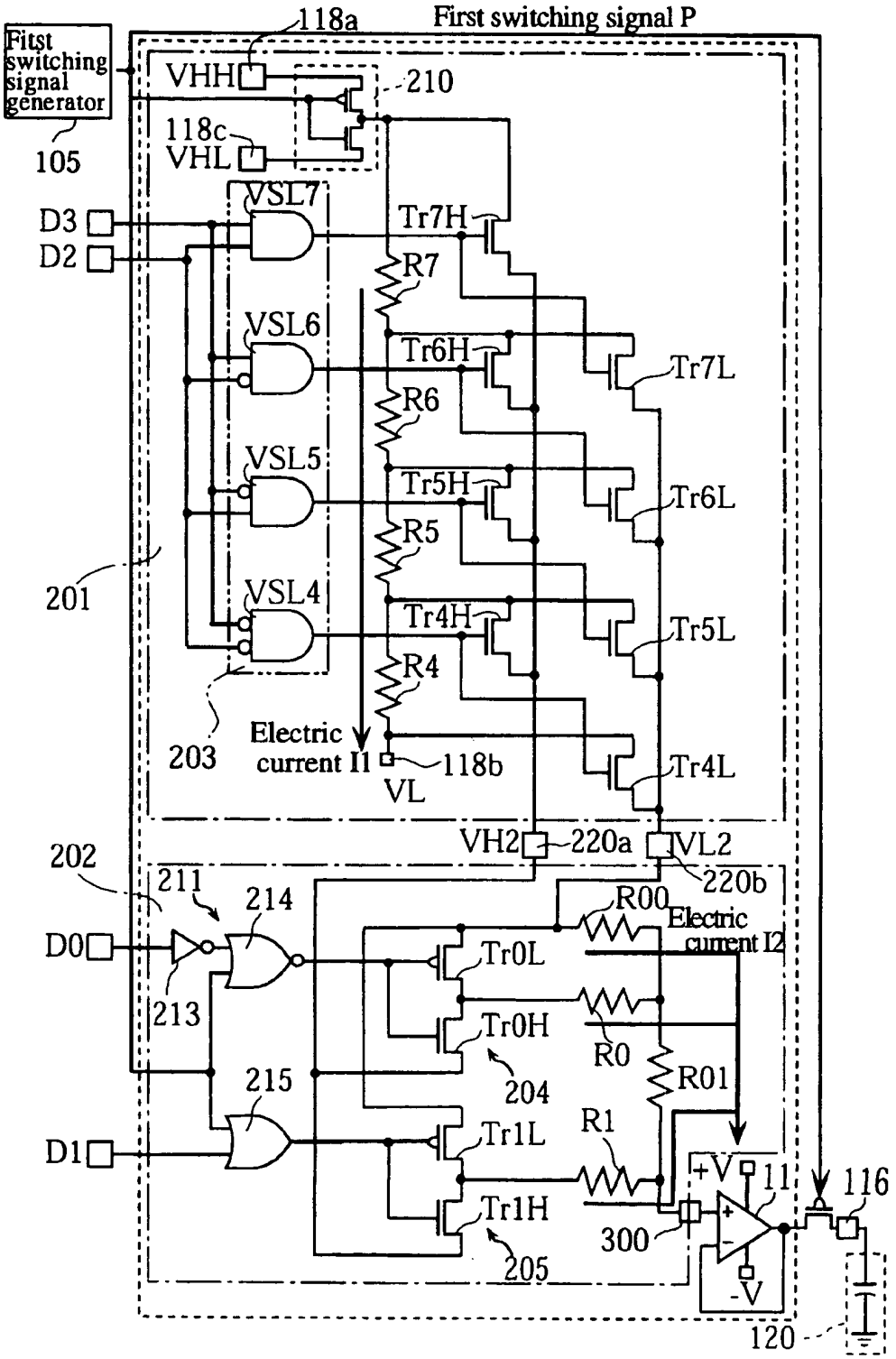

Fitst switching signal generator
105
118a
First switching signal P
VHH
210
118c
VHL
VSL7
Tr7H
D3
D2
R7
VSL6
Tr6H
Tr7L
R6
VSL5
Tr5H
Tr6L
R5
201
VSL4
Tr4H
Tr5L
R4
203
Electric current I1
118b
VL
Tr4L
VH2
220a
VL2
220b
202
211
214
R00
Electric current I2
D0
Tr0L
213
Tr0H
R0
R01
204
215
R1
D1
Tr1L
+V
11
116
Tr1H
300
205
-V
120

FIG. 31

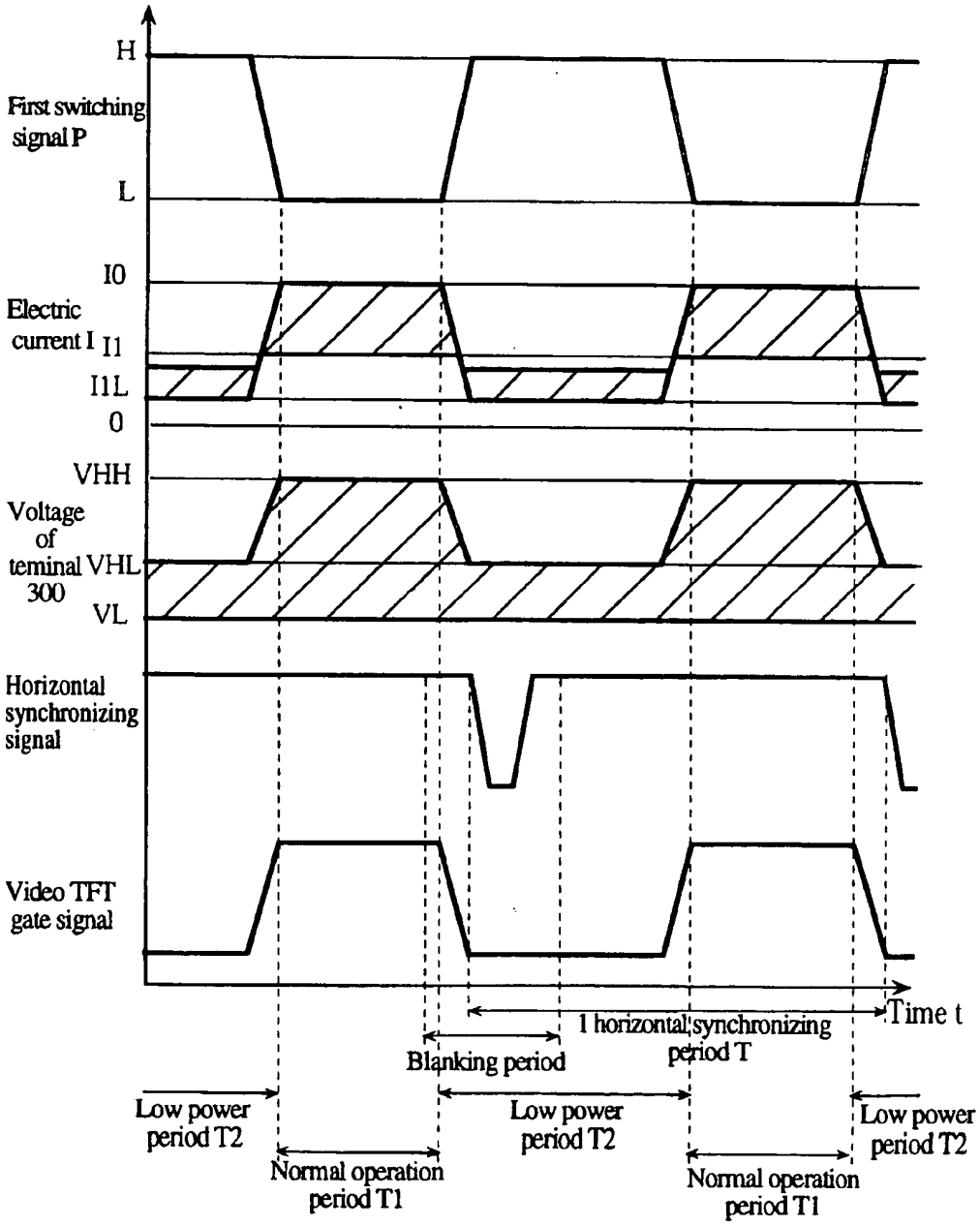

H
First switching signal P
L
I0
Electric current I
I1
I1L
0
VHH
Voltage of teminal 300
VHL
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
1 horizontal synchronizing period T
Blanking period
Low power period T2
Normal operation period T1
Low power period T2
Normal operation period T1
Low power period T2

FIG. 32

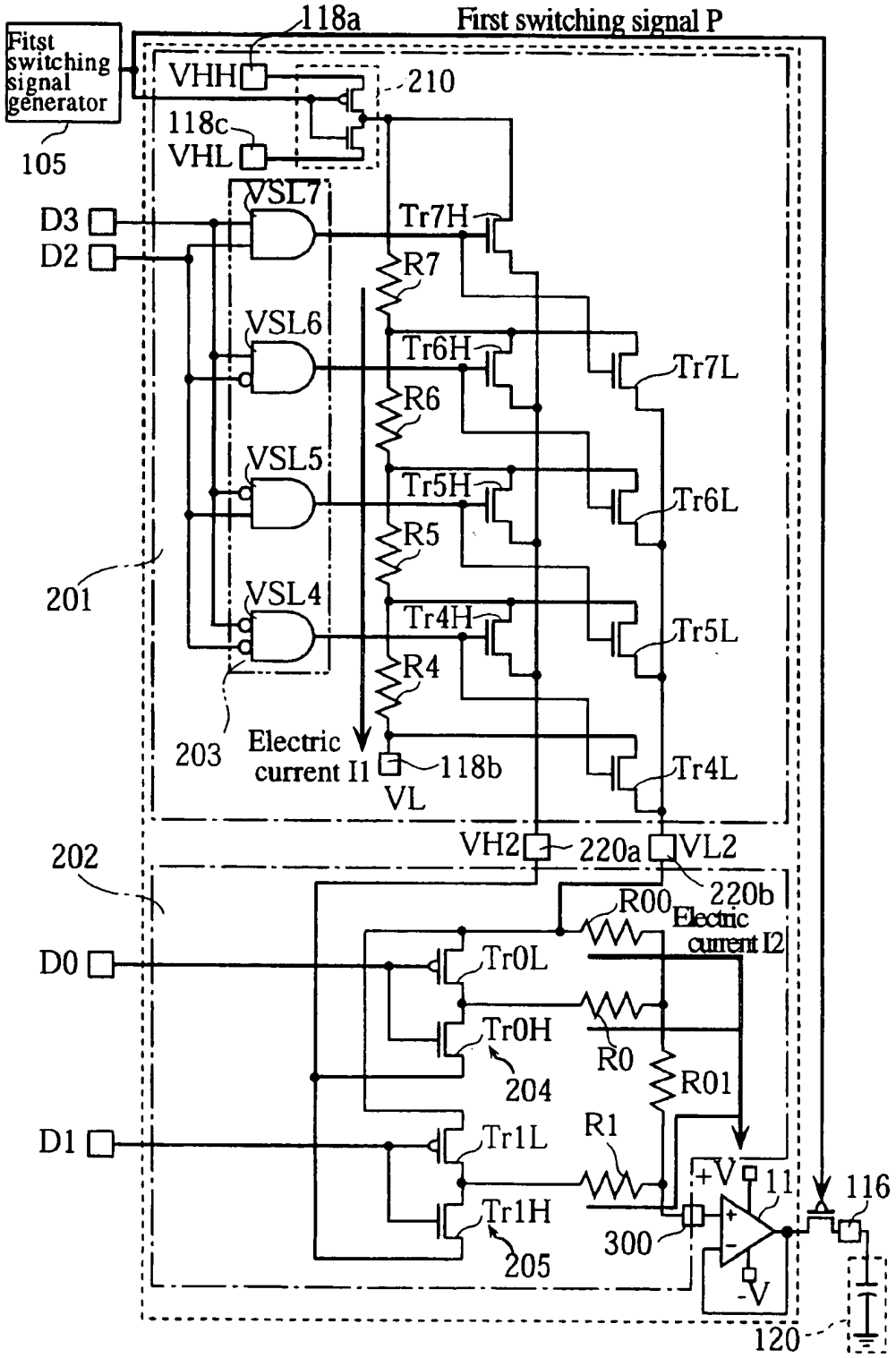

Fitst switching signal generator
105
118a
First switching signal P
VHH
210
118c
VHL
VSL7
Tr7H
D3
D2
R7
VSL6
Tr6H
Tr7L
R6
VSL5
Tr5H
Tr6L
R5
201
VSL4
Tr4H
Tr5L
R4
203
Electric current I1
118b
VL
Tr4L
202
VH2
220a
VL2
220b
R00
Electric current I2
D0
Tr0L
Tr0H
R0
204
R01
D1
Tr1L
R1
+V
11
116
Tr1H
300
205
-V
120

FIG. 33

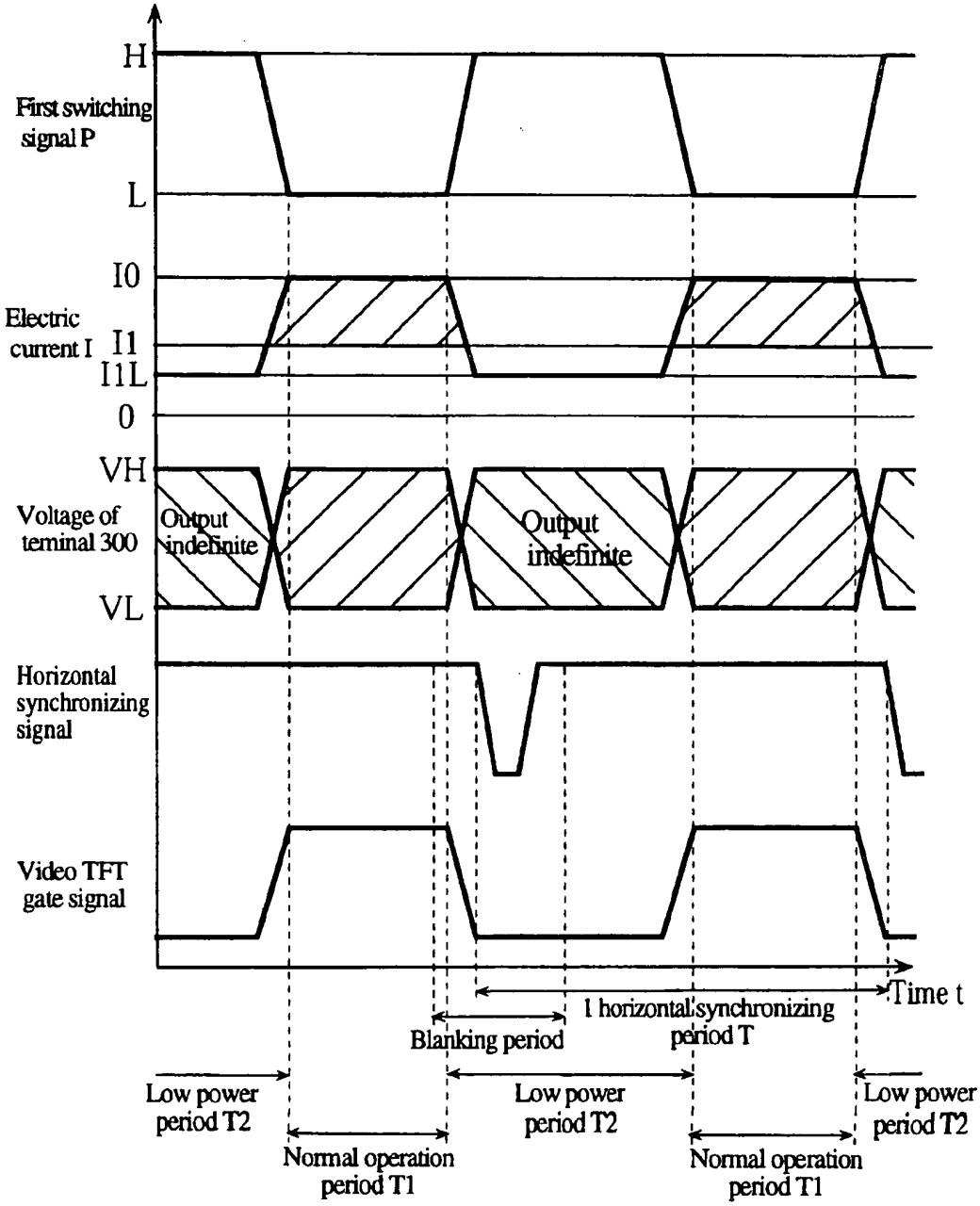

H
First switching signal P
L
I0
Electric current I
I1
I1L
0
VH
Voltage of terminal 300
Output indefinite
Output indefinite
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
1 horizontal synchronizing period T
Blanking period
Low power period T2
Low power period T2
Low power period T2
Normal operation period T1
Normal operation period T1

FIG. 34

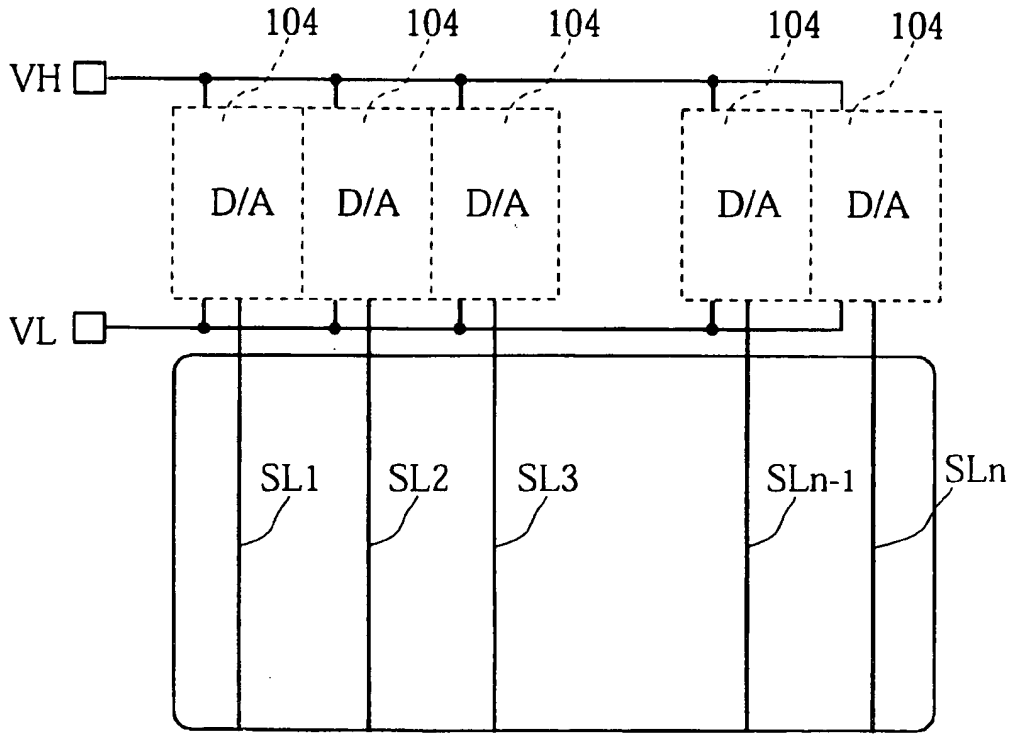


FIG. 35

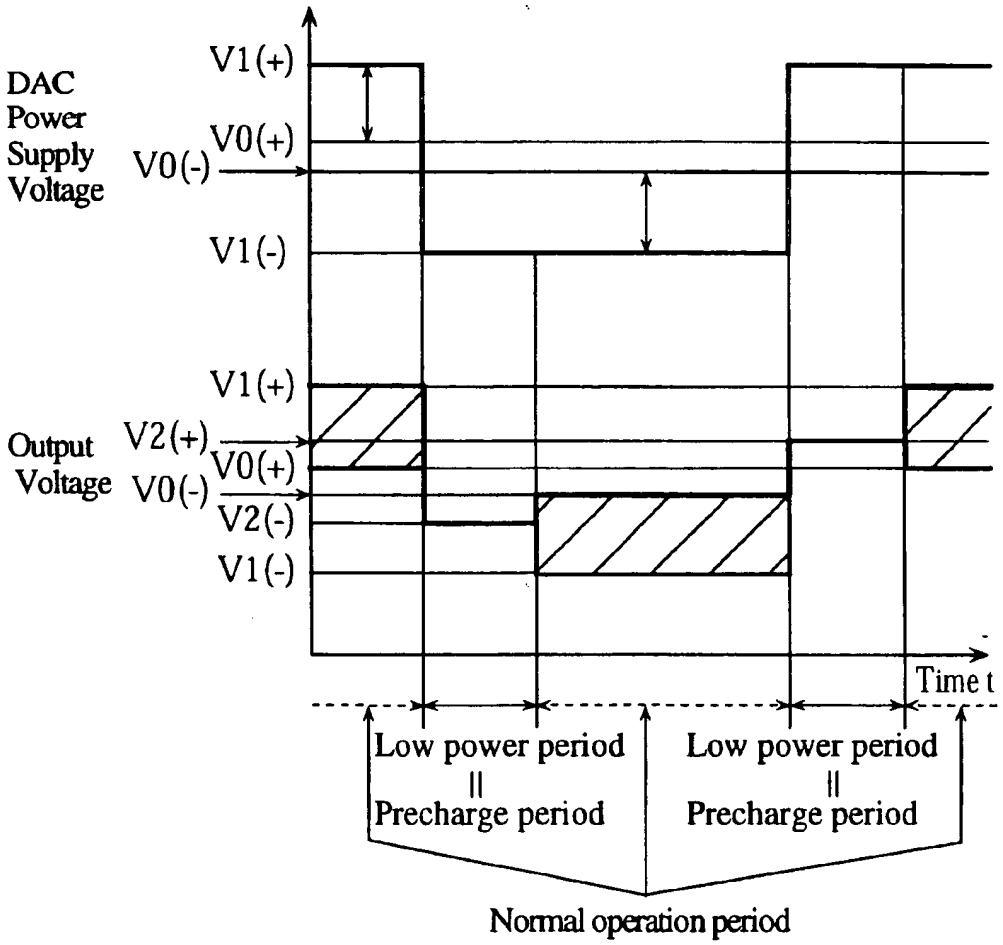

DAC
Power
Supply
Voltage
V1(+)
V0(+)
V0(-)
V1(-)
Output
Voltage
V1(+)
V2(+)
V0(+)
V0(-)
V2(-)
V1(-)
Time t
Low power period
||
Precharge period
Low power period
||
Precharge period
Normal operation period

FIG. 36

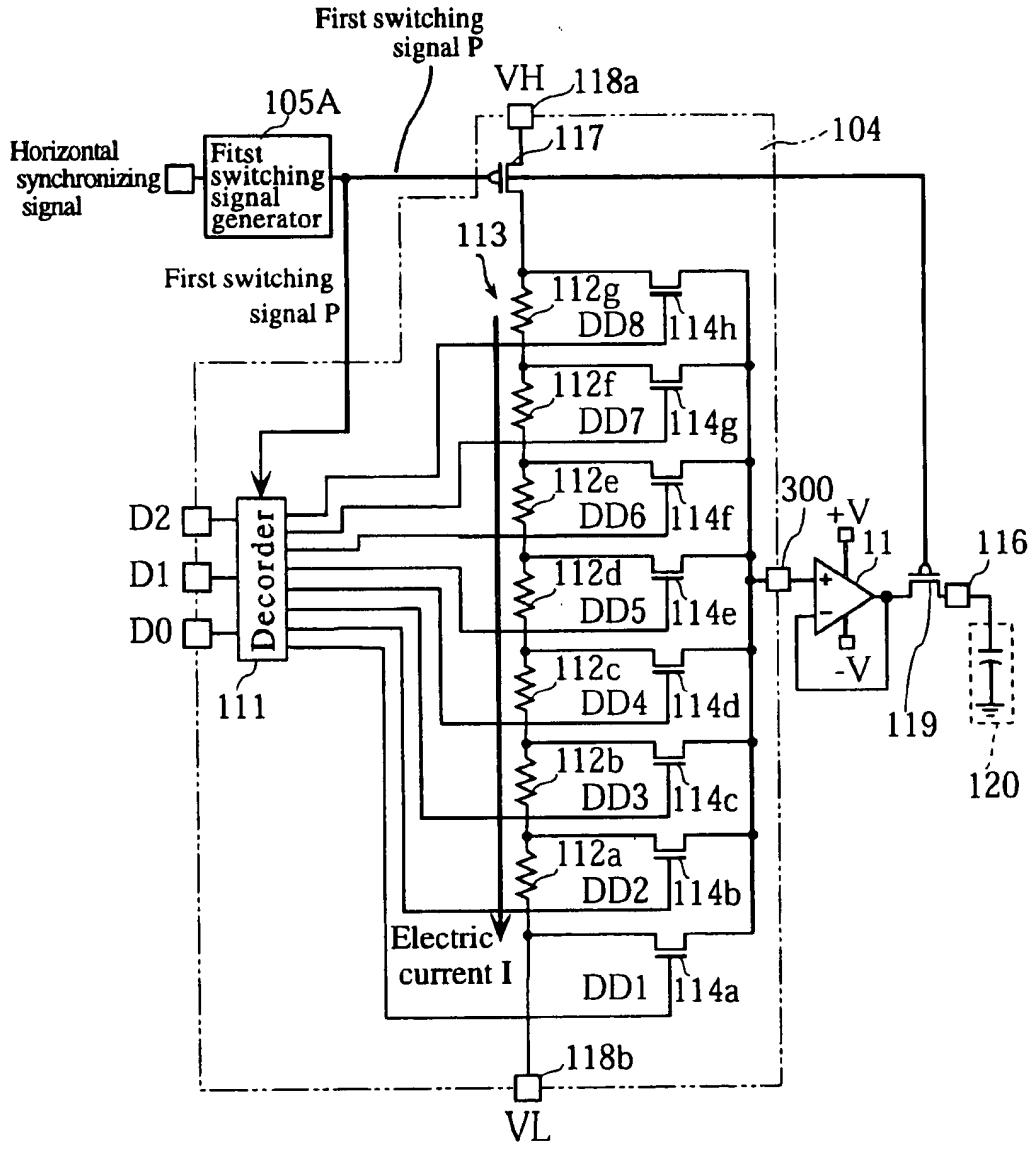

First switching signal P
VH
118a
105A
117
104
Horizontal synchronizing signal
Fitst switching signal generator
113
First switching signal P
112g
DD8
114h
112f
DD7
114g
112e
DD6
114f
300
+V
11
116
D2
D1
D0
Decorder
112d
DD5
114e
112c
DD4
114d
-V
119
111
112b
DD3
114c
120
112a
DD2
114b
Electric current I
DD1
114a
118b
VL

FIG. 37

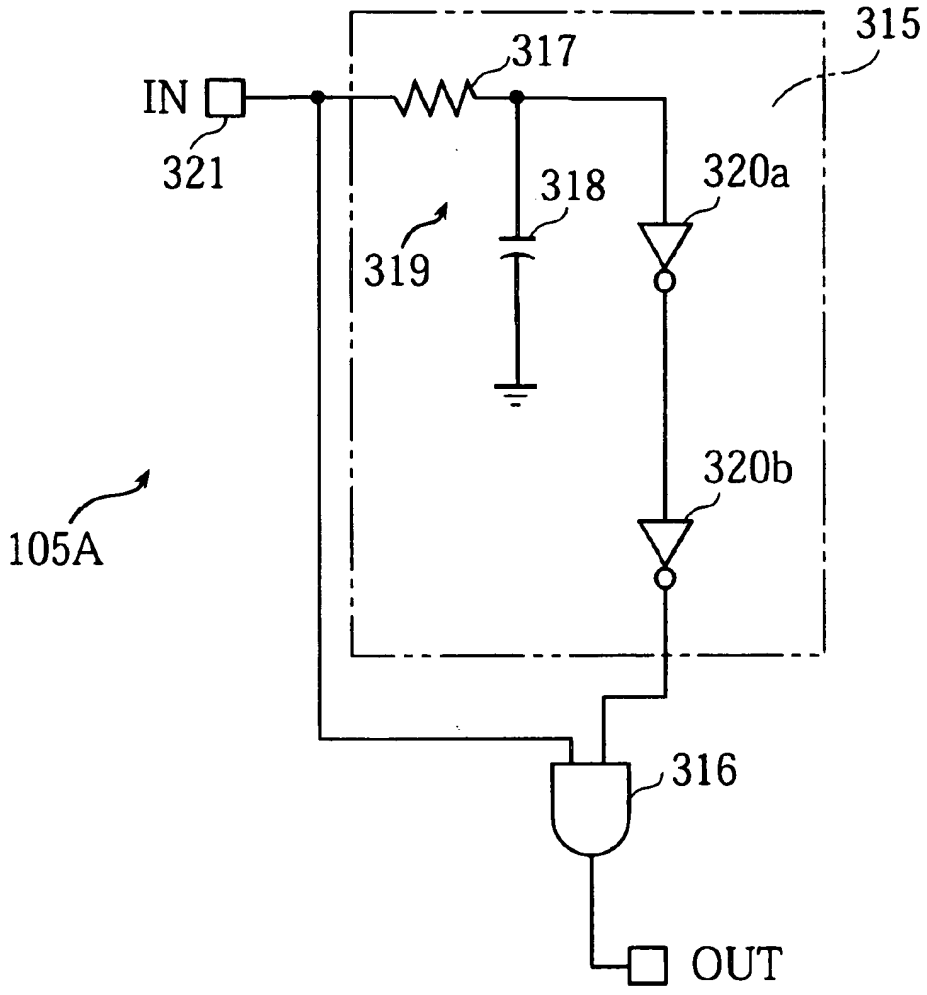


FIG. 38

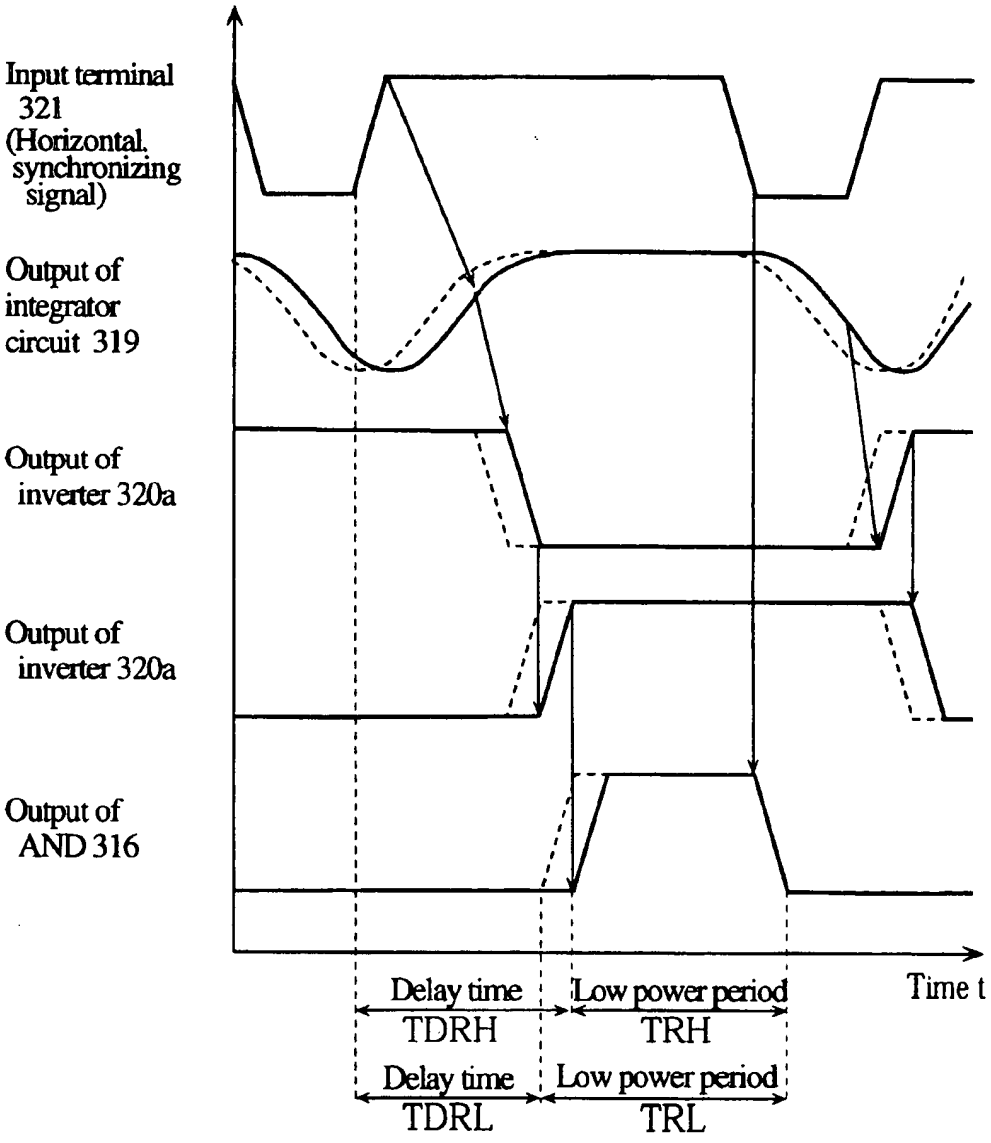

Input terminal 321 (Horizontal synchronizing signal)
Output of integrator circuit 319
Output of inverter 320a
Output of inverter 320a
Output of AND 316
Delay time TDRH
Low power period TRH
Delay time TDRL
Low power period TRL
Time t

FIG. 39

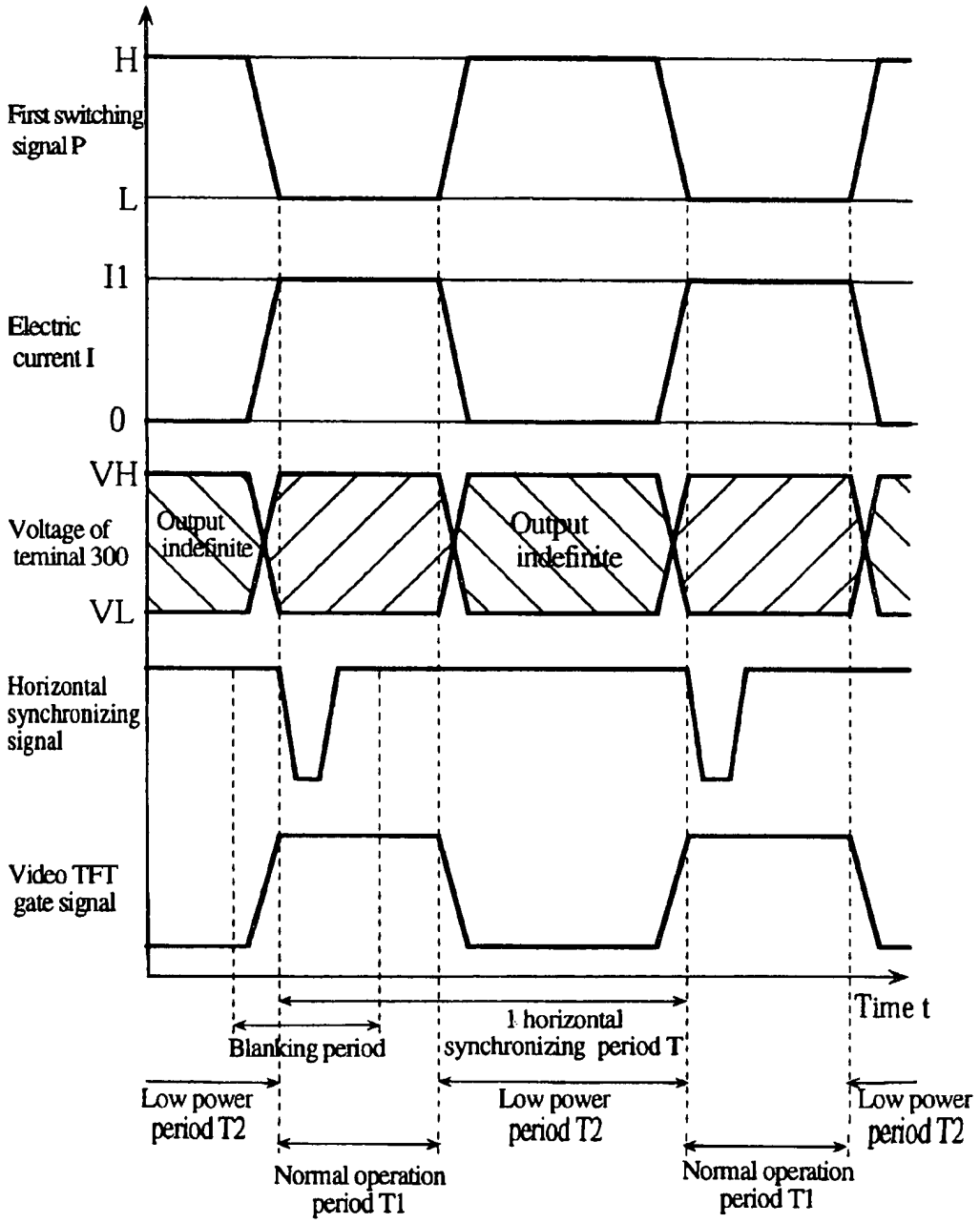

H
First switching signal P
L
I1
Electric current I
0
VH
Voltage of terminal 300
Output indefinite
Output indefinite
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
Blanking period
1 horizontal synchronizing period T
Low power period T2
Low power period T2
Low power period T2
Normal operation period T1
Normal operation period T1

FIG. 40

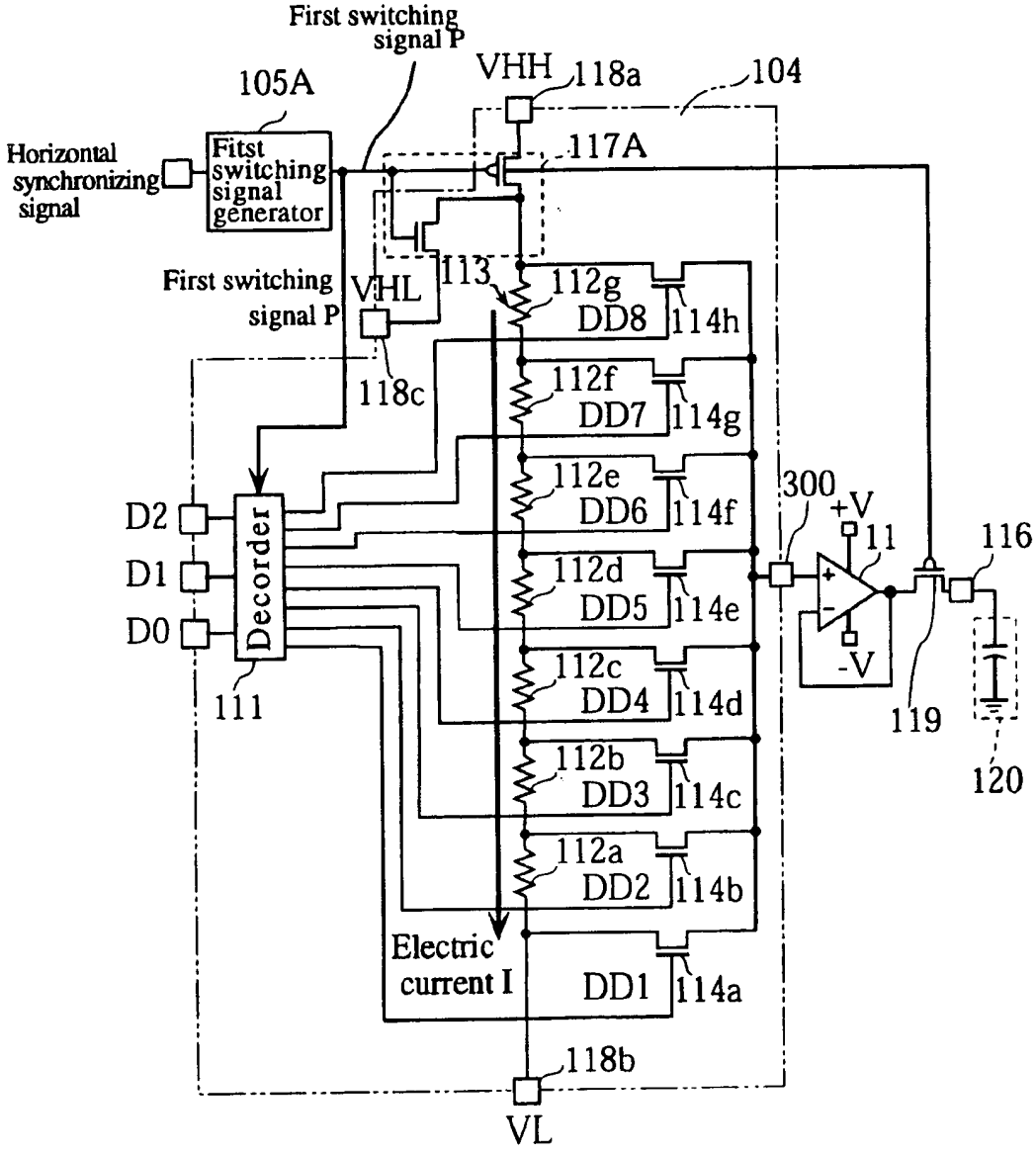
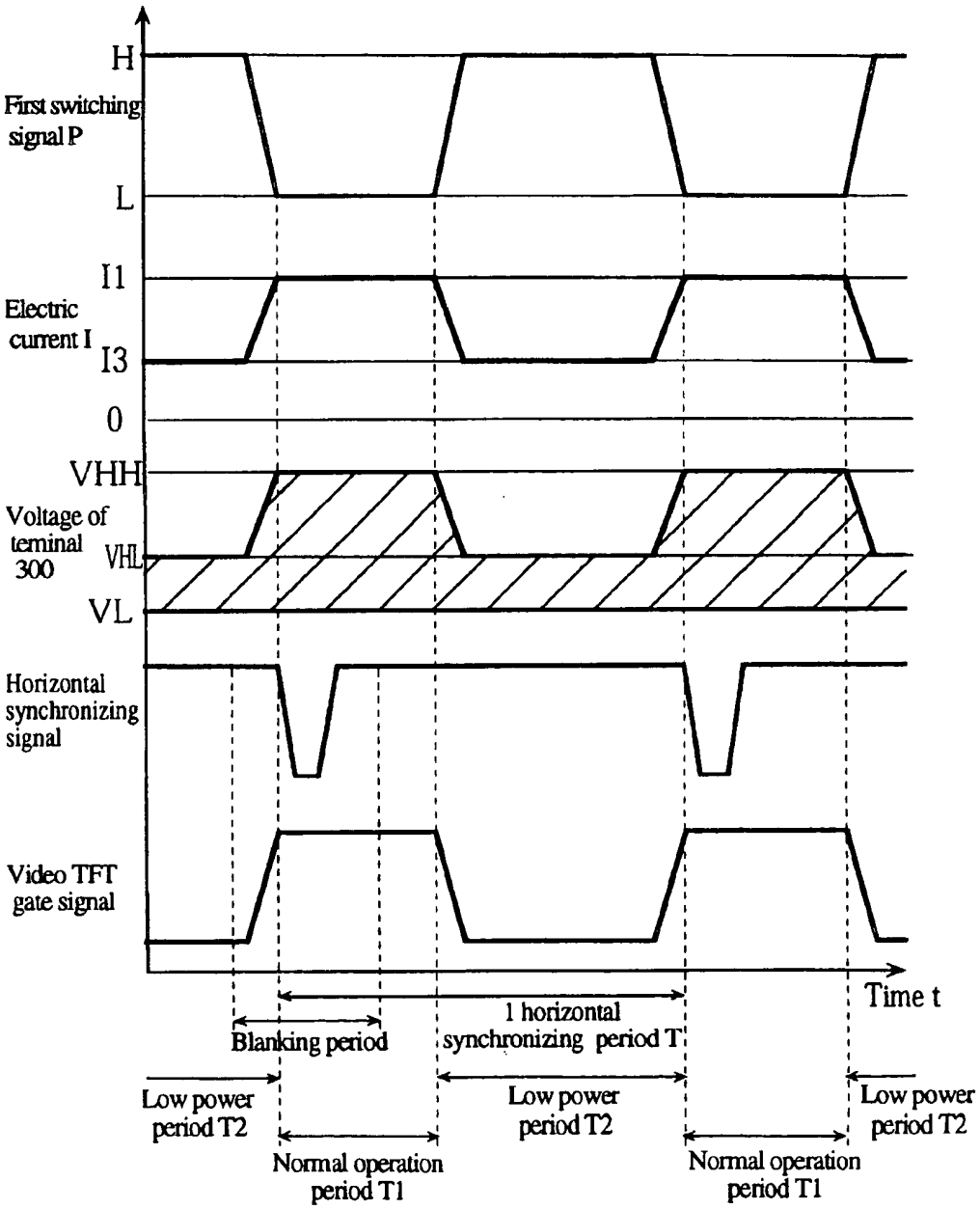

First switching signal P
105A
VHH
118a
104
Horizontal synchronizing signal
Fitst switching signal generator
117A
First switching signal P
VHL
113
112g
DD8
114h
118c
112f
DD7
114g
112e
DD6
114f
300
+V
11
116
D2
D1
D0
Decorder
112d
DD5
114e
112c
DD4
114d
-V
119
111
112b
DD3
114c
120
112a
DD2
114b
Electric current I
DD1
114a
118b
VL

FIG. 41


H
First switching signal P
L
I1
Electric current I
I3
0
VHH
Voltage of terminal 300
VHL
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
Blanking period
1 horizontal synchronizing period T
Low power period T2
Normal operation period T1
Low power period T2
Normal operation period T1
Low power period T2

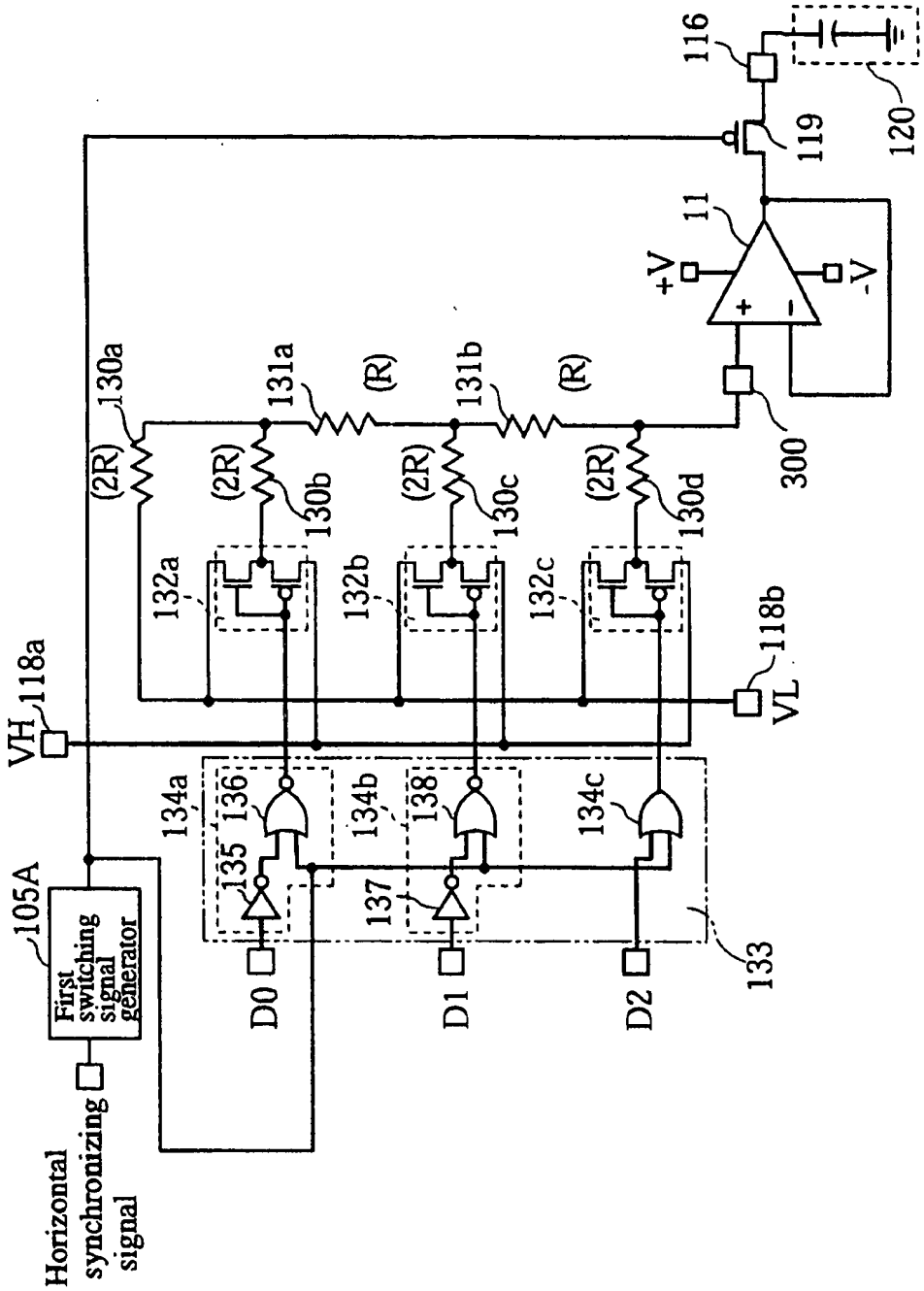
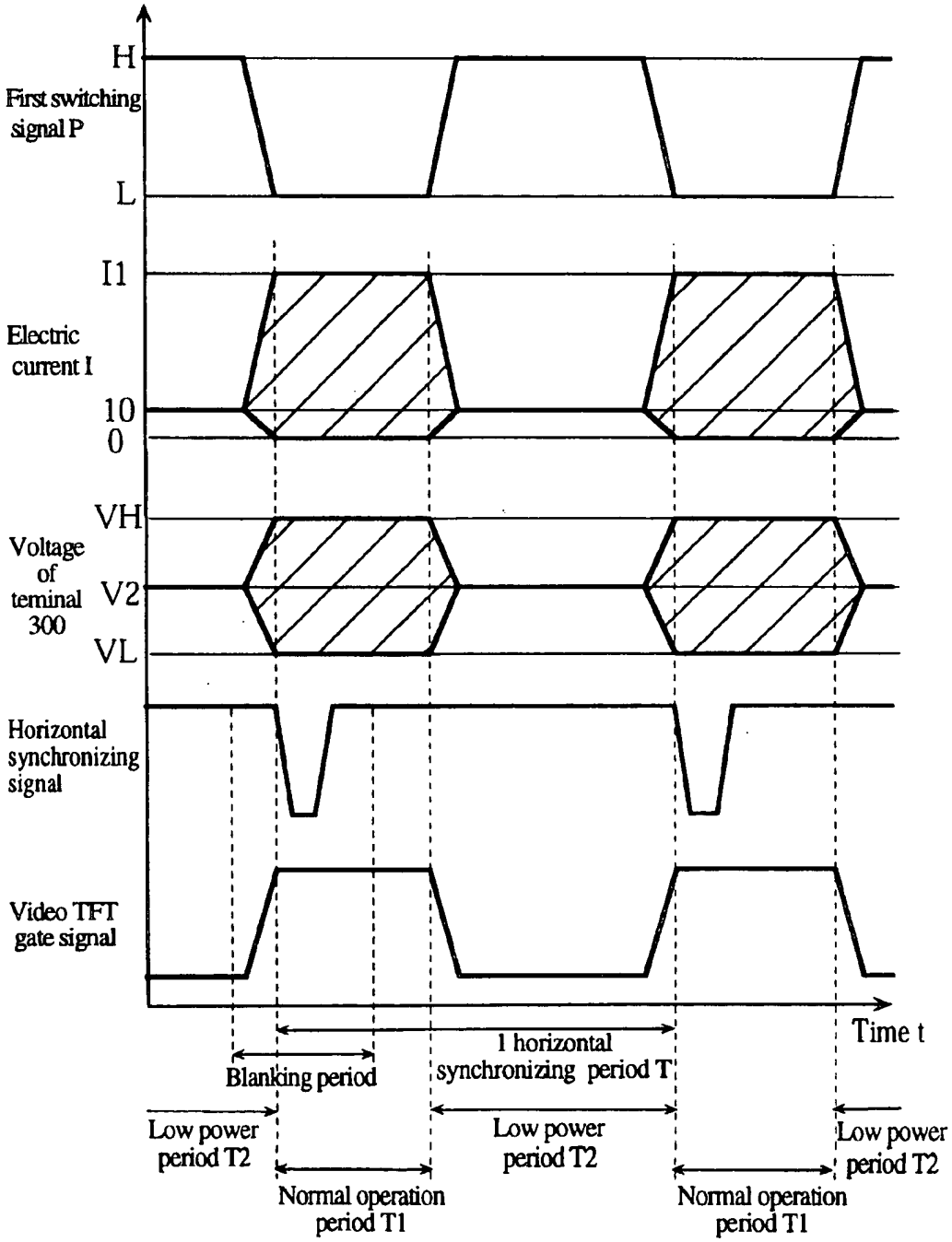

116
119
120
11
+V
-V
300
130a
131a
(R)
131b
(R)
(2R)
130b
130c
130d
132a
132b
132c
118a
VH
118b
VL
134a
134b
134c
136
138
135
137
133
105A
First switching signal generator
Horizontal synchronizing signal
D0
D1
D2

FIG. 42

FIG. 43


H
First switching signal P
L
I1
Electric current I
10
0
VH
Voltage of teminal 300
V2
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
Blanking period
1 horizontal synchronizing period T
Low power period T2
Normal operation period T1
Low power period T2
Normal operation period T1
Low power period T2

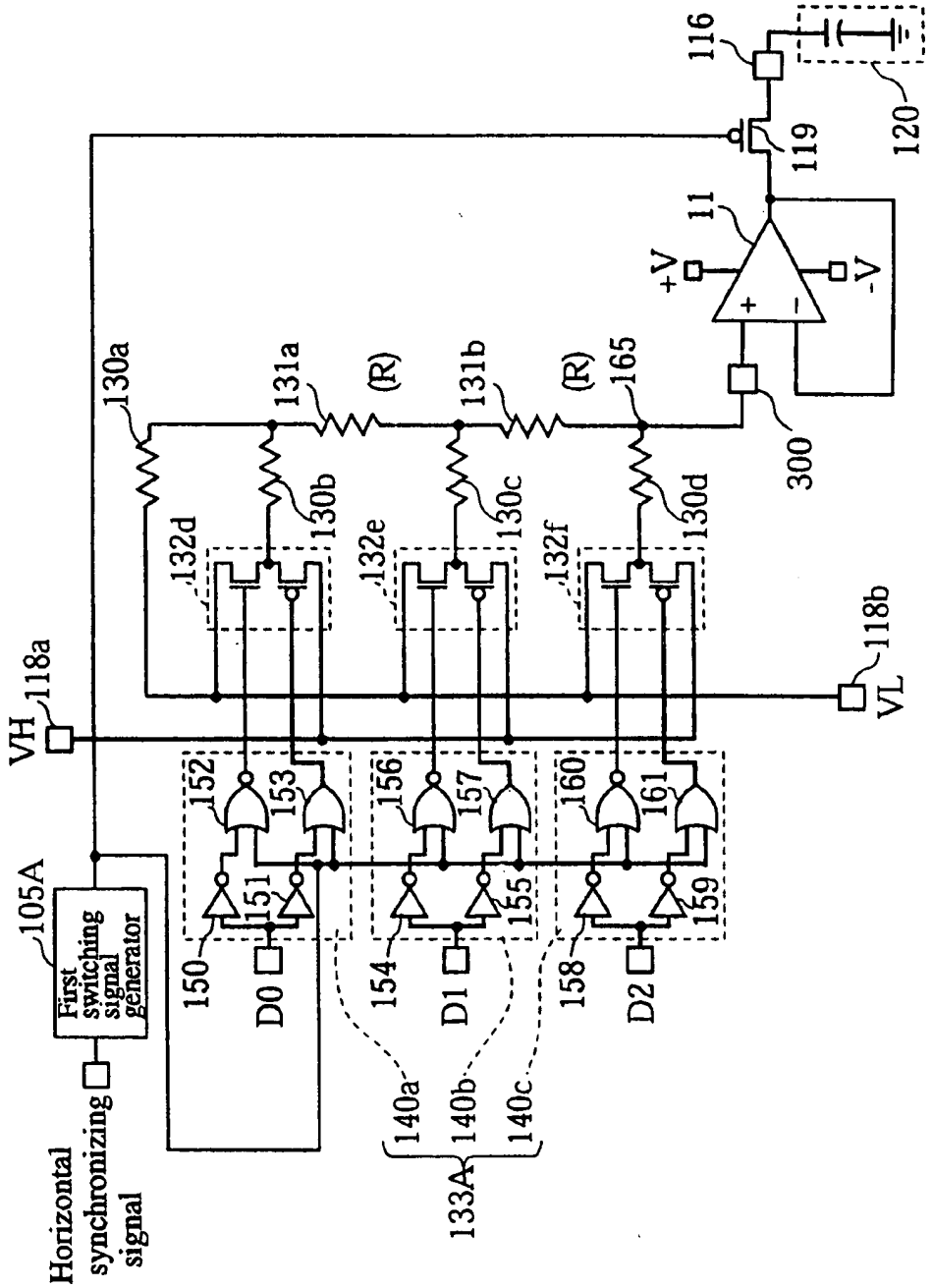

116
120
119
11
+V
-V
130a
131a
(R)
131b
(R)
165
300
130b
130c
130d
132d
132e
132f
118b
VL
118a
VH
152
153
156
157
160
161
105A
First switching signal generator
151
155
159
150
154
158
D0
D1
D2
140a
140b
140c
133A
Horizontal synchronizing signal

FIG. 44

FIG. 45

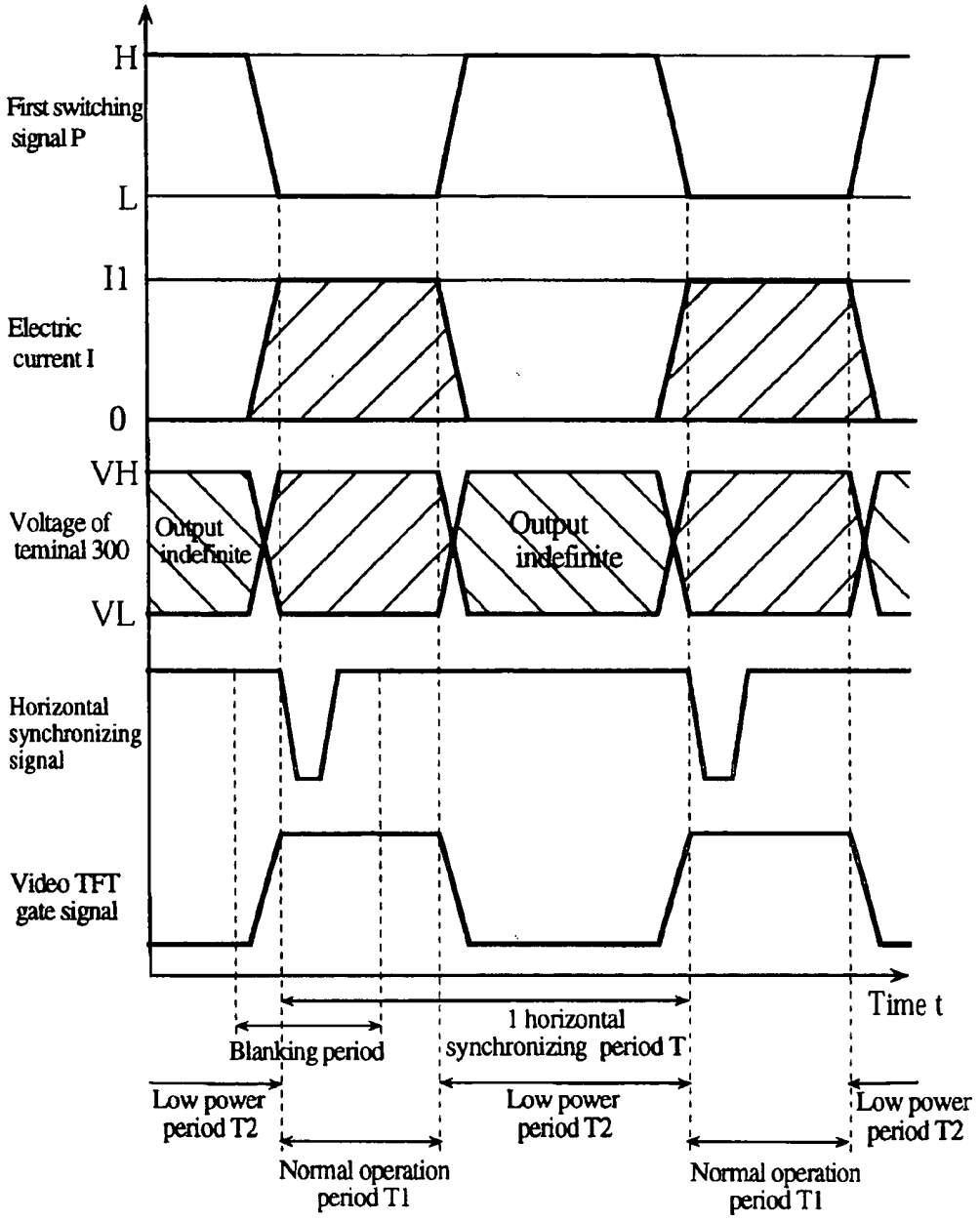

H
First switching signal P
L
I1
Electric current I
0
VH
Voltage of teminal 300
Output indefinite
Output indefinite
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
Blanking period
1 horizontal synchronizing period T
Low power period T2
Low power period T2
Low power period T2
Normal operation period T1
Normal operation period T1

FIG. 46

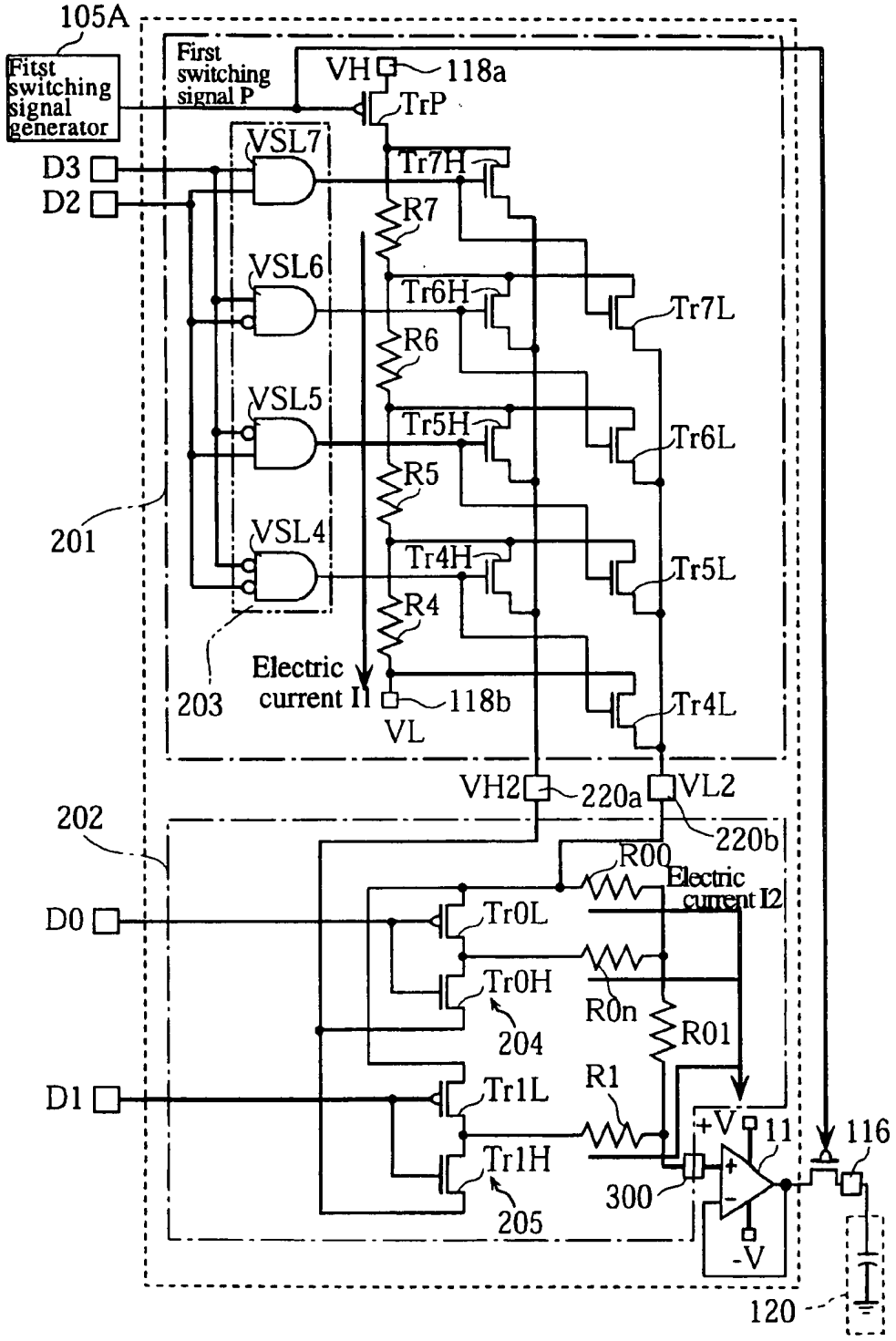

105A
Fitst switching signal generator
First switching signal P
VH
118a
TrP
VSL7
Tr7H
D3
D2
R7
VSL6
Tr6H
Tr7L
R6
VSL5
Tr5H
Tr6L
R5
201
VSL4
Tr4H
Tr5L
R4
Electric current I1
203
118b
VL
Tr4L
VH2
220a
VL2
220b
202
R00
Electric current I2
D0
Tr0L
Tr0H
R0n
R01
204
D1
Tr1L
R1
+V
11
116
Tr1H
300
205
-V
120

FIG. 47

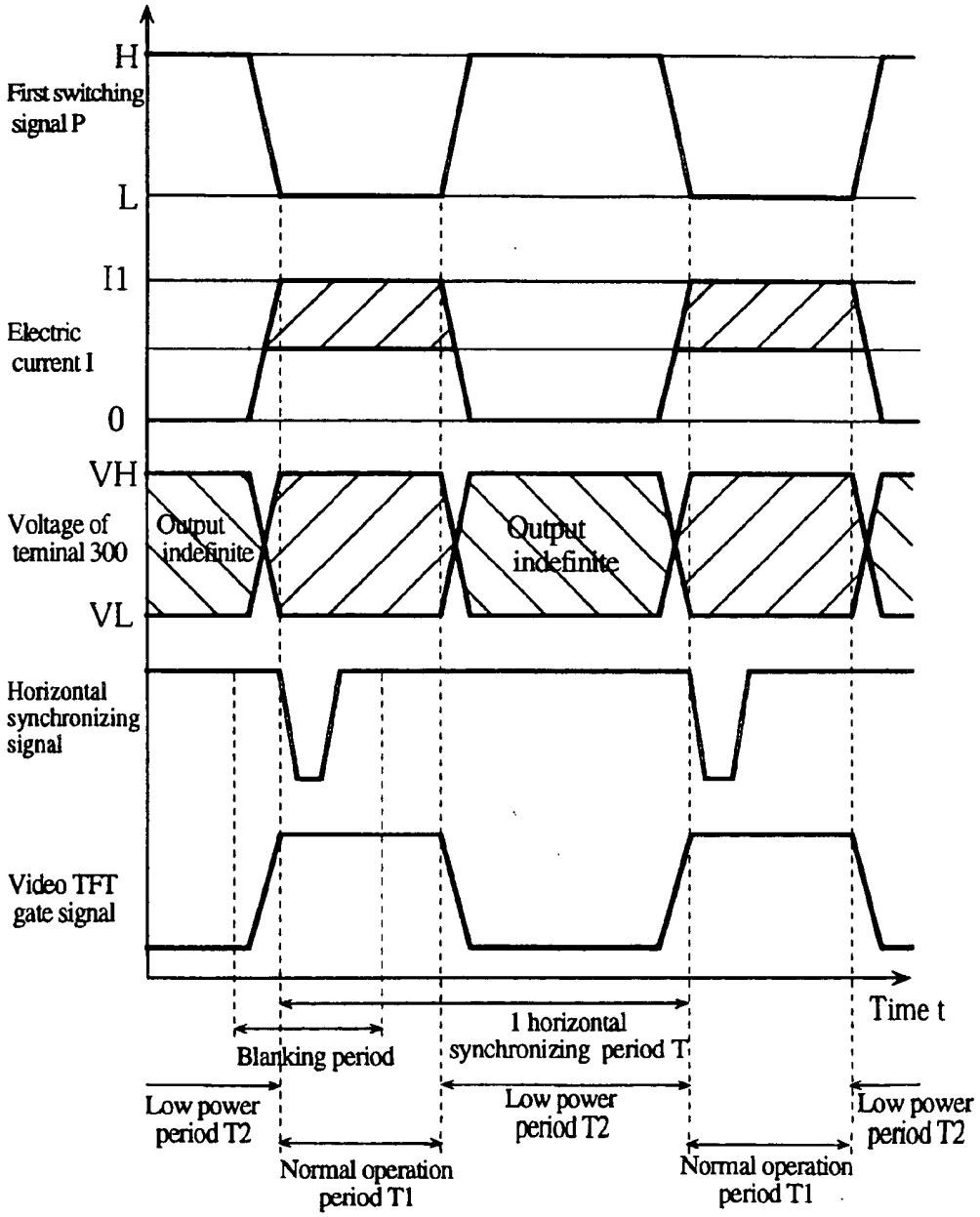

H
First switching signal P
L
I1
Electric current I
0
VH
Voltage of terminal 300
Output indefinite
Output indefinite
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
Blanking period
1 horizontal synchronizing period T
Low power period T2
Normal operation period T1
Low power period T2
Normal operation period T1
Low power period T2

FIG. 48

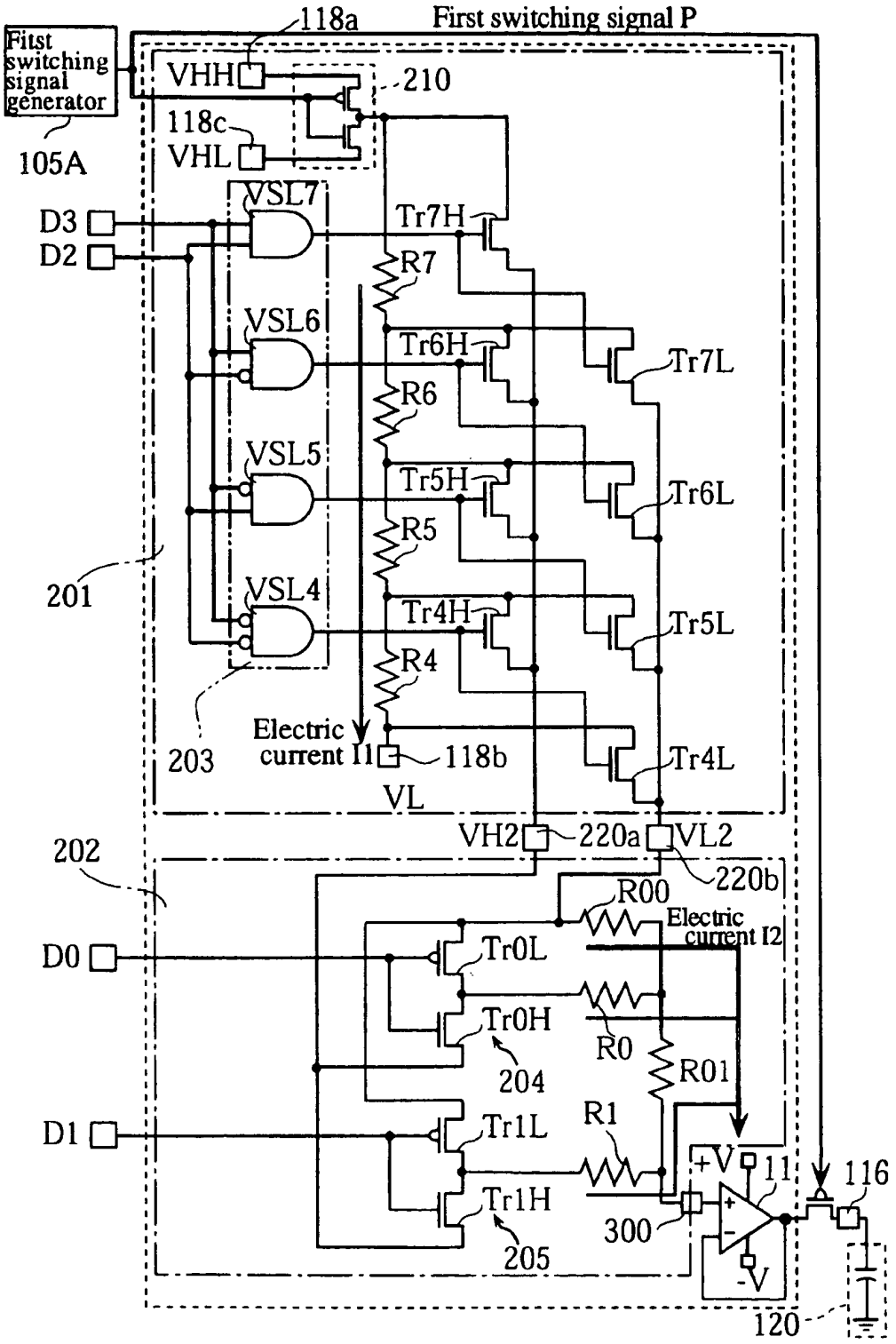

Fitst switching signal generator
105A
118a
First switching signal P
VHH
210
118c
VHL
VSL7
Tr7H
D3
D2
R7
VSL6
Tr6H
Tr7L
R6
VSL5
Tr5H
Tr6L
R5
201
VSL4
Tr4H
Tr5L
R4
203
Electric current I1
118b
Tr4L
VL
VH2
220a
VL2
202
220b
R00
Electric current I2
D0
Tr0L
Tr0H
R0
204
R01
D1
Tr1L
R1
+V
11
116
Tr1H
300
205
-V
120

FIG. 49

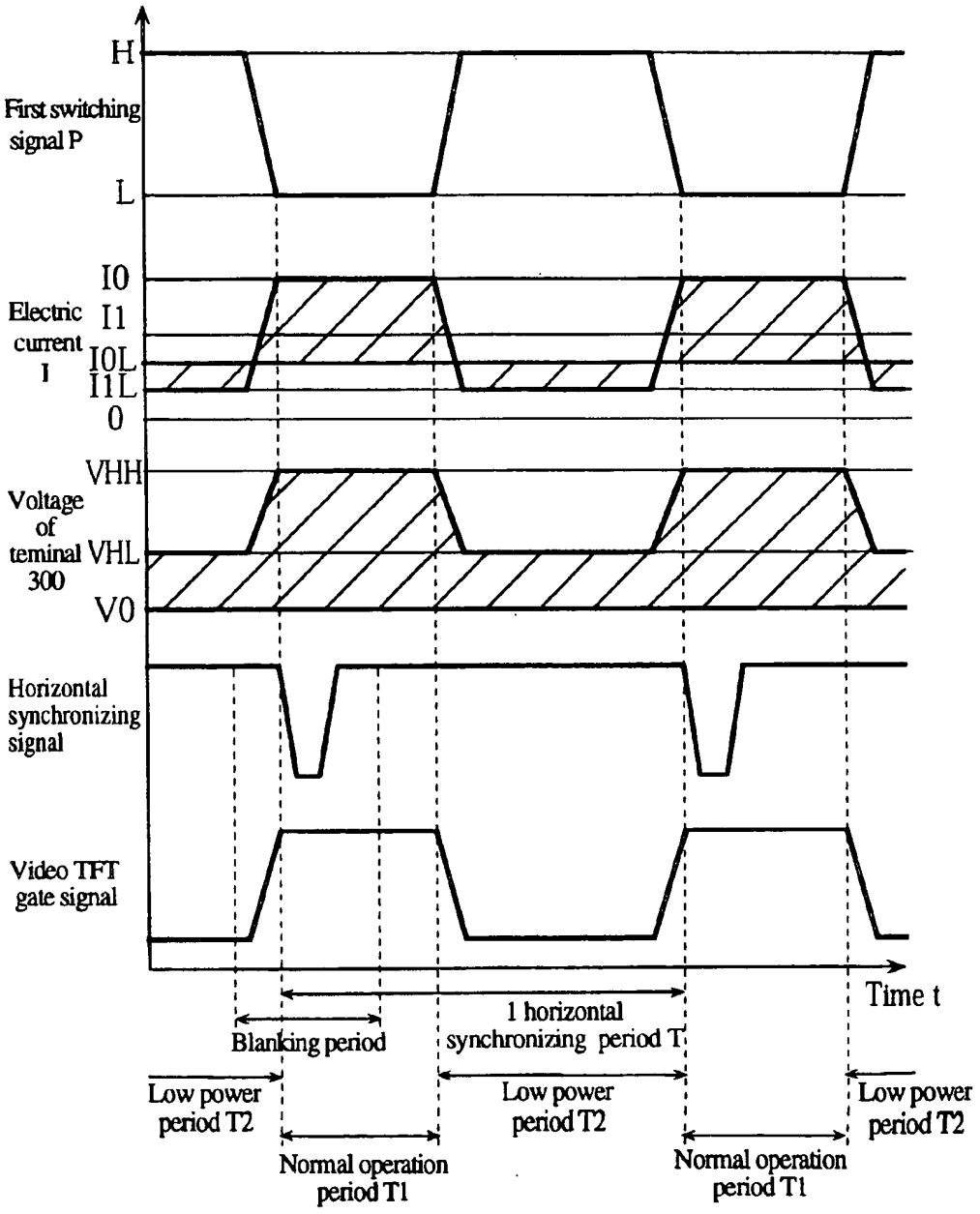

H
First switching signal P
L
I0
Electric current I
I1
I0L
I1L
0
VHH
Voltage of teminal 300
VHL
V0
Horizontal synchronizing signal
Video TFT gate signal
Time t
Blanking period
1 horizontal synchronizing period T
Low power period T2
Normal operation period T1
Low power period T2
Normal operation period T1
Low power period T2

FIG. 50

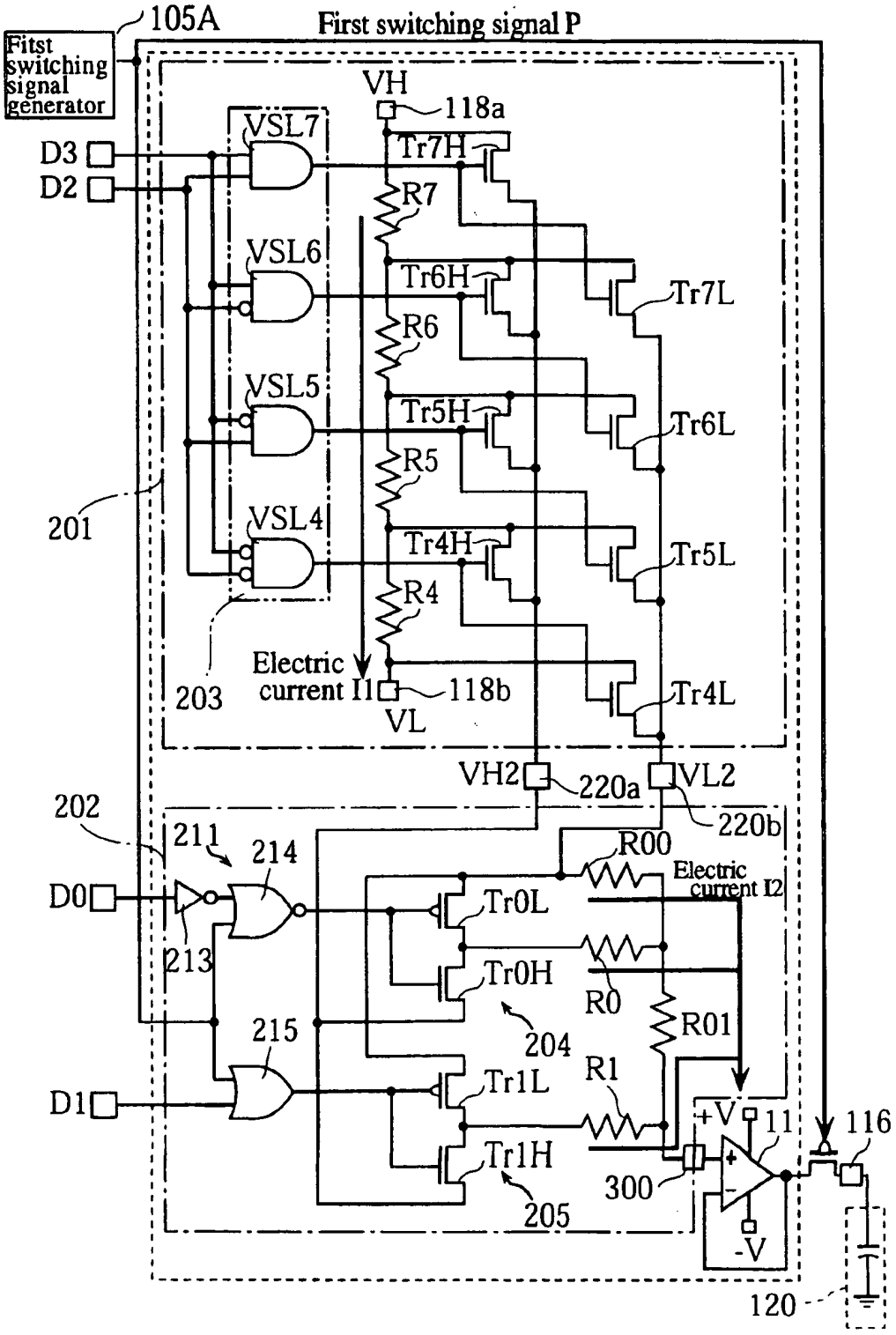

105A
First switching signal P
Fitst switching signal generator
VH
118a
VSL7
Tr7H
D3
D2
R7
VSL6
Tr6H
Tr7L
R6
VSL5
Tr5H
Tr6L
R5
201
VSL4
Tr4H
Tr5L
R4
Electric current I1
203
118b
Tr4L
VL
VH2
220a
VL2
220b
202
211
214
R00
Electric current I2
D0
Tr0L
213
Tr0H
R0
R01
204
215
D1
Tr1L
R1
+V
11
116
Tr1H
300
205
-V
120

FIG. 51

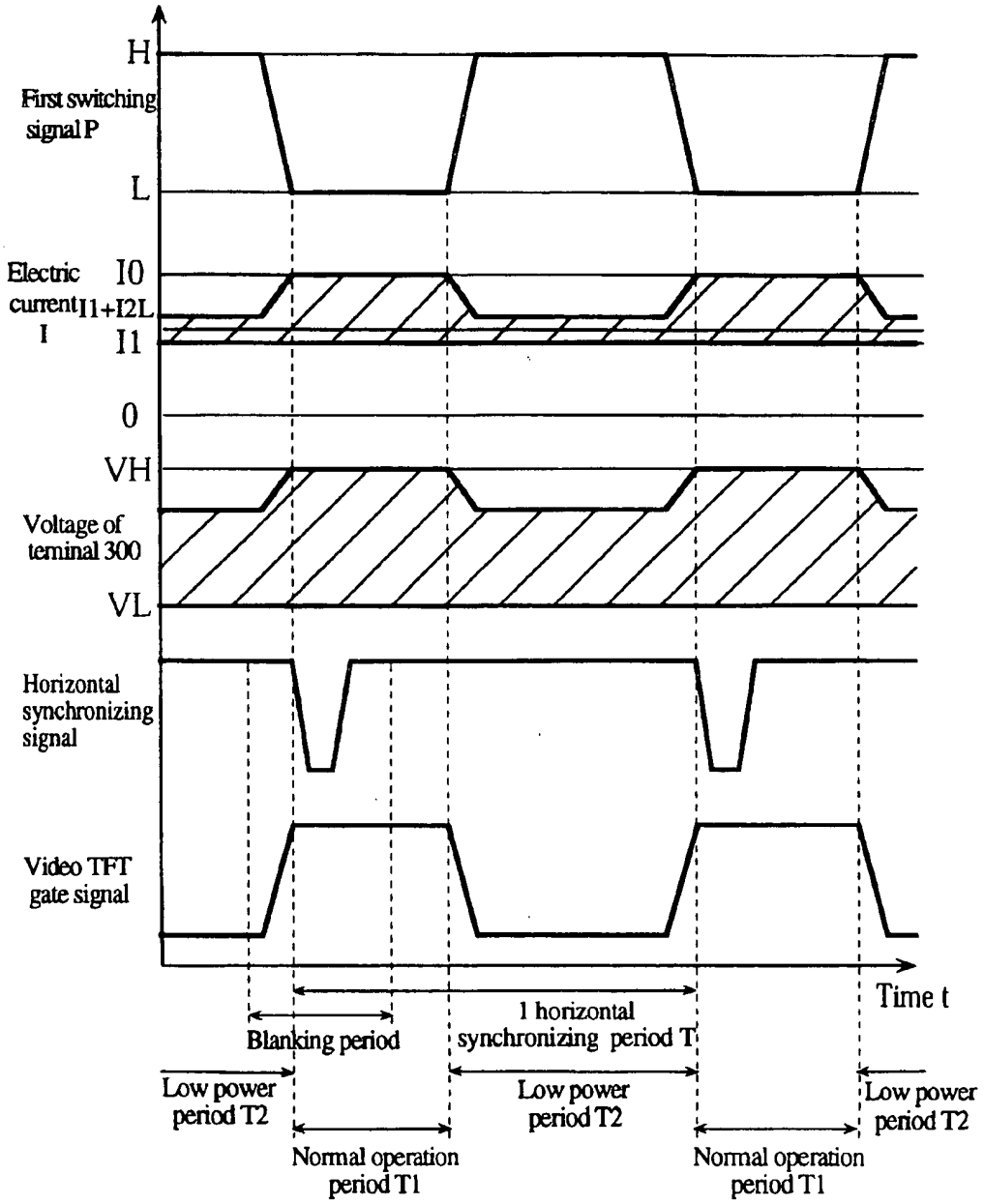

H
First switching signal P
L
Electric current I
I0
I1+I2L
I1
0
VH
Voltage of terminal 300
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
Blanking period
1 horizontal synchronizing period T
Low power period T2
Normal operation period T1
Low power period T2
Normal operation period T1
Low power period T2

FIG. 52

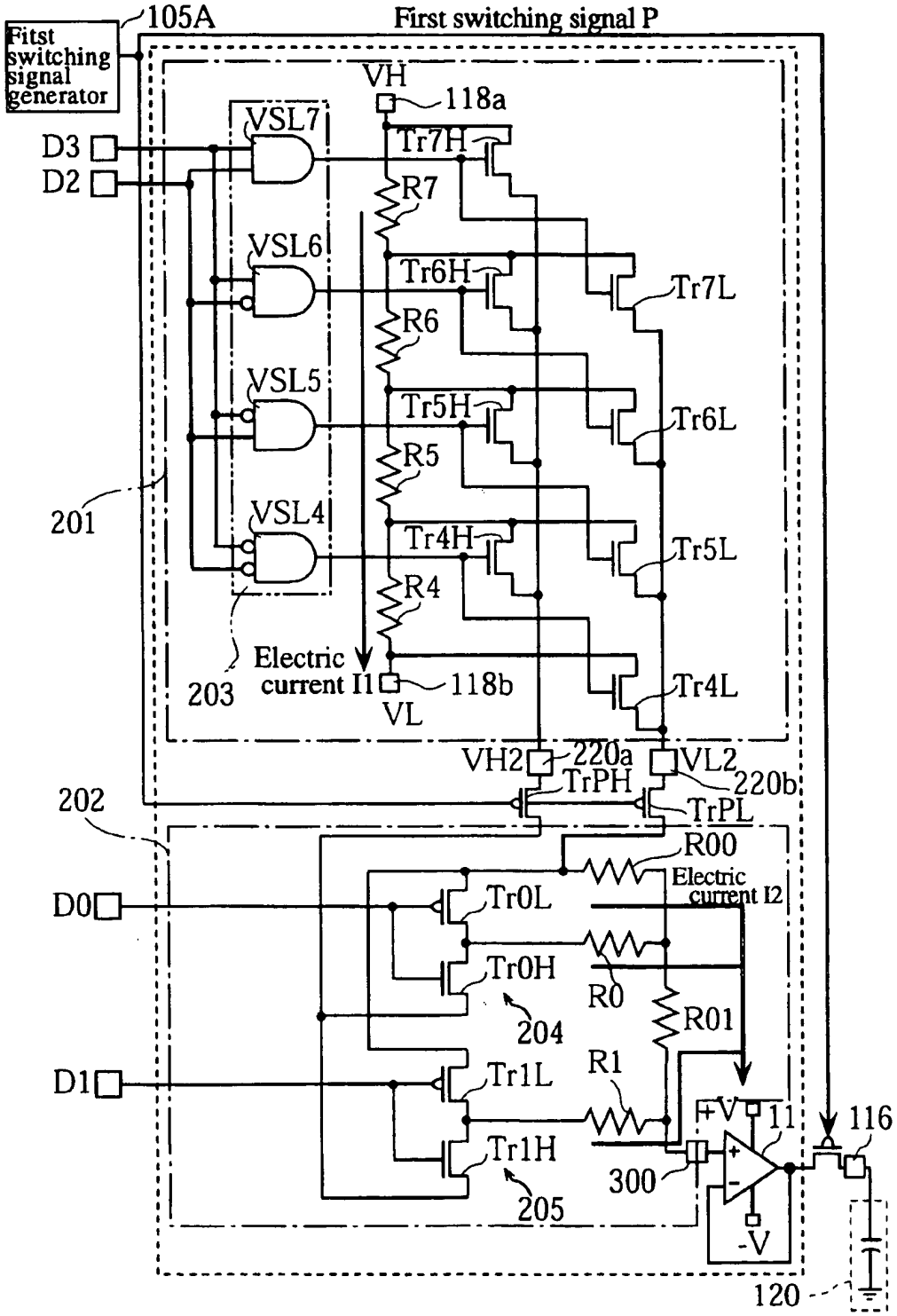

105A
First switching signal P
Fitst switching signal generator
VH
118a
VSL7
Tr7H
D3
D2
R7
VSL6
Tr6H
Tr7L
R6
VSL5
Tr5H
Tr6L
R5
201
VSL4
Tr4H
Tr5L
R4
Electric current I1
203
118b
VL
Tr4L
VH2
220a
VL2
220b
TrPH
TrPL
202
R00
Electric current I2
D0
Tr0L
Tr0H
R0
R01
204
D1
Tr1L
R1
+V
11
116
Tr1H
300
205
-V
120

FIG. 53

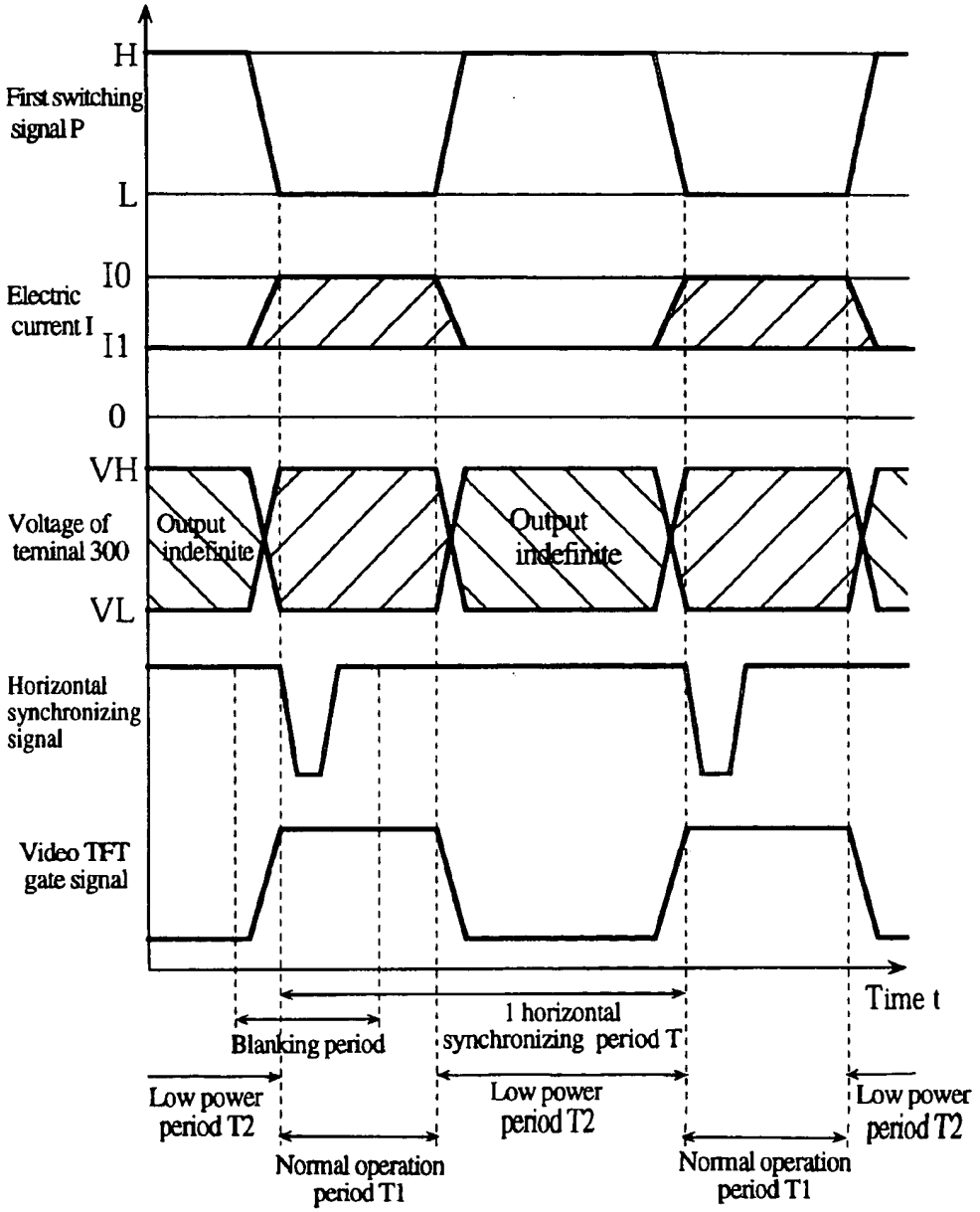

H
First switching signal P
L
I0
Electric current I
I1
0
VH
Voltage of teminal 300
Output indefinite
Output indefinite
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
Blanking period
1 horizontal synchronizing period T
Low power period T2
Normal operation period T1
Low power period T2
Normal operation period T1
Low power period T2

FIG. 54

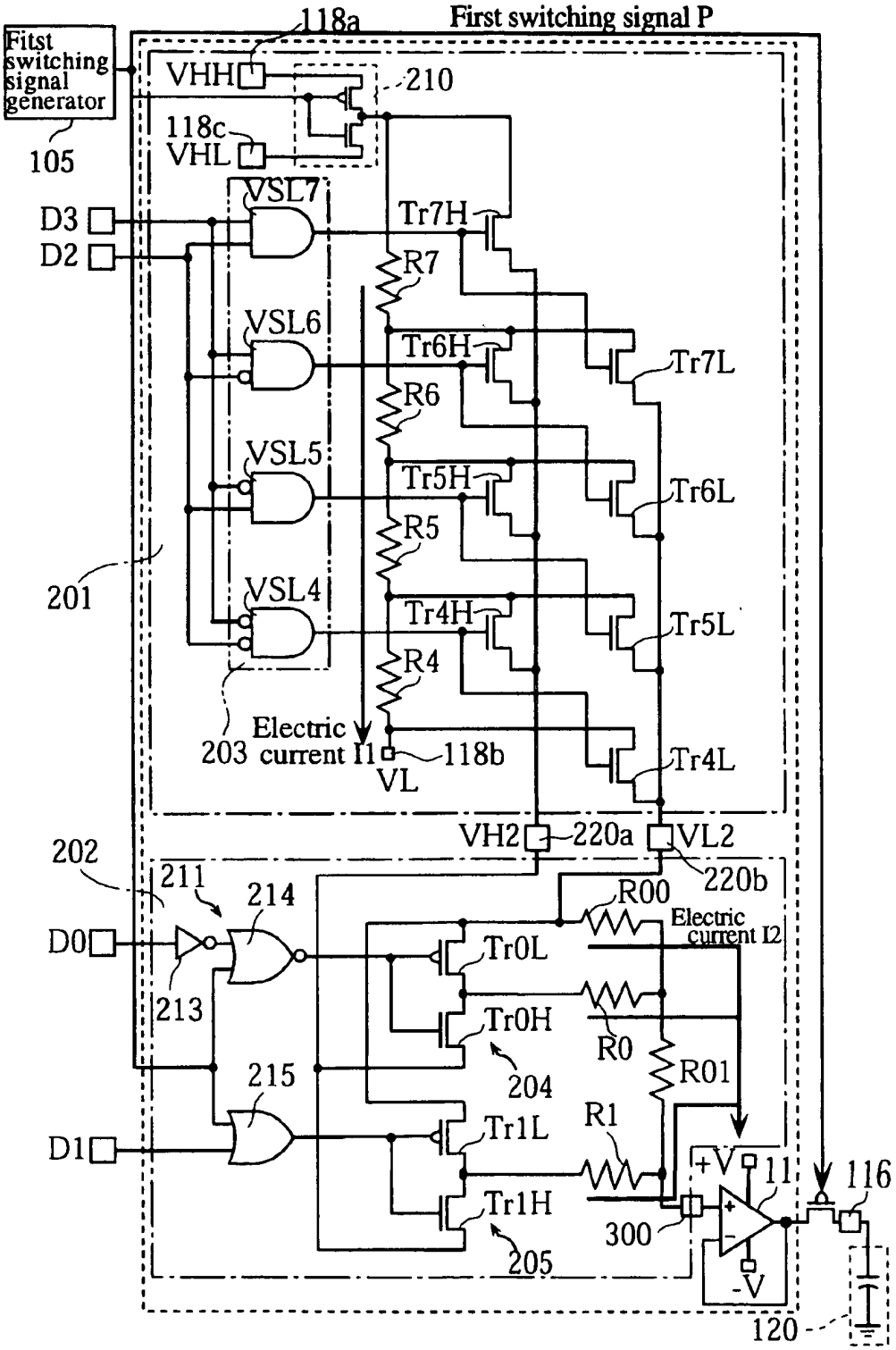

Fitst switching signal generator
105
118a
First switching signal P
VHH
210
118c
VHL
VSL7
Tr7H
D3
D2
R7
VSL6
Tr6H
Tr7L
R6
VSL5
Tr5H
Tr6L
R5
201
VSL4
Tr4H
Tr5L
R4
Electric
203 current I1
118b
VL
Tr4L
VH2
220a
VL2
220b
202
211
214
R00
Electric current I2
D0
213
Tr0L
Tr0H
R0
R01
204
215
R1
Tr1L
D1
+V
11
116
Tr1H
300
205
-V
120

FIG. 55

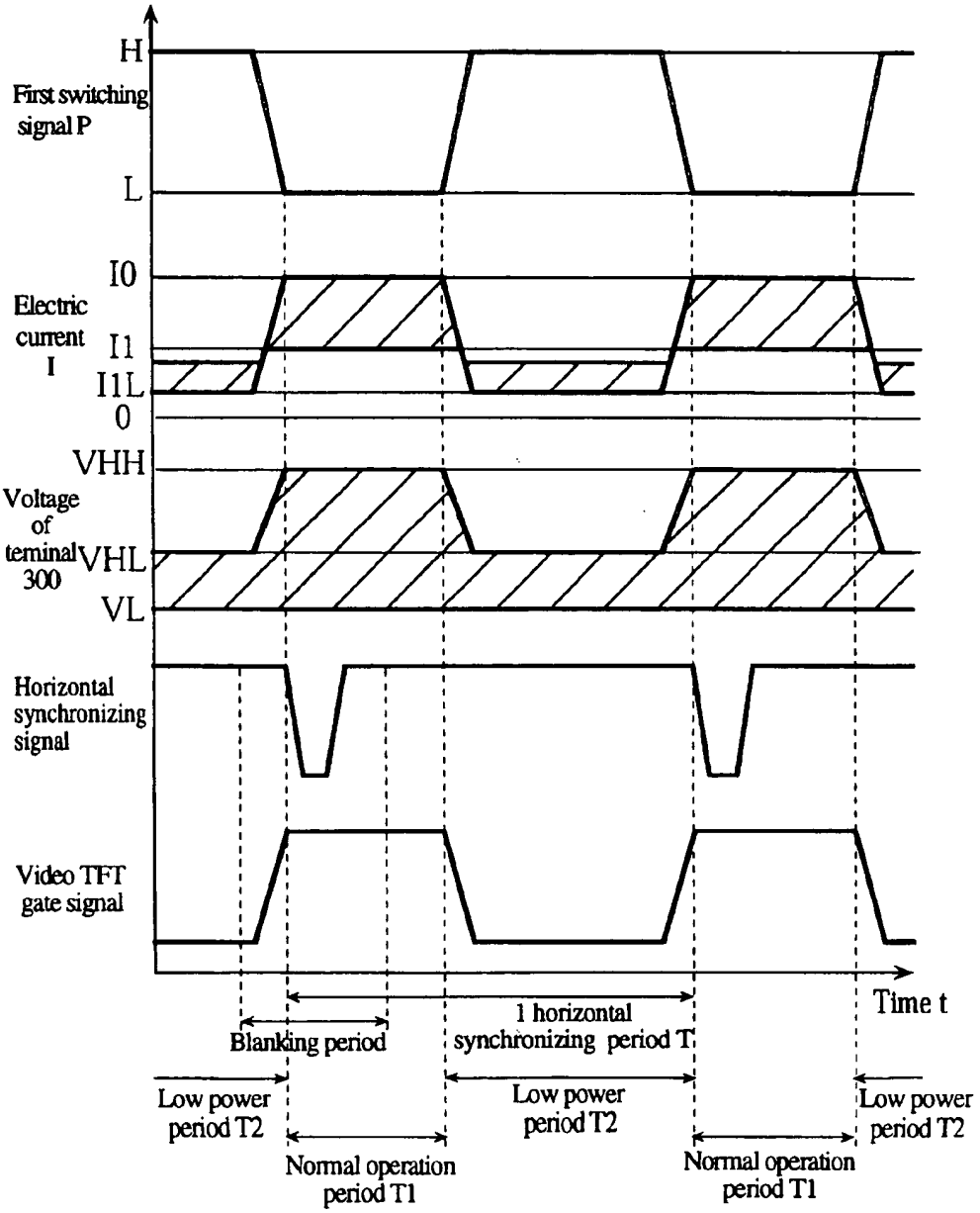

H
First switching signal P
L
I0
Electric current I
I1
I1L
0
VHH
Voltage of teminal 300
VHL
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
Blanking period
1 horizontal synchronizing period T
Low power period T2
Normal operation period T1
Low power period T2
Normal operation period T1
Low power period T2

FIG. 56

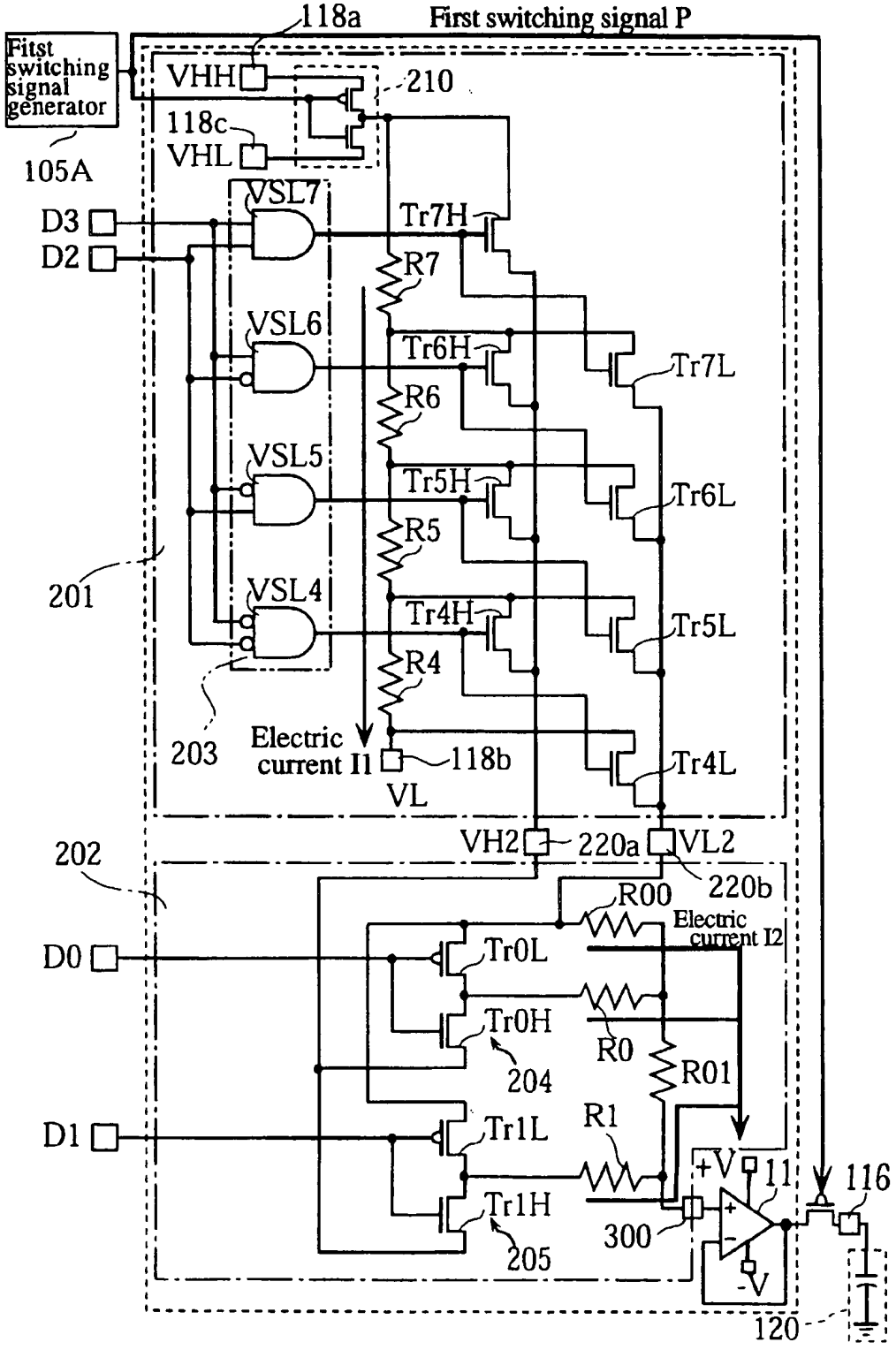

118a
First switching signal P
Fitst switching signal generator
105A
VHH
210
118c
VHL
VSL7
Tr7H
D3
D2
R7
VSL6
Tr6H
Tr7L
R6
VSL5
Tr5H
Tr6L
R5
201
VSL4
Tr4H
Tr5L
R4
203
Electric current I1
118b
VL
Tr4L
VH2
220a
VL2
202
220b
R00
Electric current I2
D0
Tr0L
Tr0H
R0
204
R01
D1
Tr1L
R1
+V
11
116
Tr1H
300
205
-V
120

FIG. 57

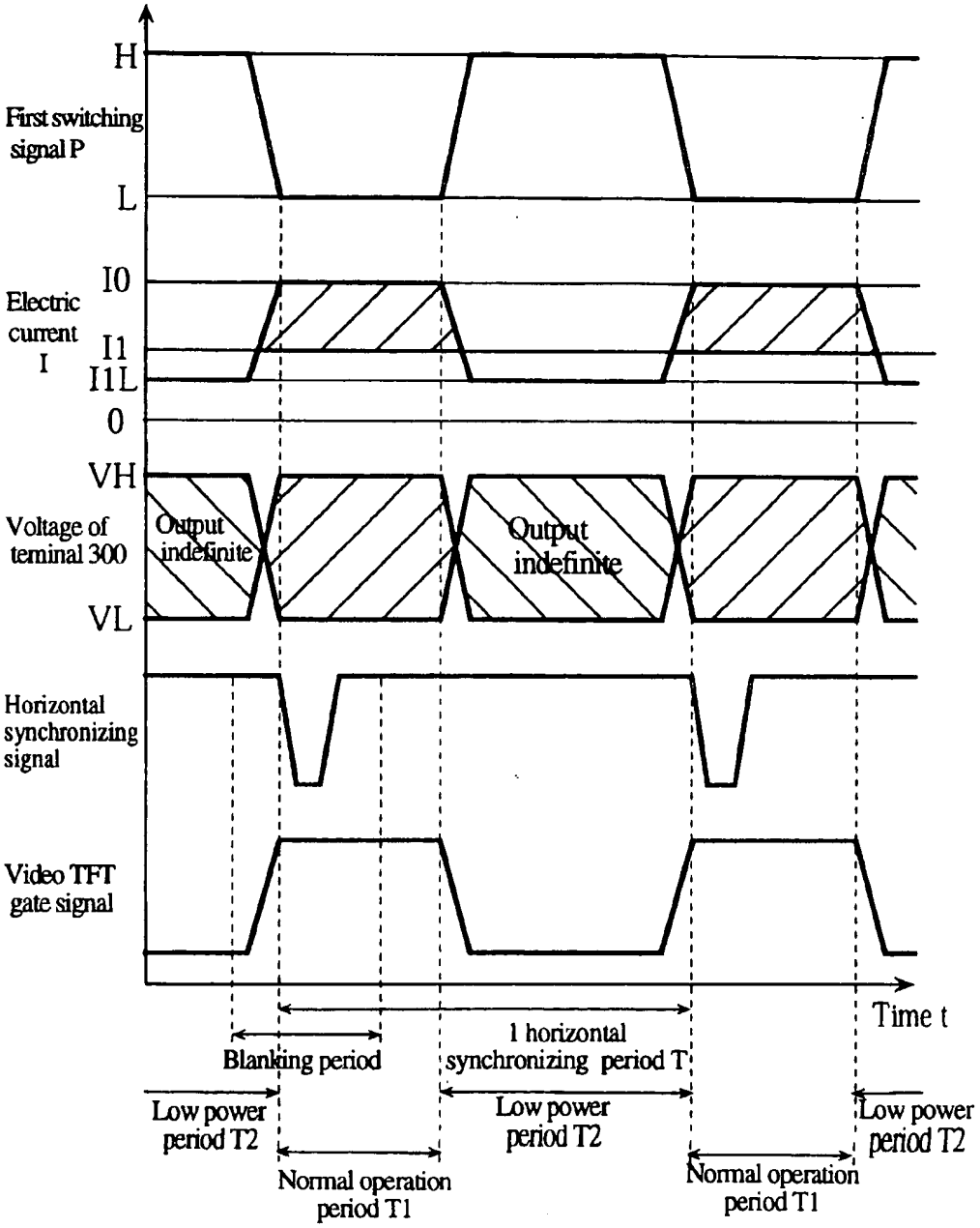

H
First switching signal P
L
I0
Electric current I
I1
I1L
0
VH
Voltage of terminal 300
Output indefinite
Output indefinite
VL
Horizontal synchronizing signal
Video TFT gate signal
Time t
Blanking period
1 horizontal synchronizing period T
Low power period T2
Low power period T2
Low power period T2
Normal operation period T1
Normal operation period T1

FIG. 58

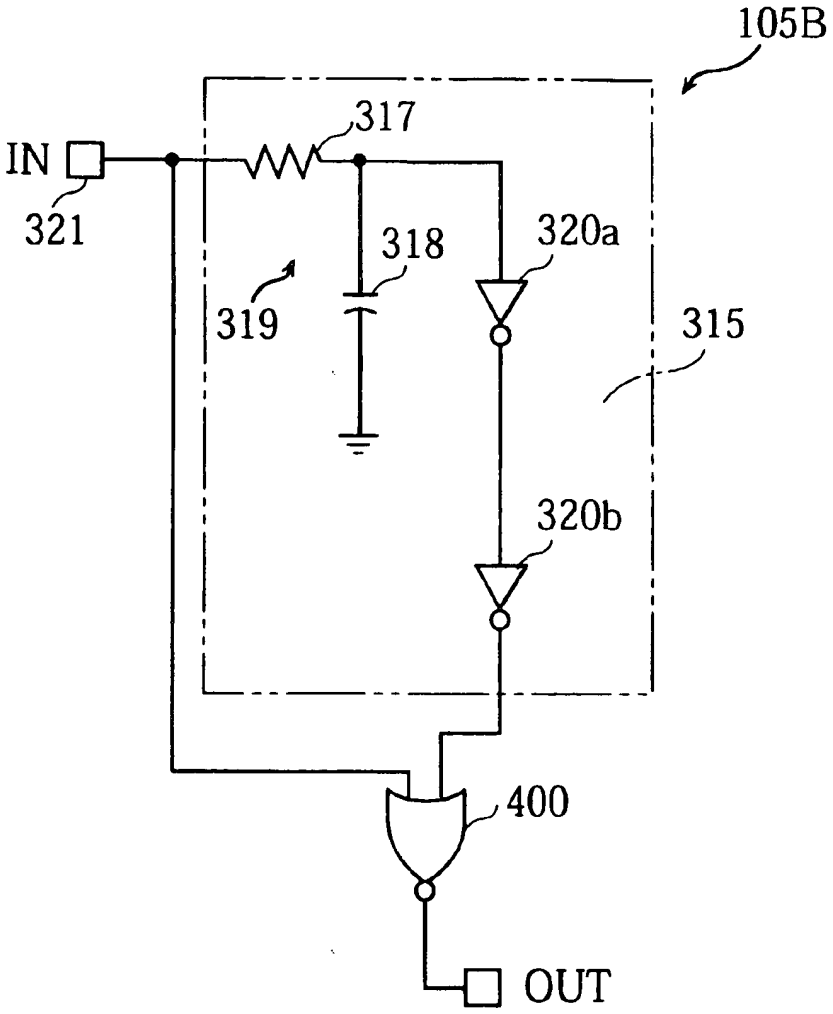


FIG. 59

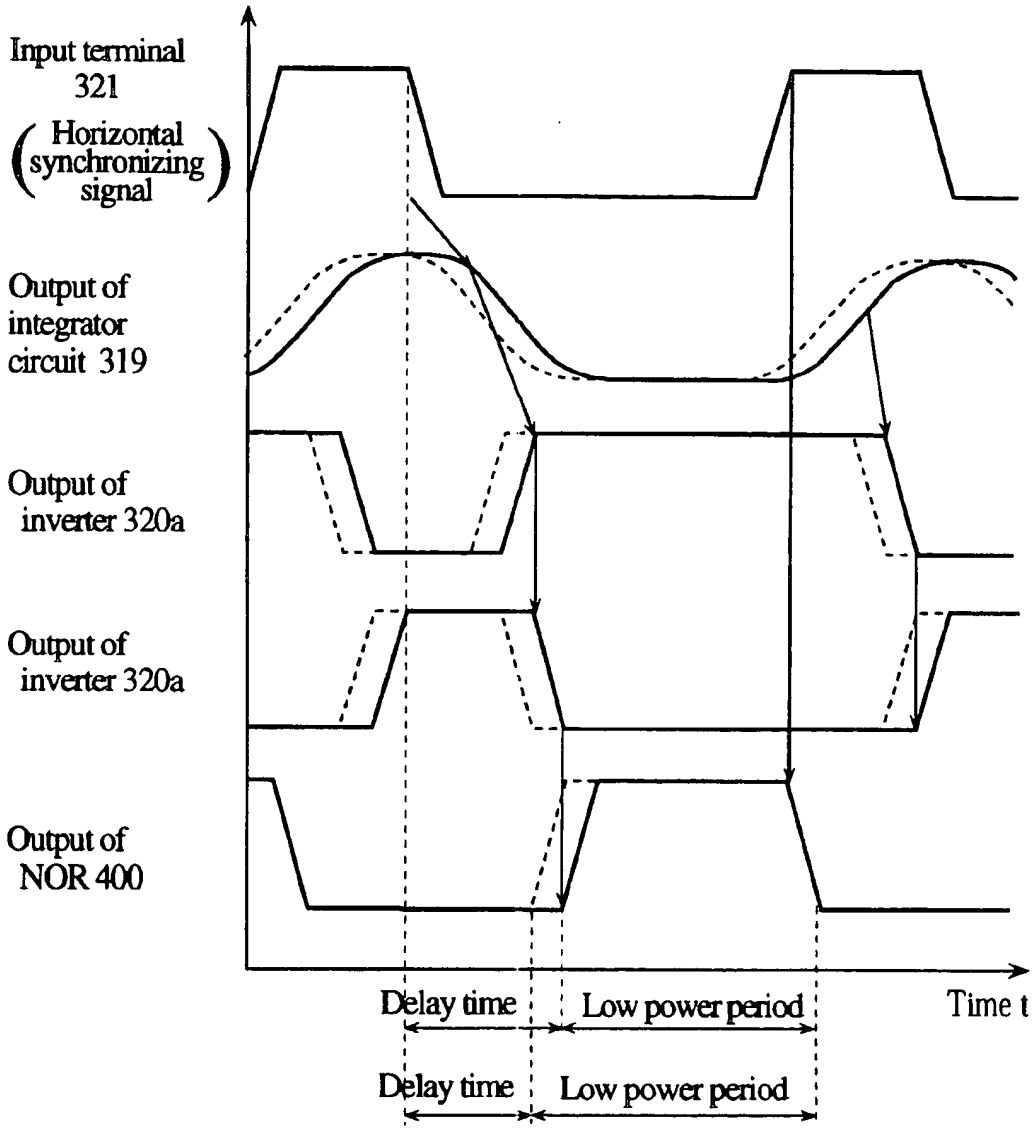
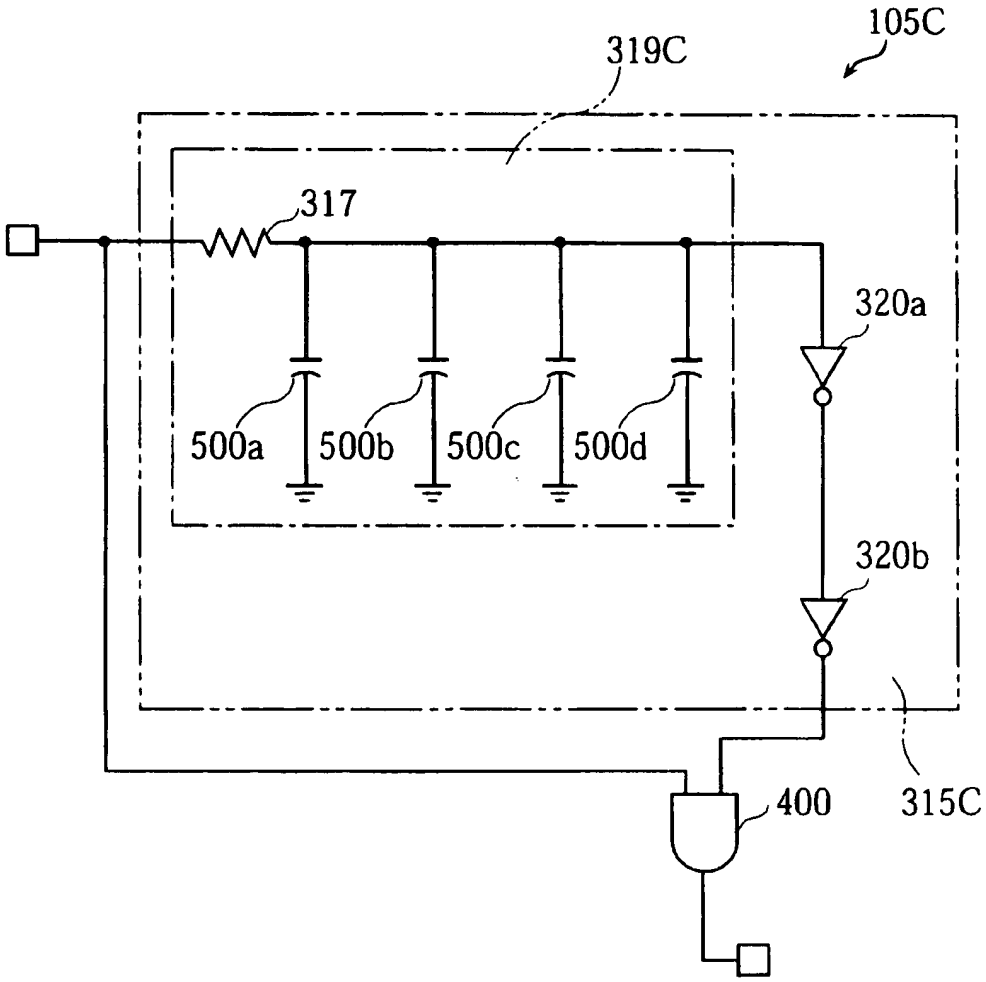

Input terminal 321
(Horizontal synchronizing signal)
Output of integrator circuit 319
Output of inverter 320a
Output of inverter 320a
Output of NOR 400
Delay time
Low power period
Time t
Delay time
Low power period

FIG. 60



DRIVE CIRCUIT FOR ACTIVE MATRIX LIQUID CRYSTAL DISPLAY

TECHNICAL FIELD

This invention relates to a driver circuit for an active matrix liquid crystal display comprising a resistive dividing type digital to analog converter circuit.

BACKGROUND ART

A driver circuit for an active matrix liquid crystal display capable of displaying multi-scale gray images or full-color images generally comprises a digital-to-analog converter circuit (DAC) so that analog video signals are outputted. A capacitor based DAC is well known in the art as one type of such a DAC. However, such a capacitor based DAC has a drawback in that a linear output voltage characteristic cannot be obtained easily when such a capacitor based DAC is employed in constructing a driver circuit for a liquid crystal display (LCD). In view of this drawback, a resistive dividing type DAC using resistance elements has also been employed for an LCD driver circuit.

Among such resistive dividing type DACs, some types are constructed utilizing resistance elements and switching elements, both having an individual component form, but many types are constructed within a single crystalline silicon integrated circuit (IC) and formed in a chip form. Such a driver IC has been used for conventional LCD driver circuits. Specifically, in those driver circuits having resistive dividing type DACs, driver ICs are attached onto an array substrate by a tape automated bonding or by directly mounting onto the array substrate.

However, such an LCD driver circuit has drawbacks as described in the following.

(1) A driver IC is essential as a component of an LCD, and therefore the component cost is high.

(2) A step of mounting the driver IC onto an array substrate is inevitably required.

(3) The thickness of an LCD is increased corresponding to the thickness of the driver IC, and in addition, the driver IC requires a large area in the array substrate. These have been the major obstacles in the attempts to reduce the physical sizes and thickness of LCDs.

(4) Furthermore, in conventional driver circuits utilizing a crystalline silicon, a silicon in which an n-type or p-type impurity of approximately $10^{16}/cm^3$ is doped is typically employed for resistance elements that constitute DACs in the driver circuits. A resistance value of these resistance elements must be controlled with extremely high precision by controlling a concentration of these impurities so as to suppress an output variation among these DAC chips. As a result, in order to produce a chip with an extremely precise resistance value, an ion implantation method should be employed in doping an n-type or p-type impurity in a crystalline silicon. However, by this method, it is extremely difficult to suppress a variation of the resistance value within a predetermined range when a large chip size or a large number of the chip is required, and moreover a throughput until completing the driver circuit is low.

In addition to the above drawbacks, conventional LCD driver circuits have such drawbacks as described below, in view of reducing their power consumption.

A resistive dividing type DAC is a well-known circuit, and while some of the DACs are constructed utilizing the resistance elements and switching elements having an individual component form, many of the DACs commercially

available have a chip form incorporated within a single crystalline silicon (c-Si) IC. Recently, there have been developed techniques intended to incorporate an LCD driver circuit including such DACs on a glass substrate by forming thin-film transistors (herein after referred as 'TFTs') utilizing poly-silicon (p-Si). However, because p-Si TFTs are inferior to c-Si transistors' in their performance and thereby in the power efficiency in the circuits, the effective reduction in power consumption has been difficult for such an LCD driver circuit incorporated on the grass substrate, although such a circuit has certain advantages such as low cost and small sizes owing to the fact that they are capable of eliminating driver ICs. In conventional LCD driver circuits, a waste of power consumption is noted particularly during a writing period for source lines and pixel electrodes. The discussion will now focus on this account. Generally speaking, a large amount of capacitive load is connected to a source line because a certain capacitance is generated in each intersection of a source line and gate line, or in each gap between a source line and counter electrode. Therefore, when a driving voltage is outputted from a driver circuit to a source line, a potential of the source line does not reach a required voltage for driving liquid crystals immediately after the driving voltage is outputted, and a certain amount of time is required until a desired voltage is obtained. After this amount of time, i.e., a writing period to a source line elapses, a gate scanning pulse is outputted to a pixel transistor, and thereby a potential of a pixel electrode reaches a desired voltage. Or, a gate scanning pulse is outputted almost simultaneously with an output of a driving voltage, and a potential of a pixel electrode reaches a desired voltage corresponding to the change of a potential of a source line. A writing to a pixel electrode is thus completed according to either of the above described manners. Therefore, there is essentially no need to continue applying a predetermined driving voltage to a source line. Nevertheless, in conventional driving methods, such a writing period to a source line or a pixel electrode has been made equivalent to one horizontal synchronizing period. This is because the writing to a source line or a pixel electrode has been controlled by a horizontal synchronizing signal. As a result, in prior arts, the driver circuit continues a normal operation for applying a driving voltage even during the period in which there is no need to keep applying a predetermined driving voltage to a source line. This has been a major drawback from the viewpoint of reduction in power consumption.

In view of the above-described disadvantages in prior arts, it is therefore an object of the present invention to provide a driver circuit for an active matrix liquid crystal display in which, by eliminating a driver IC from a component of an LCD, the component cost is reduced, the manufacturing steps are simplified, and moreover the reduction of sizes and thickness is achieved.

It is another object of the present invention to provide a driver circuit for an active matrix liquid crystal display in which the reduction of power consumption is achieved by reducing a current consumption of the digital-analog converter circuits therein during a period excluding a normal operation period.

DISCLOSURE OF THE INVENTION

In accordance with the first aspect of the invention, there is provided a driver circuit for an active matrix liquid crystal display formed on an array substrate of the liquid crystal display comprising:

a resistive dividing type digital-to-analog converter circuit (DAC), comprising a plurality of resistance ele-

ments and a plurality of switches related to the resistance elements;

the driver circuit constructed so that an output signal from the DAC is outputted as a driving voltage for a liquid crystal display portion of the liquid crystal display via a current amplifier element having an impedance conversion function wherein a voltage amplification ratio of the current amplifier element is 1;

the driver circuit characterized in that the resistance elements are composed of an impurity-containing semiconductor layer formed on the array substrate.

According to the above-mentioned construction, it is made possible to reduce the component cost of an LCD since the driver circuit is formed on the array substrate without using driver ICs as a component for the LCD. Moreover, it is also made possible to reduce the manufacturing cost since the step of mounting the driver ICs onto the substrate is made unnecessary. In addition, the reduction in the thickness and sizes of an LCD can be achieved easily. In particular, the above-mentioned semiconductor layer is formed simultaneously with a step of forming pixel transistors without independently necessitating an step of forming the above-mentioned semiconductor layer, and therefore it is possible to substantially reduce the manufacturing cost.

Furthermore, according to the above construction, it is made possible to produce resistance elements for a driver circuit having a large circuit area without taking into account a joint areas between each chip since the resistance elements are integrally formed on the array substrate. Generally, a mass non-separated type ion shower method, which has a large throughput, is employed as a method for doping an n-type or p-type impurity over a large area. When this method is employed, a variation of resistance values in the entire glass substrate becomes relatively large, and an output variation in the entire glass substrate becomes approximately 20 mV or higher, but an output variation between the channels next to each other is at most within several mV. It is therefore possible to set a large process margin since there are no joint areas between each chip, as seen in prior arts. The output variation in the entire array is approximately 0.1 V, but this causes no problem since, if converted into a luminance variation in the liquid crystal panel, it falls within the range of 10%.

In addition, since the electric current is amplified by a current amplifier element, an output from the DAC circuit can be made substantially smaller in comparison with a output current necessary to charge a capacitive load of a source line. Therefore, the freedom in designing a circuit increases and the reduction in the display size and manufacturing cost is easily achieved.

For the current amplifier element, a voltage follower type op-amp, a source follower type thin film transistor (TFT), and the like may be employed.

In accordance with the second aspect of the invention, there is provided a driver circuit for an active matrix liquid crystal display formed on an array substrate of the liquid crystal display comprising:

a resistive dividing type DAC, comprising a plurality of resistance elements and a plurality of switches related to the resistance elements;

the driver circuit constructed so that an output signal from each of the DACs is directly outputted as a driving voltage for a liquid crystal display portion of the liquid crystal display;

the driver circuit characterized in that the resistance elements are composed of an impurity-containing semiconductor layer formed on the array substrate.

According to the above construction, the display size and manufacturing cost can be further reduced by making the circuit scale smaller, although the voltage required for driving the LCD portion has to be generated by the DAC circuit alone. In addition, an output voltage characteristic with high precision and small variation can be easily obtained since the voltage from the DAC is directly outputted as a driving voltage for the LCD portion.

Furthermore, according to the above construction in which the signal amplifier element is eliminated, when compared with, for example, the construction with the amplifier element formed on the array substrate among the ones employing the amplifier element, the entire circuit area can be made smaller corresponding to the circuit area allotted for the signal amplifier element, and the power consumption can be also reduced corresponding to the power to be consumed by the amplifier element. Likewise, when compared with the construction with an amplifier element mounted onto array substrate, for example, the cost reduction can be achieved since the amplifier element is eliminated from the components of an LCD, and the step of mounting the amplifier element is also eliminated.

In accordance with the third aspect of the invention, there is provided a driver circuit for an active matrix liquid crystal display comprising:

a resistive dividing type DAC, comprising a plurality of resistance elements and a plurality of switches related to the resistance elements;

the driver circuit constructed so that an output signal from the DAC is outputted as a driving voltage for a liquid crystal display portion of the liquid crystal display via a current amplifier element having an impedance conversion function wherein a voltage amplification ratio of the current amplifier element is 1, the current amplifier element being mounted on the array substrate and a remaining portion of the driver circuit excluding the current amplifier element being formed on the array substrate;

the driver circuit characterized in that the resistance elements are composed of an impurity-containing semiconductor layer formed on the array substrate.

According to the above construction, the manufacturing steps are slightly increased since a step of mounting an amplifier element becomes necessary. The effect of the size and thickness reduction of the LCD also becomes slightly small because of the amplifier element incorporated into an IC chip form. However, in the case of forming the amplifier element on the array substrate, unlike the case of forming switching transistors, it is necessary that the formed transistor be capable of achieving an accurate amplification ratio, and therefore, the manufacturing is rendered very difficult particularly when a non-single crystalline material is utilized. Hence, the construction where an IC chip-formed individual component is employed only for the current amplifier element has an advantage in that the manufacturing is made easier than the construction where the amplifier element is formed on the array substrate.

In accordance with the fourth aspect of the invention, there is provided a driver circuit as in one of the first to third aspects of the invention, wherein the semiconductor layer is composed of a non-single crystalline material including silicon and germanium, and contains an impurity which acts as a donor or an acceptor.

According to the above construction, the same effect as in the first aspect of the invention can be attained.

In accordance with the fifth aspect of the invention, there is provided a driver circuit as in one of the first to third

aspects of the invention, wherein the semiconductor layer is a non-single crystalline silicon layer and is at least one layer of an n-type layer and a p-type layer.

According to the above construction, the same effect as in the first aspect of the invention can be attained.

In accordance with the sixth aspect of the invention, there is provided a driver circuit as in one of the first to third aspects of the invention, wherein the DAC is an R-b 2R ladder type DAC.

According to the above construction employing an R-2R ladder type DAC, it is made possible to obtain a linear output voltage characteristic. Moreover, an adverse effect on an output voltage characteristic by a variation of resistance values is rendered small since the DAC is constructed by two types of resistance elements each having a different resistance value. In addition, the total area occupied by the resistance elements in the DAC is made remarkably smaller in comparison with the case where the same output voltage characteristic is realized by utilizing a DAC other than an R-2R ladder type construction.

The reason is as follows. When an R-2R ladder type DAC for four-bit digital input signal is employed, assuming a reference resistance value is r1, the resistance value of all the resistance elements used (note that this means a resistance value converted into a circuit occupying area of resistance elements, not a composite resistance value) results in 13×r1. Now, assume that a linear output voltage characteristic as in the above construction is realized by utilizing a so-called weighted resistance type DAC. An example of the weighted resistance value type DAC can be realized by the construction as follows. The DAC has two types of power supplies (which correspond to VH and VL in FIG. 2) and a certain number of series circuit connected in parallel. Each of the series circuits has a switching element for alternatively selecting one of the power supplies, and a resistance element with one end connected to the switching element and the other end connected to the output terminal. The number of the series circuit corresponds with the bit number of digital input signal. Each switching state of the switching elements is controlled in response to the digital input signal so as to select one of the power supplies. In this example, a resistance ratio of each resistance element against the reference resistance value (the resistance value of the resistance element responsive to the least significant bit) is set at 1:2n−1 ('n' is the bit number of the digital input signal).

According to this example, in the case of 4-bit digital input signal, if a reference resistance value is r1, the resistance values of the rest of the three resistance elements are 2×r1, 4×r1, and 8×r1 respectively, and the resistance value of all the resistance elements used accordingly results in 15×r1. On the other hand, in the case of the construction according to the sixth aspect of the invention, the resistance value of all the resistance elements used results in 13×r1, as described above. Hence, when it is assumed that each of the resistance elements is formed by a non-single crystalline semiconductor layer having an identical sheet resistance, the total area occupied by the resistance elements in the weighted resistance type DAC requires 15/13 times in comparison with the construction according to the sixth aspect of the invention. As the bit number of the digital input signal increases further, the weighted resistance type DAC correspondingly requires a larger total area occupied by the resistance elements than that of the construction according to the sixth aspect of the invention. It is apparent from the above example that the construction according to the sixth aspect of the invention can achieve remarkable reduction of the total area occupied by the resistance element in the DAC.

In accordance with the seventh aspect of the invention, there is provided a driver circuit as in the fourth aspect of the invention, wherein the DAC is an R-2R ladder type DAC.

According to the above construction, the same effect as in the sixth aspect of the invention can be attained.

In accordance with the eighth aspect of the invention, there is provided a driver circuit as in the fifth aspect of the invention, wherein the DAC is an R-2R ladder type DAC.

According to the above construction, the same effect as in the sixth aspect of the invention can be attained.

In accordance with the ninth aspect of the invention, there is provided a driver circuit as in one of the first to third aspects of the invention, wherein the DAC is a voltage potentiometer type DAC.

According to the above construction employing a voltage potentiometer type DAC, the output voltage results in the voltage weighted corresponding to the ratio of the resistance values of the resistance elements connected in series. Therefore, the output voltage characteristic can be easily made into the one with a desired curve, not just into a linear characteristic, by appropriately setting the resistance values of the resistance elements. Moreover, if the electric current flowing via the switching elements is small, the current dividing or voltage drop caused by the switching elements is avoided and the output voltage is determined only by the voltage dividing by the resistance elements. Therefore, the circuit can be designed without worrying about ON resistance of the switching elements.

In accordance with the 10th aspect of the invention, there is provided a driver circuit as in the fourth aspect of the invention, wherein the DAC is a voltage potentiometer type DAC.

According to the above construction, the same effect as in the ninth aspect of the invention can be attained.

In accordance with the 11th aspect of the invention, there is provided a driver circuit as in the fifth aspect of the invention, wherein the DAC is a voltage potentiometer type DAC.

According to the above construction, the same effect as in the ninth aspect of the invention can be attained.

In accordance with the 12th aspect of the invention, there is provided a driver circuit as in one of the first to third aspects of the invention, wherein the DAC comprises:

a first DAC section which operates in response to one of more significant bit data and lesser significant bit data of digital video input data; and

a second DAC section which uses an output voltage as a reference voltage and operates in response to the other one of more significant bit data and lesser significant bit data of digital video input data; and

wherein one of the DAC sections is an R-2R ladder type DAC, and the other one of the DAC sections is a voltage potentiometer type DAC.

According to the above construction, both types of the DACs, an R-2R ladder type DAC and a voltage potentiometer type DAC, are employed for the DACs incorporated in the driver circuit, and thereby it is made possible to obtain a driver circuit having both of the advantages intrinsic to each type of the DACs.

In accordance with the 13th aspect of the invention, there is provided a driver circuit as in one of the first to third aspects of the invention, further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between the driver circuit and a capacitive load connected to a

source line only during the remaining period in response to the first switching signal;

wherein the DAC is composed of a voltage potentiometer type DAC comprising:

a series circuit wherein a plurality of the resistance elements are connected in series, one end of the series circuit is connected to a high voltage power supply terminal, and the other end is connected to a low voltage power supply terminal;

a first switch connected between the one end of the series circuit and the high voltage power supply terminal or between the other end of the series circuit and the low voltage supply terminal, the first switch to be turned to an ON state during the normal operation period and to be turned to an OFF state during the remaining period in response to the first switching signal; and

a group of second switches wherein a switching state of each of the second switches is controlled in response to a digital video data, and each of the second switches is connected between a connecting point of each of the resistance elements and an output terminal of the DAC.

According to the above construction, the following effects are attained.

During the normal operation period, the first switch is turned to ON state in response to the first switching signal, and the switching states of the second switch group is controlled in response to the digital video data. The driving voltage corresponding to the digital video data is thereby outputted to the source line.

During the remaining period excluding the normal operation period in one horizontal synchronizing period, the first switch is turned to OFF state in response to the first switching signal. A power supply to the resistance elements is thereby shut off, and an electric current constantly flowing in the resistance element becomes "0". It is thereby made possible to reduce the electric power consumed in the resistance elements during the low power period. In addition, during this low power period, the electrical connection between the driver circuit and the capacitive load is cut off by the means for cutting off the electrical connection. The potential of the capacitive load is thereby retained, and it is made possible to prevent a deterioration of the display characteristics of the liquid crystal resulting from a potential variation of the pixel electrodes. As a result, it is made possible that an entire period excluding a period necessary to change the voltage of the capacitive load is made to be the low power period.

The term "normal operation period" herein is intended to mean, as defined in detail in "the Best Mode for Carrying Out the Invention" hereinafter, (1) a period during which a potential of a source line reaches a desired potential (i.e., a source line writing period) in the case where a gate pulse is provided to a pixel transistor after the potential of the source line completely reaches the desired voltage, or (2) a period during which a potential of a pixel electrode reaches a desired potential (i.e., a pixel electrode writing period) in the case where the time at which a gate pulse is provided to a pixel transistor and the time at which a potential of a source line begins to change by the change of an output voltage from a driver circuit are almost simultaneous. In other words, the term "normal operation period" means a period in which, with a various capacitances connected to a source line taken into consideration, a DAC must continue to output a driving voltage corresponding to a digital data so as to substantially completely change a potential of a pixel electrode. Therefore, in one horizontal synchronizing period, it is not necessary for a DAC to continue a normal operation during a remaining period in which the normal operation period is excluded. Hence, the present invention achieves an effect of reducing power consumption when compared with prior arts in which a DAC continues a normal operation during the remaining period as well as the normal operation period.

The "means for cutting off the electrical connection between the driver circuit and a capacitive load" may be (1) a construction in which an output switch is provided on the output side in a driver circuit, and the switch is turned to ON state during the normal operation period and OFF state during the remaining period, or may be (2) a construction in which a driving power supply for the current amplifier element is turned to ON state during the normal operation period and OFF state during the remaining period. However, this construction (2) is limited for an amplifier element having a construction where an output impedance results in high impedance when the driving power supply is turned OFF. For an amplifier element with a construction where the output impedance does not results in high, an output switch should be provided. Further, it may be (3) a construction in which a group of second switches in the DAC is forcibly turned OFF during the remaining period.

In accordance with the 14th aspect of the invention, there is provided a driver circuit as in the 13th aspect of the invention, wherein the means for cutting off the electrical connection between the driver circuit and the capacitive load connected to the source line is such an output switch provided on an output side of the driver circuit that, in response to the first switching signal, the output switch is turned to an ON state during the normal operation period, and is turned to an OFF state during the remaining period so as to cut off the electrical connection.

According to the above construction, the electrical connection between the driver circuit and the capacitive load connected to the source line is cut off during the remaining period by the output switch provided on the output side in the driver circuit. By contrast, according to a construction of cutting off the power supply of the amplifier, there arises some cases in which the output impedance does not become high when the power supply is cut off, depending on the construction of the amplifier element. In these cases, it is not possible to cut off the electrical connection between the driver circuit and the capacitive load. In addition, in a construction of turning OFF a group of second switches forcibly, the circuit design becomes slightly more complex since it is necessary to previously store a fixed data for cutting off the group of second switches and to provide a switch for selecting a video data during the normal operation period and the fixed data during the low power period. On the other hand, according to the above construction with the output switch, it is easily made possible to cut off the electrical connection with the capacitive load because the above-described difficulties do not occur.

In accordance with the 15th aspect of the invention, there is provided a driver circuit as in one of the first to third aspects of the invention, further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between the driver circuit and a capacitive load connected to a source line only during the remaining period in response to the first switching signal;

wherein the DAC is composed of a voltage potentiometer type DAC comprising:

a series circuit wherein the resistance elements are connected in series, one end of the series circuit is commonly connected to a first high voltage power supply terminal and a second high voltage power supply terminal having a lower voltage level than the first high voltage power supply, and the other end is connected to a low voltage power supply terminal;

a third switch connected between one end of the series circuit and the power supply terminals, the third switch for switching an electrical connection of the one end of the series circuit in response to the first switching signal so that the one end of the series circuit is connected to the first high voltage power supply terminal during the normal operation period and is connected to the second high voltage power supply terminal during the remaining period; and

a group of second switches wherein a switching state of each of the second switches is controlled in response to a digital video data, and each of the second switches is connected between a connecting point of each of the resistance elements and an output terminal of the DAC.

According to the above construction, the following effects are attained.

During the normal operation period, the third switch is switched to the first high voltage power supply side in response to the first switching signal, and the switching states of the group of second switches are controlled in response to the digital video data. Thereby, a driving voltage corresponding to the digital video data is outputted to the source line.

During the remaining period, the third switch is switched to the second high voltage power supply side in response to the first switching signal. Thereby, the reduction in power consumption can be achieved by reducing the current flowing in the DAC. In addition, in the low power period, the electrical connection between the driver circuit and the capacitive load is cut off by the means for cutting off the electrical connection with the capacitive load. The potential of the capacitive load is thereby retained. Consequently, it is made possible that an entire period excluding a period necessary to change a voltage of the capacitive load is set to be the low power period.

According to this construction, it is possible to fix a potential in the circuit since a certain fixed current flows in the circuit, although the degree of the reduction in power consumption is slightly less than a construction with the means for cutting off the power supply. Therefore, it is made possible to reduce the occurrence of a signal noise resulting from a sudden current increase caused by a normal operation voltage at the transition to the normal operation period.

In accordance with the 16th aspect of the invention, there is provided a driver circuit as in the 15th aspect of the invention, wherein the means for cutting off the electrical connection between the driver circuit and the capacitive load connected to the source line is such an output switch provided on an output side of the driver circuit that, in response to the first switching signal, the output switch is turned to an ON state during the normal operation period, and is turned to an OFF state during the remaining period so as to cut off the electrical connection.

According to the above construction employing the output switch, it is made possible to completely cut off the electrical connection with the capacitive load by a simple circuit construction.

In accordance with the 17th aspect of the invention, there is provided a driver circuit as in one of the first to third aspects of the invention, further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between the driver circuit and a capacitive load connected to a source line only during the remaining period in response to the first switching signal;

wherein the DAC is composed of an R-2R ladder type DAC comprising:

an R-2R ladder resistance element network composed of two types of the resistance elements, each type having a different resistance value;

a group of fourth switches, each provided for each bit of digital video data, for determining an output voltage by alternatively selecting between a connecting state with a high voltage power supply terminal and a connecting state with a low voltage power supply terminal; and

a second switching signal generator circuit for generating a second switching signal to control a switching state of each of the fourth switches and outputting the second switching signal to the group of fourth switches, wherein the second switching signal generator circuit receives the first switching signal and the digital video data, and outputs a data corresponding to the digital video input data as the second switching signal during the normal operation period, and outputs a fixed data as the second switching signal during the remaining period, the fixed data causing a current value in the resistance element network to be not more than an median current value between a minimum current value and a maximum current value in the resistance element network.

According to the above construction, the following effects are attained.

During the normal operation period, the second switching signal generator circuit outputs the second switching signal corresponding to the digital video input data. A driving voltage corresponding to the digital video input data is thereby outputted to the source line.

During the remaining period, the second switching signal generator circuit makes the input data into an fixed input data which results in a current value flowing in the resistance network being not more than the median current value between the minimum current value and the maximum current value, and outputs the fixed data as a second switching signal to the group of fourth switches. Thereby, the power consumption in the DAC is made less than the average power consumption in prior arts, in which a DAC continues the normal operation throughout one horizontal synchronizing period. As a result, this construction too achieves the reduction in power consumption of the DAC.

According to this construction, it is possible to fix a potential in the circuit since a certain fixed current flows in the circuit, although the degree of the reduction in power consumption is slightly less than a construction with the means for cutting off the power supply. Therefore, it is made possible to reduce the occurrence of a signal noise resulting from a sudden current increase caused by a normal operation voltage at the transition to the normal operation period.

In accordance with the 18th aspect of the invention, there is provided a driver circuit as in the 17th aspect of the invention, wherein the means for cutting off the electrical

connection between the driver circuit and the capacitive load connected to the source line is such an output switch provided on an output side of the driver circuit that, in response to the first switching signal, the output switch is turned to an ON state during the normal operation period, and is turned to an OFF state during the remaining period so as to cut off the electrical connection.

According to the above construction employing the output switch, it is made possible to completely cut off the electrical connection with the capacitive load by a simple circuit construction.

In accordance with the 19th aspect of the invention, there is provided a driver circuit as in one of the first to third aspects of the invention, further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between the driver circuit and a capacitive load connected to a source line only during the remaining period in response to the first switching signal;

wherein the DAC is composed of an R-2R ladder type DAC comprising:

an R-2R ladder resistance element network composed of two types of the resistance elements, each type having a different resistance value;

a group of fifth switches for determining an output voltage; and

a third switching signal generator circuit for generating a third switching signal to control a switching state of each of the fifth switches and outputting the third switching signal to the group of fifth switches, the third switching signal generator circuit comprising a storage circuit for storing a fixed data causing the group of fifth switches to be OFF state, wherein the third switching signal generator circuit receives the first switching signal and digital video data, and outputs during the normal operation period a data corresponding to the digital video data as the third switching signal, and outputs during the remaining period the fixed data stored in the storage circuit as the third switching signal so as to cut off the power supply to the resistance element network.

According to the above construction, the following effects are attained.

During the normal operation period, the third switching signal generator circuit outputs the third switching signal corresponding to the digital video input data. A driving voltage corresponding to the digital video input data is thereby outputted to the source line.

During the remaining period, the third switching signal generator circuit outputs the fixed data stored in the storage circuit as a third switching signal. All of the fifth switches are thereby turned to OFF state. Consequently, the current flowing in the circuit results in "0", and the reduction in power consumption is thus attained.

In accordance with the 20th aspect of the invention, there is provided a driver circuit as in the 19th aspect of the invention, wherein the means for cutting off the electrical connection between the driver circuit and the capacitive load connected to the source line is such an output switch provided on an output side of the driver circuit that, in response to the first switching signal, the output switch is turned to an ON state during the normal operation period, and is turned to an OFF state during the remaining period so as to cut off the electrical connection.

According to the above construction employing the output switch, it is made possible to completely cut off the electrical connection with the capacitive load by a simple circuit construction.

In accordance with the 21st aspect of the invention, there is provided a driver circuit as in one of the first to third aspects of the invention, further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between the driver circuit and a capacitive load connected to a source line only during the remaining period in response to the first switching signal;

wherein the DAC comprises:

a first DAC section which operates in response to more significant bits of digital video input data; and

a second DAC section, which comprises a first connecting terminal receiving a higher voltage output from the first DAC section and a second connecting terminal receiving a lower voltage output from the first DAC section, which employs as a reference voltage a voltage between the first connecting terminal and the second connecting terminal, and which operates in response to lesser significant bits of the digital video input data;

the first DAC section being composed of a voltage potentiometer type DAC and the second DAC section being composed of an R-2R ladder type DAC;

the first DAC section comprising:

a series circuit wherein a plurality of the resistance elements are connected in series, one end of the series circuit is connected to a high voltage power supply terminal, and the other end is connected to a low voltage power supply terminal;

a sixth switch connected between one end of the series circuit and the high voltage power supply terminal or between the other end of the series circuit and the low voltage power supply circuit, the sixth switch to be turned to an ON state during the normal operation period and to be turned to an OFF state during the remaining period in response to the first switching signal;

a group of seventh switches each connected between a connecting point of each of the resistance elements in the series circuit and the first connecting terminal, the seventh switches controlled by the more significant bits of the digital video input data; and

a group of eighth switches each connected between a connecting point of each of the resistance elements in the series circuit and the second connecting terminal, the eighth switches controlled by the more significant bits of the digital video input data;

the second DAC section comprising:

an R-2R ladder resistance element network composed of two types of the resistance elements, each type having a different resistance value; and

a group of ninth switches for alternatively selecting between a connecting state with the first connecting terminal and a connecting state with the second connecting terminal in response to the lesser significant bits of the digital video input data;

the driver circuit, wherein:

during the normal operation period, the sixth switch is turned to the ON state, a switching state of each of

the seventh switches and a switching state of each of the eighth switches are controlled corresponding to the more significant bits of the digital video input data, and a switching state of each of the ninth switches is controlled corresponding to the lesser significant bits of the digital video input data; and

during the remaining period, the sixth switch is turned to the OFF state and the electrical connection with the capacitive load is cut off by the means for cutting off the electrical connection.

According to the above construction, the following effects are attained.

During the normal operation period, the sixth switch is turned to ON state, the switching states of the seventh switches and eighth switches are controlled in response to the more significant bits of the digital video data, and the switching state of the ninth switch is controlled in response to the lesser significant bits of the digital video data. A driving voltage corresponding to the digital video input data is thereby outputted to the source line.

During the remaining period, the sixth switch is turned to OFF state, and in addition, the electrical connection between the driver circuit and the capacitive load is cut off by the aforementioned means for cutting off the electrical connection. The current flowing in the circuit thereby becomes "0", and the reduction in power consumption is thus attained. In other words, the reduction in power consumption is achieved by cutting off the power supply of the first DAC section, the first DAC section being a voltage potentiometer type and allotted for the more significant bits.

In accordance with the 22nd aspect of the invention, there is provided a driver circuit as in the 21st aspect of the invention, wherein the means for cutting off the electrical connection between the driver circuit and the capacitive load connected to the source line is such an output switch provided on an output side of the driver circuit that, in response to the first switching signal, the output switch is turned to an ON state during the normal operation period, and is turned to an OFF state during the remaining period so as to cut off the electrical connection.

According to the above construction employing the output switch, it is made possible to completely cut off the electrical connection with the capacitive load by a simple circuit construction.

In accordance with the 22nd aspect of the invention, there is provided a driver circuit as in one of the first to third aspects of the invention, further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between the driver circuit and a capacitive load connected to a source line only during the remaining period in response to the first switching signal;

wherein the DAC comprises:

a first DAC section which operates in response to more significant bits of digital video input data; and

a second DAC section, which comprises a first connecting terminal receiving a higher voltage output from the first DAC section and a second connecting terminal receiving a lower voltage output from the first DAC section, which employs as a reference voltage a voltage between the first connecting terminal and the second connecting terminal, and which operates in response to lesser significant bits of the digital video input data;

the first DAC section being composed of a voltage potentiometer type DAC and the second DAC section being composed of an R-2R ladder type DAC;

the first DAC section comprising:

a series circuit wherein a plurality of the resistance elements are connected in series, one end of the series circuit is commonly connected to a first high voltage power supply terminal and a second high voltage power supply terminal having a lower voltage level than the first high voltage power supply terminal via a tenth switch for selecting a power supply, the tenth switch controlled by the first switching signal, and the other end of the series circuit is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of the resistance elements in the series circuit and the first connecting terminal, the seventh switches controlled by the more significant bits of the digital video input data; and

a group of eighth switches each connected between a connecting point of each of the resistance elements in the series circuit and the second connecting terminal, the eighth switches controlled by the more significant bits of the digital video input data;

the second DAC section comprising:

an R-2R ladder resistance element network composed of two types of the resistance elements, each type having a different resistance value; and

a group of ninth switches for alternatively selecting between a connecting state with the first connecting terminal and a connecting state with the second connecting terminal in response to the lesser significant bits of the digital video input data;

the driver circuit wherein:

during the normal operation period, the tenth switch is switched to the first high voltage power supply terminal, a switching state of the seventh switches and a switching state of the eighth switches are controlled corresponding to the more significant bits of the digital video input data, and a switching state of the ninth switches is controlled corresponding to the lesser significant bits of the digital video input data; and

during the remaining period, the tenth switch is switched to the second high voltage power supply terminal and the electrical connection with a capacitive load is cut off by the means for cutting off the electrical connection.

According to the above construction, the following effects are attained.

During the normal operation period, the tenth switch for selecting the power supply is switched to the first high voltage power supply terminal side, the switching states of the seventh switches and eighth switches are controlled in response to the more significant bits of the digital video data, and the switching state of the ninth switch is controlled in response to the lesser significant bits of the digital video data. A driving voltage corresponding to the digital video data is thereby outputted to the source line.

During the remaining period, the tenth switch for selecting the power supply is switched to the second high voltage power supply terminal side, and the electrical connection with the capacitive load is cut off by the aforementioned means for cutting off the electrical connection. The current

flowing in the circuit is thereby reduced, and the reduction in power consumption is thus attained. In other words, the reduction in power consumption is achieved by selecting a power supply voltage of the first DAC section, the first DAC section being a voltage potentiometer type and allotted for the more significant bits.

In accordance with the 24th aspect of the invention, there is provided a driver circuit as in the 23rd aspect of the invention, wherein the means for cutting off the electrical connection between the driver circuit and the capacitive load connected to the source line is such an output switch provided on an output side of the driver circuit that, in response to the first switching signal, the output switch is turned to an ON state during the normal operation period, and is turned to an OFF state during the remaining period so as to cut off the electrical connection.

According to the above construction employing the output switch, it is made possible to completely cut off the electrical connection with the capacitive load by a simple circuit construction.

In accordance with the 25th aspect of the invention, there is provided a driver circuit as in one of the first to third aspects of the invention, further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between the driver circuit and a capacitive load connected to a source line only during the remaining period in response to the first switching signal;

wherein the DAC comprises:

a first DAC section which operates in response to more significant bits of digital video input data; and

a second DAC section, which comprises a first connecting terminal receiving a higher voltage output from the first DAC section and a second connecting terminal receiving a lower voltage output from the first DAC section, which employs as a reference voltage a voltage between the first connecting terminal and the second connecting terminal, and which operates in response to lesser significant bits of the digital video input data;

the first DAC section being composed of a voltage potentiometer type DAC and the second DAC section being composed of an R-2R ladder type DAC;

the first DAC section comprising:

a series circuit wherein a plurality of the resistance elements are connected in series, one end of the series circuit is connected to a high voltage power supply terminal, and the other end is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of the resistance elements in the series circuit and the first connecting terminal, the seventh switches controlled by the more significant bits of the digital video input data; and

a group of eighth switches each connected between a connecting point of each of the resistance elements in the series circuit and the second connecting terminal, the eighth switches controlled by the more significant bits of the digital video input data;

the second DAC section comprising:

an R-2R ladder resistance element network composed of two types of the resistance elements, each type having a different resistance value;

a group of ninth switches provided for each of the lesser significant bits of the digital input data for alternatively selecting between a connecting state with the first connecting terminal and a connecting state with the second connecting terminal; and

a fourth switching signal generator circuit for generating a fourth switching signal to control a switching state of each of the ninth switches and outputting the fourth switching signal to the group of ninth switches, wherein the fourth switching signal generator circuit receives the lesser significant bits of the digital video input data and the first switching signal, and outputs during the normal operation period the fourth switching signal corresponding to the lesser significant bits of the digital video data, and outputs during the remaining period a fixed data as the fourth switching signal, the fixed data causing a current value in the resistance element network to be not more than the median current value between a minimum current value and a maximum current value in the resistance element network.

According to the above construction, the following effects are attained.

During the normal operation period, the switching state of the seventh and eighth switches are controlled in response to the more significant bits, and the ninth switches are switched to either a high voltage power supply or a low voltage power supply so as to obtain a driving voltage corresponding to the video data. The driving voltage corresponding to the digital video input data is thereby outputted to the source line.

During the remaining period, the fourth switching signal generator circuit makes the input data into an fixed input data which results in a current value in the resistance network being not more than the median current value between the minimum current value and the maximum current value, and outputs the fixed data as the fourth switching signal to the group of ninth switches. The power consumption in the second DAC section is thereby reduced, and the reduction in power consumption is thus attained. In other words, the reduction in power consumption is achieved by selecting an input data to the second DAC section, the second DAC section being an R-2R ladder type and allotted for the lesser significant bits.

In accordance with the 26th aspect of the invention, there is provided a driver circuit as in the 25th aspect of the invention, wherein the means for cutting off the electrical connection between the driver circuit and the capacitive load connected to the source line is such an output switch provided on an output side of the driver circuit that, in response to the first switching signal, the output switch is turned to an ON state during the normal operation period, and is turned to an OFF state during the remaining period so as to cut off the electrical connection.

According to the above construction employing the output switch, it is made possible to completely cut off the electrical connection with the capacitive load by a simple circuit construction.

In accordance with the 27th aspect of the invention, there is provided a driver circuit as in one of the first to third aspects of the invention, further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between the driver circuit and a capacitive load connected to a source line only during the remaining period in response to the first switching signal;

wherein the DAC comprises:

a first DAC section which operates in response to more significant bits of digital video input data; and

a second DAC section comprising a first connecting terminal receiving a higher voltage output from the first DAC section, an eleventh switch connected between the first connecting terminal and a power supply input line connected to the first connecting terminal, a second connecting terminal receiving a lower voltage output from the first DAC section, and a twelfth switch connected between the second connecting terminal and a power supply input line connected to the second connecting terminal, the second DAC section employing as a reference voltage a voltage between the first connecting terminal and the second connecting terminal, and the second digital-to-analog converter operating in response to lesser significant bit of the digital video input data;

the first DAC section being composed of a voltage potentiometer type DAC and the second DAC section being composed of an R-2R ladder type DAC;

the first DAC section comprising:

a series circuit wherein a plurality of the resistance elements are connected in series, one end of the series circuit is connected to a high voltage power supply terminal, and the other end is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of the resistance elements in the series circuit and the first connecting terminal, the seventh switches controlled by the more significant bits of the digital video input data; and

a group of eighth switches each connected between a connecting point of each of the resistance elements in the series circuit and the second connecting terminal, the eighth switches controlled by the more significant bits of the digital video input data;

the second DAC section further comprising:

an R-2R ladder resistance element network composed of two types of the resistance elements, each type having a different resistance value; and

a group of ninth switches provided for each of the lesser significant bits of the digital input data for alternatively selecting between a connecting state with the first connecting terminal and a connecting state with the second connecting terminal;

the driver circuit wherein:

during the normal operation period, the eleventh switch and the twelfth switch are turned to an ON state and a switching state of each of the seventh switches and a switching state of each of the eighth switches are controlled corresponding to the more significant bits of the digital video input data, and a switching state of each of the ninth switches is controlled corresponding to the lesser significant bits of the digital video input data; and

during the remaining period, the eleventh switch and the twelfth switch are turned to the OFF state and the electrical connection with the capacitive load is cut off by the means for cutting off the electrical connection.

According to the above construction, the following effects are attained.

During the normal operation period, the eleventh switch and twelfth switch is turned to ON state, the switching state of the seventh and eighth switches are controlled in response to the more significant bits of the digital video data, and the switching states of the ninth switches are controlled in response to the lesser significant bits of the digital video data. A driving voltage corresponding to the digital video input data is thereby outputted to the source line.

During the remaining period, the eleventh switch and twelfth switch is turned to OFF state. The current flowing in the second DAC section becomes "0", and the reduction in power consumption is thus attained. In other words, the reduction in power consumption is achieved by cutting off the power supply of the second DAC section, the second DAC section being an R-2R ladder type and allotted for the lesser significant bits.

In accordance with the 28th aspect of the invention, there is provided a driver circuit as in the 27th aspect of the invention, wherein the means for cutting off the electrical connection between the driver circuit and the capacitive load connected to the source line is such an output switch provided on an output side of the driver circuit that, in response to the first switching signal, the output switch is turned to an ON state during the normal operation period, and is turned to an OFF state during the remaining period so as to cut off the electrical connection.

According to the above construction employing the output switch, it is made possible to completely cut off the electrical connection with the capacitive load by a simple circuit construction.

In accordance with the 29th aspect of the invention, there is provided a driver circuit as in one of the first to third aspects of the invention, further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between the driver circuit and a capacitive load connected to a source line only during the remaining period in response to the first switching signal;

wherein the DAC comprises:

a first DAC section which operates in response to more significant bits of digital video input data; and

a second DAC section, which comprises a first connecting terminal receiving a higher voltage output from the first DAC section and a second connecting terminal receiving a lower voltage output from the first DAC section, which employs as a reference voltage a voltage between the first connecting terminal and the second connecting terminal, and which operates in response to lesser significant bits of the digital video input data;

the first DAC section being composed of a voltage potentiometer type DAC and the second DAC section being composed of an R-2R ladder type DAC;

the first DAC section comprising:

a series circuit wherein a plurality of the resistance elements are connected in series, one end of the series circuit is commonly connected to a first high voltage power supply terminal and a second high voltage power supply terminal having a lower voltage level than the first high voltage power supply terminal via a tenth switch for selecting a power supply, and the other end of the series circuit is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of the resistance ele-

ments in the series circuit and the first connecting terminal, the seventh switches controlled by the more significant bits of the digital video input data; and

a group of eighth switches each connected between a connecting point of each of the resistance elements in the series circuit and the second connecting terminal, the eighth switches controlled by the more significant bits of the digital video input data;

the second DAC section comprising:

an R-2R ladder resistance element network composed of two types of the resistance elements, each type having a different resistance value;

a group of ninth switches provided for each of the lesser significant bits of the digital input data for alternatively selecting between a connecting state with the first connecting terminal and a connecting state with the second connecting terminal; and

a fourth switching signal generator circuit for generating a fourth switching signal to control a switching state of each of the ninth switches and outputting the fourth switching signal to the group of ninth switches, wherein the fourth switching signal generator circuit receives the lesser significant bits of the digital video input data and the first switching signal, and outputs during the normal operation period the fourth switching signal corresponding to the lesser significant bits of the digital video data, and outputs during the remaining period a fixed data as the fourth switching signal, the fixed data causing a current value in the resistance element network to be not more than the median current value between a minimum current value and a maximum current value in the resistance element network;

the driver circuit wherein:

during the normal operation period, the tenth switch is switched to the first high voltage power supply terminal, a switching state of the seventh switches and a switching state of the eighth switches are controlled corresponding to the more significant bits of the digital video input data, and a switching state of the ninth switches is controlled corresponding to the lesser significant bits of the digital video input data; and

during the remaining period, the tenth switch is switched to the second high voltage power supply terminal, the ninth switches are switched corresponding to the fixed input data, and the electrical connection with the capacitive load is cut off by the means for cutting off the electrical connection.

According to the above construction, the following effects are attained.

During the normal operation period, the tenth switch for selecting the power supply is switched to the first high voltage power supply terminal side, the switching states of the seventh switches and eighth switches are controlled in response to the more significant bits of the digital video data, and the ninth switches are switched to either a high voltage side or a low voltage side so as to obtain a driving voltage corresponding to the lesser significant bits of the video data. The driving voltage corresponding to the digital video data is thereby outputted to the source line.

During the remaining period, the tenth switch for selecting the power supply is switched to the second high voltage power supply terminal side, the ninth switches are switched in response to the aforementioned fixed input data, and the electrical connection with the capacitive load is cut off by the aforementioned means for cutting off the electrical connection. The second high voltage power supply is selected in the first DAC section, and the current flowing in the circuit is thereby reduced, and the supplied power for the second DAC section is accordingly reduced. In addition, in the second DAC section, the power consumption is further reduced with the use of the fixed data. In other words, the reduction in power consumption is achieved by selecting the power supply voltages of the first DAC section, the first DAC section being a voltage potentiometer type and allotted for the more significant bits, as well as by selecting the input data to the second DAC section, the second DAC section being an R-2R ladder type and allotted for the lesser significant bits.

In accordance with the 30th aspect of the invention, there is provided a driver circuit as in the 29th aspect of the invention, wherein the means for cutting off the electrical connection between the driver circuit and the capacitive load connected to the source line is such an output switch provided on an output side of the driver circuit that, in response to the first switching signal, the output switch is turned to an ON state during the normal operation period, and is turned to an OFF state during the remaining period so as to cut off the electrical connection.

According to the above construction employing the output switch, it is made possible to completely cut off the electrical connection with the capacitive load by a simple circuit construction.

In accordance with the 30th aspect of the invention, there is provided a driver circuit as in one of the first to third aspects of the invention, further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between the driver circuit and a capacitive load connected to a source line only during the remaining period in response to the first switching signal;

wherein the DAC comprises:

a first DAC section which operates in response to more significant bits of digital video input data; and

a second DAC section comprising a first connecting terminal receiving a higher voltage output from the first DAC section, an eleventh switch connected between the first connecting terminal and a power supply input line connected to the first connecting terminal, a second connecting terminal receiving a lower voltage output from the first DAC section, and a twelfth switch connected between the second connecting terminal and a power supply input line connected to the second connecting terminal, the second DAC section employing as a reference voltage a voltage between the first connecting terminal and the second connecting terminal, and the second digital-to-analog converter operating in response to lesser significant bit of the digital video input data;

the first DAC section being composed of a voltage potentiometer type DAC and the second DAC section being composed of an R-2R ladder type DAC;

the first DAC section comprising:

a series circuit wherein a plurality of the resistance elements are connected in series, one end of the series circuit is commonly connected to a first high voltage power supply terminal and a second high

voltage power supply terminal having a lower voltage level than the first high voltage power supply terminal via a tenth switch for selecting a power supply, and the other end of the series circuit is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of the resistance elements in the series circuit and the first connecting terminal, the seventh switches controlled by the more significant bits of the digital video input data; and

a group of eighth switches each connected between a connecting point of each of the resistance elements in the series circuit and the second connecting terminal, the eighth switches controlled by the more significant bits of the digital video input data;

the second DAC section comprising:

an R-2R ladder resistance element network composed of two types of the resistance elements, each type having a different resistance value; and

a group of ninth switches provided for each of the lesser significant bits of the digital input data for alternatively selecting between a connecting state with the first connecting terminal and a connecting state with the second connecting terminal;

the driver circuit wherein:

during the normal operation period, the tenth switch is switched to the first high voltage power supply terminal, a switching state of the seventh switches and a switching state of the eighth switches are controlled corresponding to the more significant bits of the digital video input data and a switching state of the ninth switches is controlled corresponding to the lesser significant bits of the digital video input data; and

during the remaining period, the tenth switch is switched to the second high voltage power supply terminal, the eleventh switch and the twelfth switch are turned to the OFF state and the electrical connection with the capacitive load is cut off by the means for cutting off the electrical connection.

According to the above construction, the following effects are attained.

During the normal operation period, the tenth switch for selecting the power supply is switched to the first high voltage power supply terminal side, the switching states of the seventh switches and eighth switches are controlled in response to the more significant bits of the digital video data, the ninth switches are switched to either a high voltage side or a low voltage side so as to obtain a driving voltage corresponding to the lesser significant bits of the video data, and the eleventh switch and twelfth switch are turned to ON state. A driving voltage corresponding to the digital video data is thereby outputted to the source line.

During the remaining period, the tenth switch for selecting the power supply is switched to the second high voltage power supply terminal side, the eleventh switch and twelfth switch are turned to OFF state, and the electrical connection with the capacitive load connected to the source line is cut off by the aforementioned means for cutting off the electrical connection. The second high voltage power supply is selected for the first DAC section, and the current flowing in the circuit is thereby reduced. In the second DAC section, the current flowing in the circuit becomes "0" by the cutting off the power supply. In other words, the reduction in power consumption is achieved by selecting the power supply voltages of the first DAC section, the first DAC section being a voltage potentiometer type and allotted for the more significant bits, as well as by cutting off the power supply to the second DAC section, the second DAC section being an R-2R ladder type and allotted for the lesser significant bits.

In accordance with the 32nd aspect of the invention, there is provided a driver circuit as in the 31st aspect of the invention, wherein the means for cutting off the electrical connection between the driver circuit and the capacitive load connected to the source line is such an output switch provided on an output side of the driver circuit that, in response to the first switching signal, the output switch is turned to an ON state during the normal operation period, and is turned to an OFF state during the remaining period so as to cut off the electrical connection.

According to the above construction employing the output switch, it is made possible to completely cut off the electrical connection with the capacitive load by a simple circuit construction.

In accordance with the 33rd aspect of the invention, there is provided a driver circuit as in one of the first to third aspects of the invention, further comprising:

a fifth switching signal generator circuit which receives a predetermined reference signal and generates a fifth switching signal for selecting one of the modes between a precharge period mode for a precharge which is carried out prior to writing video data into a source line and a remaining period mode excluding the precharge period mode;

wherein the DAC is composed of an R-2R ladder type DAC comprising:

an R-2R ladder resistance element network composed of two types of the resistance elements, each type having a different resistance value;

a group of fourth switches, each provided for each bit of digital video data, for determining an output voltage by alternatively selecting between a connecting state with a high voltage power supply terminal and a connecting state with a low voltage power supply terminal; and

a sixth switching signal generator circuit for generating a sixth switching signal to control a switching state of each of the fourth switches and outputting the sixth switching signal to the group of fourth switches, wherein the sixth switching signal generator circuit receives the fifth switching signal and digital video data, and outputs a data corresponding to the digital video data as the sixth switching signal during the remaining period, and outputs a fixed data as the sixth switching signal during the precharge period, the fixed data causing a current value in the resistance element network to be not more than an median current value between a minimum current value and a maximum current value in the resistance element network.

According to the above construction, during the precharge period, a combination of the switching states of the fourth switches is made, by the sixth switching signal generator circuit, to be such a combination as results in a current value in the resistance network being not more than the median current value between the minimum current value and the maximum current value in the resistance network. Therefore, it is made possible to reduce the power consumption in the precharge period.

In accordance with the 34th aspect of the invention, there is provided a driver circuit as in one of the first to third aspects of the invention, further comprising:

a fifth switching signal generator circuit which receives a predetermined reference signal and generates a fifth switching signal for selecting one of the modes between a precharge period mode for a precharge which is carried out prior to writing video data into a source line and a remaining period mode excluding the precharge period mode;

wherein the DAC comprises:

a first DAC section which operates in response to more significant bits of digital video input data; and

a second DAC section, which comprises a first connecting terminal receiving a higher voltage output from the first DAC section and a second connecting terminal receiving a lower voltage output from the first DAC section, which employs as a reference voltage a voltage between the first connecting terminal and the second connecting terminal, and which operates in response to lesser significant bits of the digital video input data;

the first DAC section being composed of a voltage potentiometer type DAC and the second DAC section being composed of an R-2R ladder type DAC;

the first DAC section comprising:

a series circuit wherein a plurality of the resistance elements are connected in series, one end of the series circuit is commonly connected to a first high voltage power supply terminal and a second high voltage power supply terminal having a lower voltage level than the first high voltage power supply terminal via a tenth switch for selecting a power supply, and the other end of the series circuit is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of the resistance elements in the series circuit and the first connecting terminal, the seventh switches controlled by the more significant bits of the digital video input data; and

a group of eighth switches each connected between a connecting point of each of the resistance elements in the series circuit and the second connecting terminal, the eighth switches controlled by the more significant bits of the digital video input data;

the second DAC section comprising:

an R-2R ladder resistance element network composed of two types of the resistance elements, each type having a different resistance value;

a group of ninth switches provided for each of the lesser significant bits of the digital input data for alternatively selecting between a connecting state with the first connecting terminal and a connecting state with the second connecting terminal; and

a fourth switching signal generator circuit for generating a seventh switching signal to control a switching state of each of the ninth switches and outputting the seventh switching signal to the group of ninth switches, wherein the seventh switching signal generator circuit receives the fifth switching signal and the lesser significant bits of the digital video data, and outputs a data corresponding to the lesser significant bits of the digital video input data as the seventh switching signal during the remaining period, and outputs a fixed data as the seventh switching signal during the precharge period, the fixed data causing a current value in the resistance element network to be not more than an median current value between a minimum current value and a maximum current value in the resistance element network;

the driver circuit wherein:

during the remaining period, the tenth switch is switched to the first high voltage power supply terminal, a switching state of the seventh switches and a switching state of the eighth switches are controlled corresponding to the more significant bits of the digital video input data, and a switching state of the ninth switches is controlled corresponding to the lesser significant bits of the digital video input data; and

during the precharge period, the tenth switch is switched to the second high voltage power supply terminal, the ninth switches are switched corresponding to the fixed input data, and the electrical connection with the capacitive load is cut off by the means for cutting off the electrical connection.

According to the above construction, during the remaining period excluding the precharge period, the tenth switch for selecting the power supply is switched to the first high voltage power supply terminal side, the switching states of the seventh switches and eighth switches are controlled corresponding to the more significant bits of the digital video data, and the ninth switches are switched to either a high power supply or low power supply so as to obtain a driving voltage corresponding to the lesser significant bits of the video data.

During the precharge period, the tenth switch for selecting the power supply is switched to the second high voltage power supply terminal side, and the ninth switches are switched in response to the aforementioned fixed data. It is thereby made possible to reduce the power consumption in the precharge period.

In accordance with the 35th aspect of the invention, there is provided a driver circuit as in the 13th aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the first switching signal is generated by which an output signal from the delay circuit for delaying the horizontal synchronizing signal for a predetermined time determined by a resistance value of the resistance element which composes the integrator circuit and a horizontal synchronizing signal are ANDed together, and therefore it is made possible to determine the length of a high level period of the first switching signal by the resistance value. Consequently, it is made possible to absorb the difference in the steady-state currents flowing in the resistance elements in the DAC, which is caused by a variation of the resistance values of the resistance elements in each substrate.

The description below further details the above effect. In the case of a resistance element on an array substrate having

a high resistance value, it is preferable that the low power period be short, since the current flowing in the DAC is relatively small and therefore it takes relatively a long time to charge a capacitive load connected to a source line SL. In this case, even if the low power period is made short (i.e., the normal operation period is made long), no adverse effect occurs in view of the reduction in power consumption because the power consumption during the normal operation period is decreased by the resistance elements having a high resistance value. On the other hand, in the case of a resistance element having a low resistance value, it is preferable that the low power period be long, since the current flowing in the DAC is relatively large and therefore the time required for charging the source line becomes relatively short. When there arises a need to change the lengths of the normal operation period and the low power period according to the resistance values of the resistance elements on each of the array substrates in order to meet the two requirements, one being the charging of the source line and the other being the reduction in power consumption, this construction enables the length of the high level period of the first switching signal to be automatically adjusted to the most suitable length by the first switching signal generator circuit so that it can meet the two requirements. It is therefore made possible to automatically carry out an adjustment for optimizing the power consumption regardless of the precision of the resistance elements, by constructing the integrator circuit with the resistance element formed on the same array substrate as the one on which the resistance elements of the DAC are formed. As a result, it is made possible to automatically carry out the adjustment for optimizing the power consumption for all the substrates regardless of the variation of the resistance elements.

In accordance with the 36th aspect of the invention, there is provided a driver circuit as in the 15th aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 35th aspect of the invention can be attained.

In accordance with the 37th aspect of the invention, there is provided a driver circuit as in the 17th aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 35th aspect of the invention can be attained.

In accordance with the 38th aspect of the invention, there is provided a driver circuit as in the 19th aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 35th aspect of the invention can be attained.

In accordance with the 39th aspect of the invention, there is provided a driver circuit as in the 21st aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 35th aspect of the invention can be attained.

In accordance with the 40th aspect of the invention, there is provided a driver circuit as in the 23rd aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 35th aspect of the invention can be attained.

In accordance with the 41st aspect of the invention, there is provided a driver circuit as in the 25th aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 35th aspect of the invention can be attained.

In accordance with the 42nd aspect of the invention, there is provided a driver circuit as in the 27th aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 35th aspect of the invention can be attained.

In accordance with the 43rd aspect of the invention, there is provided a driver circuit as in the 29th aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 35th aspect of the invention can be attained.

In accordance with the 44th aspect of the invention, there is provided a driver circuit as in the 31st aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 35th aspect of the invention can be attained.

In accordance with the 45th aspect of the invention, there is provided a driver circuit as in the 13th aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit and a capacitance value of the capacitance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the optimization of the normal operation period can be realized with taking into consideration not only a variation of the resistance element but also a variation of the capacitive load by employing the capacitive load connected to the source line as the capacitance element in the integrator circuit.

In accordance with the 46th aspect of the invention, there is provided a driver circuit as in the 15th aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit and a capacitance value of the capacitance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 45th aspect of the invention can be attained.

In accordance with the 47th aspect of the invention, there is provided a driver circuit as in the 17th aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit and a capacitance value of the capacitance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed

together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 45th aspect of the invention can be attained.

In accordance with the 48th aspect of the invention, there is provided a driver circuit as in the 19th aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit and a capacitance value of the capacitance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 45th aspect of the invention can be attained.

In accordance with the 49th aspect of the invention, there is provided a driver circuit as in the 21st aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit and a capacitance value of the capacitance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 45th aspect of the invention can be attained.

In accordance with the 50th aspect of the invention, there is provided a driver circuit as in the 23rd aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit and a capacitance value of the capacitance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 45th aspect of the invention can be attained.

In accordance with the 51st aspect of the invention, there is provided a driver circuit as in the 25th aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit and a capacitance value of the capacitance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 45th aspect of the invention can be attained.

In accordance with the 52nd aspect of the invention, there is provided a driver circuit as in the 27th aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit and a capacitance value of the capacitance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 45th aspect of the invention can be attained.

In accordance with the 53rd aspect of the invention, there is provided a driver circuit as in the 29th aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit and a capacitance value of the capacitance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 45th aspect of the invention can be attained.

In accordance with the 54th aspect of the invention, there is provided a driver circuit as in the 31st aspect of the invention, wherein the first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from the horizontal synchronizing signal, and outputs the first switching signal to the DAC:

the first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, the delay circuit for delaying the horizontal synchronizing signal for a predetermined delay time determined by a resistance value of the resistance element in the integrator circuit and a capacitance value of the capacitance element in the integrator circuit; and

a logic circuit wherein an output from the delay circuit and the horizontal synchronizing signal are ANDed together to output a resultant signal as the first switching signal.

According to the above construction, the same effect as in the 45th aspect of the invention can be attained.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram showing the construction of a liquid crystal display in accordance with Embodiment 1-1 of the present invention.

FIGS. **2**(*a*)–(*b*) are diagrams showing a partial construction of the LCD driver circuit in accordance with Embodiment 1-1 of the present invention.

FIG. **3** is a diagram showing the construction of the LCD driver circuit in accordance with Embodiment 1-1 of the present invention.

FIG. **4** is a diagram showing the construction of the LCD driver circuit in accordance with Embodiment 1-2.

FIG. **5** is a diagram showing the construction of the LCD driver circuit in accordance with Embodiment 1-3.

FIG. **6** is a diagram showing the construction of the LCD driver circuit in accordance with Embodiment 1-4.

FIGS. **7**(*a*)–(*c*) are diagrams to illustrate the normal operation period in Embodiment 2 of the present invention.

FIGS. **8**(*a*)–(*c*) are other diagrams to illustrate the normal operation period in Embodiment 2 of the present invention.

FIG. **9** is a schematic diagram showing the construction of the LCD driver circuit in accordance with Embodiment 2-1 of the present invention.

FIG. **10** is a timing chart of the LCD driver circuit in accordance with Embodiment 2-1 of the present invention.

FIG. **11** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-1 of the present invention.

FIG. **12** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-1 of the present invention.

FIG. **13** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-2 of the present invention.

FIG. **14** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-3 of the present invention.

FIG. **15** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-3 of the present invention.

FIG. **16** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-4 of the present invention.

FIG. **17** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-5 of the present invention.

FIG. **18** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-5 of the present invention.

FIG. **19** is a diagram showing the equivalent circuit of a DAC in the case of the input data being a sixth input data.

FIG. **20** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-6 of the present invention.

FIG. **21** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-6 of the present invention.

FIG. **22** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-7 of the present invention.

FIG. **23** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-7 of the present invention.

FIG. **24** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-8 of the present invention.

FIG. **25** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-8 of the present invention.

FIG. **26** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-9 of the present invention.

FIG. **27** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-9 of the present invention.

FIG. **28** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-10 of the present invention.

FIG. **29** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-10 of the present invention.

FIG. **30** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-11 of the present invention.

FIG. **31** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-11 of the present invention.

FIG. **32** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-12 of the present invention.

FIG. **33** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-12 of the present invention.

FIG. **34** is a schematic diagram showing the construction of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-13 of the present invention.

FIG. **35** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-13 of the present invention.

FIG. **36** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-14 of the present invention.

FIG. **37** is a circuit diagram of a first switching signal generator circuit provided in the LCD driver circuit in accordance with Embodiment 2-14 of the present invention.

FIG. **38** is a timing chart of the first switching signal generator circuit.

FIG. **39** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-14 of the present invention.

FIG. **40** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-15 of the present invention.

FIG. **41** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-15 of the present invention.

FIG. **42** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-16 of the present invention.

FIG. **43** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-16 of the present invention.

FIG. **44** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-17 of the present invention.

FIG. **45** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-17 of the present invention.

FIG. **46** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-18 of the present invention.

FIG. **47** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-18 of the present invention.

FIG. **48** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-19 of the present invention.

FIG. **49** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-19 of the present invention.

FIG. **50** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-20 of the present invention.

FIG. **51** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-20 of the present invention.

FIG. **52** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-21 of the present invention.

FIG. **53** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-21 of the present invention.

FIG. **54** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-22 of the present invention.

FIG. **55** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-22 of the present invention.

FIG. **56** is a circuit diagram of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-23 of the present invention.

FIG. **57** is a timing chart of a DAC incorporated in the LCD driver circuit in accordance with Embodiment 2-23 of the present invention.

FIG. **58** is a circuit diagram showing the construction of a first switching signal generator circuit **105B** in accordance with Embodiment 2-24 of the present invention.

FIG. **59** is a timing chart of the first switching signal generator **105B**.

FIG. **60** is a circuit diagram showing the construction of a first switching signal generator circuit **105C** in accordance with Embodiment 2-25 of the present invention.

THE BEST MODE FOR CARRYING OUT THE INVENTION

Embodiment 1

(Embodiment 1-1)

With reference to FIGS. **1** to **3**, there is described a driver circuit for an active matrix liquid crystal display (AMLCD) of Embodiment 1-1 hereinafter.

The AMLCD is constructed as shown in FIG. **1**, by stacking up a polarizing filter layer **51**, a glass substrate **52**, a liquid crystal panel PNL, a counter glass substrate **54** where a counter transparent electrode **53** is formed thereon, a polarizing filter layer **55**, and so forth.

In a display region **60** on the glass substrate **52**, there are formed source lines SL disposed parallel to each other whose number corresponds with the number of the pixels on a horizontal line, and gate lines GL disposed in the direction perpendicular to the source lines SL, whose number corresponds with the number of the pixels on a vertical line, with an insulation layer (not shown) disposed between the source lines SL and gate lines GL. In each intersectional position of source lines SL and gate lines GL, there are formed a pixel switching transistor **61** and a pixel electrode **62**.

On the glass substrate **52**, there are also formed driver circuits **71** for applying driving voltages to the source lines SL, including digital-to-analog converter circuits (DACs) therein, and vertical scanning switches GSW for selectively applying voltages Vg to the gate lines GL. It is noted that the driver circuits **71** may be provided corresponding to each set of a certain predetermined number of source lines selectively connected by switches, but for clarity of illustration, the description hereinafter assumes that a driver circuit **71** is provided corresponding to each source line SL, and the following description will be concerned with one driver circuit **71** corresponding to one source line SL.

Resistance elements comprised in the DACs in the aforementioned driver circuit **71**, as well as the pixel switching transistors **61**, are formed by polycrystalline silicon (p-Si) formed on the glass substrate **52**, as shown in FIG. **2**.

FIG. **2**(*a*) shows a circuit diagram of the switching elements and resistance elements composing the DAC in the driver circuit **71**, and FIG. **2**(*b*) shows a wiring pattern of the switching elements and resistance elements shown in FIG. **2**(*a*). It is to be noted that only one of the resistance elements composing the DAC and one switching element connected to this resistance element are shown in FIG. **2**(*a*) so that the characteristics of an LCD driver circuit of the present invention will be more clearly understood.

A resistance element R shown in FIG. **2**(*b*) is formed in an n+ layer of p-Si on an array substrate of the LCD. A switching element Tr connected to the resistance element R is an n-channel transistor. In FIG. **2**(*b*), there are also shown a source terminal S of the switching element Tr, a drain terminal D of the switching element Tr, a gate terminal G of the switching element Tr, a gate electrode **1** composed of aluminum and the like, and an output terminal **2**. There are also shown a source region **3** and a drain region **4** both formed in n+ layer of p-Si, and a channel region **5** disposed between the source region **3** and the drain region **4**.

The source terminal S is connected to the source region **3** via a contact region Rcs disposed therebetween. The gate terminal G is connected to the gate electrode **1** via a contact region Rcg disposed therebetween. The drain terminal D is commonly connected to the drain region **4** and the resistance element R via a contact region Rcd disposed therebetween. The output terminal **2** is connected to the resistance element R via a contact region Rcr disposed therebetween. Each of these contact regions Rcs, Rcg, Rcd, and Rcr functions as a

resistance element inversely proportional to each of the areas thereof. Consequently, an equivalent circuit to the wiring pattern shown in FIG. 2(*b*) will be the circuit diagram as shown in FIG. 2(*a*).

The shape of n+ layer of p-Si that functions as a resistance element R is determined according to the following grounds. The resistance value r of the resistance element R is proportional to the length L of the n+ layer of p-Si, and inversely proportional to the width W. Accordingly, the resistance value r is: $r=\rho \times L/W$ where p is a sheet resistance of n+ layer of p-Si. For example, assuming that a resistance element R with r=10 kΩ is to be formed, the required element is realized by setting L/W=5 when a sheet resistance ρ=2 kΩ/□, for example by setting L=100 μm and W=20 μm. Thus, a desired resistance value is obtained by arbitrarily selecting combinations of the length L and width W of an n+ layer. Hence, it is made possible to form on an array substrate a circuit wherein a resistance element R formed on an n+ layer of p-Si is connected to a switching element Tr.

A digital-to-analog converter circuit (DAC) in the present invention is constructed by using a plurality of the aforementioned resistors R and switching elements Tr and connecting them in a predetermined wiring pattern. By incorporating DACs in an array substrate as described above, it is made possible to eliminate drier ICs from the components of an LCD, and thereby to reduce the manufacturing cost. It is also thereby made possible to eliminate the step of mounting the driver ICs on the array substrate and to reduce the thickness of an LCD.

FIG. **3** shows a specific circuit construction of a driver circuit for an LCD. A DAC **10** comprised in this driver circuit is composed of an R-2R ladder type DAC. The DAC **10** comprises resistance elements **Rn0**, **Rn1**, **Rn2**, **Rn3**, **Rn00**, **Rn01**, **Rn12**, and **Rn23**, and switching circuits **15***a* to **15***d* provided corresponding to each bit of digital input data so as to selectively switch a high voltage power supply VH and a low voltage power supply VL. Each of the resistance elements **Rn0**, **Rn1**, **Rn2**, **Rn3**, **Rn00**, **Rn01**, **Rn12**, and **Rn23** is formed in the n+ layer of p-Si. All the resistance elements **Rn0**, **Rn1**, **Rn2**, and **Rn3** have the same resistance value, and likewise, **Rn00**, **Rn01**, **Rn12**, and **Rn23** have the same resistance value; on the other hand, the resistance value of the resistance elements **Rn00**, **Rn0**, **Rn1**, **Rn2**, and **Rn3** are twice as large as the resistance value of the resistance elements **Rn01**, **Rn12**, and **Rn23**. That is, when the resistance value of the resistance elements **Rn01**, **Rn12**, **Rn23** is represented by **r1**, the resistance value of the resistance elements **Rn00**, **Rn0**, **Rn1**, **Rn2**, **Rn3** is represented by 2×**r1**.

The switching circuit **15***a* connected to the resistance element **Rn0** is composed of a switching element **Tr0***a* and **Tr0***b*, the switching circuit **15***b* connected to the resistance element Rn1 is composed of a switching element Tr1*a* and Tr1*b*, the switching circuit **15***c* connected to the resistance element Rn2 is composed of a switching element Tr2*a* and Tr2*b*, and the switching circuit **15***d* connected to the resistance element **Rn3** is composed of a switching element Tr3*a* and Tr3*b*. These eight switching elements **Tr0***a* through Tr3*b* are an n-channel transistor formed on the array substrate.

Each of the digital input data bits **D0**, **D0***; **D1**, **D1***; **D2**, **D2***; and **D3**, **D3*** is fed to each gate of the aforementioned switching elements **Tr0***a*, **Tr0***b*; Tr1*a*, Tr1*b*; Tr2*a*, Tr2*b*; and Tr3*a*, Tr3*b* respectively. The bits **D0** to **D3** represent each bit of 4 bit digital input data signals, and the bits **D0*** to **D3*** respectively represent the inverted ones of each bit **D0** to **D3**. The bits **D0** and **D0*** function as a switching signal for the switching elements **Tr0***a* and **Tr0***b* respectively, the bits **D1** and **D1*** function as a switching signal for the switching elements Tr1*a* and Tr1*b* respectively, the bits **D2** and **D2*** function as a switching signal for the switching elements Tr2*a* and Tr2*b* respectively, and the bits **D3** and **D3*** function as a switching signal for the switching elements Tr3*a* and Tr3*b* respectively. For example, the switching element **Tr0***a* is turned ON when the bit **D0** is a logic "1", and turned OFF when the bit **D0** is a logic "0".

Although this embodiment shows an example in the case of the 4-bit digital input signals, the present invention can be practiced for other multiple-bit digital input signals by employing a plurality of the above structures.

A signal amplifier element **11** is composed of an n-channel transistor formed on the array substrate. The signal amplifier element **11** may be composed of a p-channel transistor, or a combination of an n-channel transistor and a p-channel transistor. The signal amplifier element **11** is, specifically, achieved by an operational amplifier (op-amp) which functions as a voltage follower. The signal amplifier element **11** may be composed of a source follower type n-channel transistor or a source follower type p-channel transistor in place of the op-amp which functions as a voltage follower. An analog output voltage from the DAC **10** drives a source line SL for liquid crystal elements with its output current being amplified by the signal amplifier element **11**, while the output voltage amplification ratio is held at 1. In addition, this signal amplifier element **11** has an impedance conversion function, so that it is capable of driving a source line SL having a large capacitive load quickly with the output capability of the DAC being kept small. Moreover, by forming the signal amplifier element **11** on the array substrate, it is made possible to eliminate the signal amplifier elements from the component items of an LCD, and thereby to reduce the manufacturing cost when compared with the case where the signal amplifier elements as individual components are mounted onto the array substrate. It is also thereby made possible to eliminate the step of mounting the signal amplifier elements on the array substrate.

The total area of the resistance elements used in the DAC **10** is as follows. Assuming that the resistance value **r1** of the reference resistance element **Rn01** is 10 kΩ, that the sheet resistance ρ of n+ layer of p-Si is 2 kΩ/□, and that the width of n+ layer of p-Si is 20 μm, a length **L1** of each n+ layer of p-Si which functions as the resistance elements **Rn01**, **Rn12**, and **Rn23** results in L1=100 μm, and a length L2 of each n+layer of p-Si which functions as the resistance elements **Rn00**, **Rn0**, **Rn1**, **Rn2**, and **Rn3** results in L2=200 μm. Accordingly, the total area of the resistance elements used in the DAC **10** results in 0.026 mm^2, excluding the pattern clearance areas (the gap areas between each n+ layer a resistance element).

As described above, by employing an R-2R ladder type DAC for the DAC in the present invention, it is made possible to construct a DAC with two types of resistance elements, one with the resistance value **r1** and the other with the resistance value 2×**r1**. Thereby, when compared with the case where a DAC having a construction other than the R-2R ladder type is employed to obtain similar output voltage characteristics, the total area required for resistance elements in a DAC can be substantially reduced, and moreover, the scale of a circuit required for decoding digital data can be reduced.

Now, there is described a summary of the operation of the DAC having the above-described construction. Assuming that the digital input data bits **D0**, **D1**, and **D2** are a logic "1", and that the digital input data bit **D3** is logic "0", the bits **D0***, **D1***, and **D2*** are logic "0", and the bit **D3** is a logic

"1". Therefore, the switching element Tr0*a* is turned to ON state and the Tr0*b* is turned to OFF state, and thereby, of the power supply voltages VL and VH, the voltage VH is applied to the resistance element Rn0 via the switching element Tr0*a*. Likewise, the power supply voltage VH is applied to the resistance element Rn2 via the switching element Tr1*a* and to the resistance element Rn2 via the switching element Tr2*a*. On the other hand, the switching element Tr3*a* is turned to OFF state and the switching element Tr3*b* is ON state, of the power supply voltages VL and VH, the voltage VL is applied to the resistance element Rn3 via the switching element Tr3*a*. Thus, corresponding to the each digital input data bits D0 to D3 and each inverted digital input data bits D0* to D3*, one voltage of the power supply voltages VL or VH is selected and applied to the resistance elements Rn0, R1, Rn2, and Rn3 via the switching elements Tr0*a* to Tr3*a* or the switching elements Tr0*b* to Tr3*b*. The former resistance elements R00, Rn0, Rn1, Rn2 and Rn3 have twice as large resistance value as the latter resistance elements R01, R12, and R23, and therefore the voltage at a connecting terminal **24** is represented by VL+(VH−VL)(D0+2×D1+4×D2+8×D3)/8. Thus, 16 types of linear output voltages corresponding to the digital input data D0 to D3 and D0* to D3* are obtained.

(Embodiment 1-2)

FIG. **4** shows the construction of a driver circuit according to Embodiment 1-2. In this driver circuit according to Embodiment 1-2, a voltage potentiometer type DAC is used in place of the R-2R ladder type employed in Embodiment 1-1. As for the digital input signal, it consists of three bits, D0, D1, and D2. In a DAC **28** of this embodiment, there are formed resistance elements R1 to R7 connected in series between a high voltage power supply VH and a low voltage power supply VL, switching elements Tr0 to Tr7 connected between connecting terminals C0 to C7 of the resistance elements R1 to R7 and an output terminal, and a selective circuit **30** relating to the switching elements Tr0 to Tr7. The selective circuit **30** alternatively selects one of the connecting terminals C0 to C7 of the resistance elements R1 to R7 in response to the digital input signals D0 to D2. This selective circuit **30** is composed of three-input gate circuits B0 to B7 for selecting the switching states of the switching elements Tr0 to Tr7. The gate circuits B0 to B7 are composed of n-channel transistors. The gate circuits B0 to B7 may be composed of p-channel transistors or combinations of n-channel transistors and p-channel transistors.

In a DAC having the above-described construction, when the digital input signals D1 and D2 are logic "0" and the digital input signal D0 is a logic "1", the outputs of the gate circuits B2 to B7 and B0 are made to be low level, and the output of the gate circuit B1 is made to be high level.

As a result, the switching elements Tr2 to Tr7 and Tr0 is turned to ON state and the switching element Tr1 is turned to OFF state. Thereby, the voltage of the connecting terminal C1, which is supplied from a high voltage power supply VH and dropped by the resistance elements R7 to R2, is applied to a signal amplifier element **11** as an output voltage. Thus, one of the connecting terminals C0 to C7 is selected corresponding to the switching states of the switching elements Tr0 to Tr7, and one of the voltages divided by the resistance elements R1 to R7 and is picked out as the output voltage corresponding to the selected connecting terminal. Consequently, the output voltage is weighted by a resistance value of each of the resistance elements R0 to R7. Therefore, a linear output voltage characteristic can be obtained by setting the resistance values of the resistance elements R1 to R7 at the same value, and conversely, a desired curve in the output voltage characteristic can be obtained by arbitrarily setting the resistance value ratio of the resistance elements R1 to R7 at a certain ratio.

In addition, since this embodiment has a construction in which only the resistance elements are connected in series between the power supplies, it is made possible to obtain such output voltage characteristics as designed using only resistance elements in the actual circuit. The reason is as follows. In the actual designing of circuits, if the DAC has a construction as described in FIG. **3** or other constructions, an ON resistance of switching elements should be taken into consideration in determining the output voltage. Conversely, in this embodiment, as apparent in FIG. **4**, if the current flowing through switching elements are small, i.e., the input impedance to the switching element **11** is large, a voltage drop and current diversion by the switching element can be prevented, and therefore the output voltage is determined by only dividing voltages by the resistance elements.

It is therefore made unnecessary to take into consideration ON resistances of the switching elements, and possible to determine the output voltage by only the resistance elements.

(Embodiment 1-3)

Now with reference to FIG. **5**, the construction of a driver circuit of Embodiment 1-3 is detailed below. This driver circuit of Embodiment 1-3 has a similar construction to the driver circuit described in Embodiment 1-1, and the same reference characters are used for the corresponding parts. Embodiment 1-3 differs from Embodiment 1-1 in that the signal amplifier element **11** is not employed in the circuit construction. In this embodiment, the analog output voltage from the DAC **10** is directly outputted to the source line SL without amplified, and thus it directly drives liquid crystal elements. In order to make this possible, each resistance value of the resistance elements Rn0 to Rn3, Rn00, Rn01, Rn12, and Rn23 as well as each voltage of the power supplies VG and VD are determined so that a driving voltage required for driving liquid crystal elements can be obtained by the output voltage from the DAC **10**.

According to this construction, wherein the signal amplifier element **11** is eliminated, the whole circuit area can be made smaller corresponding to the circuit area to be occupied by the signal amplifier element **11** when compared with the case where the signal amplifier element **11** is formed on the array substrate, and moreover the power consumption of the signal amplifier element **11** is eliminated.

It is noted, just for reference, that in the case where the signal amplifier element **11** is employed, the signal amplifier element **11** is required to have a high performance since the output voltage characteristics is very much dependent on the performance of the signal amplifier element **11**. However, in the present state of art, p-Si transistors are inferior to crystalline silicon transistors in their transistor performance. Hence, in the aforementioned construction of FIG. **3**, in which the signal amplifier element **11** is formed on the array substrate, a large scale circuit is inevitably required so as to obtain an output voltage characteristics and output current characteristic with high precision, and therefore a desired precision may not be able to be obtained within a limited area on the array substrate. In this respect, according to the construction of FIG. **5**, in which the signal amplifier element **11** is eliminated, the reliability of an LCD driver circuit is further improved, and the driver circuit can be suitably used for the case where a highly-precise output voltage characteristic is required. It is to be noted that in this embodiment, there has been described a driver circuit having a construction in which the signal amplifier element **11** is eliminated

from the driver circuit of FIG. 3, but this embodiment may also be achieved by employing a construction in which the signal amplifier element 11 is eliminated from the aforementioned driver circuit of FIG. 4.

(Embodiment 1-4)

FIG. 6 depicts the construction of a driver circuit of Embodiment 1-4. A DAC 40 of this embodiment comprises a first DAC section 41 operated in response to two more significant bits D3 and D2 of digital inputs D0 to D3 and a second DAC section 42 operated in response to two lesser significant bits D1 and D0. In the first DAC section 41, resistance elements R4 to R7 are connected in series between a high voltage power supply VH and a low voltage power supply VL, which are the references for an output voltage, switching elements Tr4H to Tr7H are connected between a terminal VH2 and each high voltage terminal of the connecting terminals of the resistance elements R4 to R7, and switching elements Tr4L to Tr7L are connected between a terminal VL and each low voltage terminal of the connecting terminals of the resistance elements R4 to R7. A selective circuit 44 is provided in relation to the switching elements Tr4H to Tr7H. The selective circuit 44 alternatively selects the connecting terminals of the resistance elements R4*n* to R7*n* in response to the digital input D2 and D3. This selective circuit 44 is composed of two-input gate circuits VSL4 to VSL7 for selecting the switching states of the switching elements Tr4H to Tr7H and Tr4L to Tr7L.

The second DAC section 42, which is an R-2R ladder type DAC, comprises resistance elements R00, R01, R0, and R1, and switching elements Tr0L, Tr0H, Tr1L, and Tr1H. It also has as its reference power supplies the terminals VH2 and VL2 which are the output voltages from the first DAC section 41. It outputs digital-to-analog converted signals to an output terminal 300 in response to digital input signals D0 and D1. The resistance value of the resistance element R01 is r1, and those of the resistance elements R00, R0, and R1 are twice as large as r1.

There is now described an outline of the operation of the DAC having the above construction. The first DAC section 41 basically operates according to the same manner as in the embodiment shown in FIG. 4. The digital inputs D3 and D2 are decoded by the selective circuit 44, then the potentials at both connecting terminals of one of the resistance elements R4*n* to R7*n* are alternatively selected, then the selected connecting terminal with higher potential is connected to the terminal VH2 by switching one of the switching elements Tr4H to Tr7H, and the selected connecting terminal with lower potential is connected to the terminal VL2 by switching one of the switching elements Tr4L to Tr7L corresponding to the switching element switched on the higher potential side. A desired intermediate potential between the high voltage power supply VH and the low voltage power supply VL is thus generated between the terminal VH2 and the terminal VL2.

The second DAC section 42 basically operates according to the same manner as in the embodiment shown in FIG. 3. Using as a reference voltage the terminal VH2 and the terminal VL2 connected to the first DAC section, the switching elements Tr0L, Tr0H, Tr1L, and Tr1H are switched in response to the digital input signals D0 and D1, and one of the four potentials equally divided between the terminal VH2 and VL2 is alternatively selected and outputted to the terminal 300.

The driver circuit according to the above construction can avoid a relatively large output voltage error caused by the errors of ON resistance of the switching element corresponding to the more significant bits in the embodiment shown in FIG. 3, and moreover, it can obtain the output characteristic with a desired step-like line within the range of the more significant bits. Furthermore, in the driver circuit according to the above construction, by employing the above construction of the lesser significant bit section, the scale of the selective circuit therein can be reduced, and in the case of the lesser significant bits being three or more bits, the number of the resistance elements can be also reduced when compared with the construction shown in FIG. 4.

It is understood that although the potentials of both connecting terminals of one resistance element are selected for the terminals VH2 and VL2 in this embodiment, there is no problem at all if one connecting terminal is selected from one of the resistance elements and the other connecting terminal from another resistance element.

In the embodiments described thus far, although the resistance elements are formed in the n+ layer of p-Si, the present invention is not limited thereto, and the resistance elements may be formed from an n− layer of p-Si, p+ layer, or p− layer of p-Si, or any of an n+ layer, n− layer, p+ layer, or p− layer of amorphous silicon (a-Si). The resistance elements may also be formed from a combination of an n+ layer, an n− layer, a p+ layer, and a p− layer of p-Si or a-Si. In other words, the resistance elements in the present invention should be formed by a non-monocrystalline semiconductor layer containing an impurity. Among them, an n− layer and a p− layer are particularly advantageous in that they are capable of making the circuit area smaller since an impurity layer with low concentration (n− layer and p− layer) has higher resistance than an impurity layer with high concentration (n+ layer and p+ layer). In addition, in view of designing a circuit as a whole, at the same time with taking into account the view of reducing the circuit, a variety of wiring patterns suitable for various specifications can be formed by arbitrarily selecting any of the n+, n−, p+, and p− layer of p-Si or a-Si, and thus freedom in circuit designing can be increased.

It is also to be understood that although the switching elements composing the DAC are n-channel transistors in the above-described embodiments, the switching elements may be p-channel transistors or combinations of n-channel transistors and p-channel transistors.

Further, although the signal amplifier element 11 is formed on the array substrate in the above-described embodiments, a signal amplifier element as an individual component may be mounted on the array substrate.

Embodiment 2

Embodiment 2 herein has achieved reduced power consumption in an LCD driver circuit by creating a low power period, which is a period except a normal operation period of a DAC, and reducing an electric current consumed in the DAC during the low power period. The normal operation period herein is defined as the following (1) or (2). (1) In the case where the time at which a gate pulse is provided and the time of the change of the output voltage from a driver circuit are almost simultaneous, a normal operation period is a period during which the potential of a pixel electrode reaches a desired potential (i.e., a pixel electrode writing period). (2) In the case where a source line reaches a desired potential by the change of the output voltage from a driver circuit and thereafter a gate pulse is provided, a normal operation period is a period during which the potential of a source line reaches a desired potential (i.e., a source line writing period).

The source line writing period means a period required for completely changing the potentials of all the capacitive

loads connected to a source line into a desired potential by the output voltage from a DAC. The pixel electrode writing period means a period required for, first, switching a pixel transistor ON by a scan pulse from a gate line, then establishing a continuity between the pixel electrode and a source line, and thereafter completely changing the potential of the pixel electrode into a desired potential.

With reference to FIG. **7**, in the case of the aforementioned (1), when a gate pulse has the waveform shown in FIG. **7**(*a*) and an output voltage from a driver circuit has the waveform shown in FIG. **7**(*b*), a source line potential and a pixel electrode potential are both charged by applying the output voltage from the driver circuit as shown in FIG. **7**(*c*). The source line potential reaches a desired potential at a time t1 and the pixel electrode potential reaches a desired potential at a time t2. In such a charging operation, a source line writing period is from the time at which the output voltage from the driver circuit is applied, to the time t1, and a pixel electrode writing period is from the time at which the output voltage from the driver circuit is applied, to the time t2. In this case, a normal operation period T1 is a period during which a pixel electrode reaches a desired potential (a pixel electrode writing period).

In the case of the aforementioned (2), when a gate pulse has the waveform shown in FIG. **8**(*a*) and an output voltage from a driver circuit has the waveform shown in FIG. **8**(*b*), a source line potential is charged and it reaches a desired potential at a time t4, as shown in FIG. **8**(*c*). In this case, a pixel electrode potential rises by being charged from a time t5 and reaches a desired potential at a time t6. In this case, of FIG. **8**, a normal operation period T1 is a period from a time t3 to the time t4, during which a source line potential reaches a desired potential (a source line writing period).

It is to be noted that the driver circuits of the embodiments which will be described hereinafter are, as well as the driver circuits of Embodiment 1 described hereinbefore, so-called integrated type driver circuits integrally formed on an array substrate of an LCD, and therefore the resistance elements composing the DACs therein are also formed by the semiconductor layers formed on the array substrate. Now, with reference to the figures, there is detailed EMBODIMENT 2 below.

(Embodiment 2-1)

FIG. **9** shows the entire construction of an LCD driver circuit of Embodiment 2-1. A liquid crystal panel shown as an example of Embodiment 2-1 has (n) number of source lines and (m) number of gate lines, and three-bit data is inputted therein. A driver circuit **108** is an integrated type driver circuit integrally formed on an array substrate **100**. The driver circuit **108** basically comprises a source line timing controller **101**, (n) pieces of first latch circuits **102** for latching video signals, (n) pieces of second latch circuits **103** for latching the outputs from the first latch circuits **102**, (n) pieces of DACs **104**, a first switching signal generator circuit **105** for generating a first switching signal P (see FIG. **12**) for selectively switching two modes, one of the modes being a normal operation period T1 and the other mode being a remaining period T2 (hereinafter referred to as a 'low power period T2'), which is the remaining period of one horizontal synchronizing period after the normal operation period T1 is excluded, and a gate line timing controller **106** for controlling outputs of scanning pulses for GL1 to GL(m).

FIG. **10** is a timing chart showing the operation of the driver circuit. The source line timing controller **101** successively outputs latch pulses LP1 to LP(n) to the first latch circuits **102** according to dot clock signals. A three-bit serial digital video signal DI is thereby latched by each first latch circuit **102** successively. When the digital data for one horizontal line is thus latched by each of the first latch circuits **102**, a latch pulse LP is outputted from the source line timing controller **101** to each second latch circuit **103**, and thereby the digital data for one horizontal line is latched to each of the second latch circuits **103**. The digital data latched by each second latch circuit is fed to the DAC **104** and a driving voltage corresponding to the input digital data is outputted to each source line SL1 to SL(n). Meanwhile, synchronized with such driving voltages outputted to the source lines SL1 to SL(n), a scanning pulse is outputted from the gate line timing controller **106** to a gate line GL1 and thereby the pixel transistors are turned ON, and thus the driving voltages are written into the liquid crystal layer. Thereafter, the same operation is repeated until it reaches the (m)-st line, and a scanning for one field is thereby completed. Hence, an image of the video signals for one field is displayed.

It is to be noted that the data DL latched by each of the first latch circuits **102** is updated when each latch pulse LP1 to LP(n) is inputted. This updating of the latched data DL is carried out once in each horizontal synchronizing period for each first latch circuit **102**. In a blanking period, the latest data of input video signals for one line is stored in the first latch circuits **102**. During this blanking period, a common latch pulse LP is inputted to the second latch circuits **103**, and the data DLL is updated so that the data DLL becomes the latest data for one line. The input data to the DACs **104** for driving the source lines are the data DLL latched in the latch circuits **103**. The data are updated coinciding with the time at which the latch pulse LP is inputted to each second latch circuit **103**, and the same data are fed into the DACs **104** throughout one horizontal synchronizing period.

In this embodiment, a normal operation period T1 is a portion of one horizontal synchronizing period T, and a low power period T2 is defined as a remaining period excluding the normal operation period T1 from one horizontal synchronizing period T. This embodiment is characterized by reducing the power consumption of the DACs **104** in this low power period T2. More specifically, in prior arts, one entire horizontal synchronizing period has been the normal operation period. In this embodiment, however, the normal operation period T1 is limited to the period during which it is essential to keep applying a driving voltage to source lines, and it is characterized in that the power consumption in the resistance elements in the DACs **104** is reduced in the low power period T2. This embodiment thus achieves the reduction in power consumption when compared with prior arts wherein DACs continue the normal operation throughout one entire horizontal synchronizing period T.

FIG. **11** is a diagram showing the specific circuit construction of such a DAC, and FIG. **12** is a timing chart showing the operation of the DAC. The DAC **104** is a voltage potentiometer DAC. This DAC **104** comprises a series circuit **13** in which a plurality of resistance elements **112***a* to **112***g* are connected in series, second switches **114***a* to **114***h* for selectively outputting the voltages divided by the resistance elements **112***a* to **112***g* to an output terminal **300** of the DAC, a signal amplifier element **11** connected between the second switches **114***a* to **114***h* and an output terminal **116** of the driver circuit, an output switch **119** connected between the signal amplifier element **11** and the output terminal **116**, and a decoder **111** for decoding three-bit digital input signals D0, D1, and D2 into eight-bit digital signals DD1 to DD8.

One end of the aforementioned series circuit **113** is connected to a power supply terminal **118***a* of a high voltage

power supply VH with a first switch **117** interposed therebetween, and the other end is connected to a power supply terminal **118***b* of a low voltage power supply VL. The second switches **114***a* to **114***h* are composed of an n-channel TFT, and the first switch **117** and the output switch **119** are composed of a p-channel TFT.

The first switching signal generator circuit **105** generates a first switching signal P as shown in FIG. **11** from a horizontal synchronizing signal inputted therein. The first switching signal P comprises a high-level period and low-level period, and is so constituted that the low-level period becomes identical to the normal operation period T1 and the high-level period becomes identical to the low power period T2.

The first switching signal generator circuit **105** outputs the first switching signal P to the first switch **117** and the output switch **119**. The first switch **117** is turned to OFF state in the case of the first switching signal P being high-level, and turned to ON state in the case of the first switching signal P being low-level. As a result, during the normal operation period T1, a power supply voltage (VH−VL) is applied to the resistance elements in the DAC **104**, while during the low power period T2, the power supply voltage applied to the DAC **104** is "0".

The output terminal **116** is connected to a capacitive load **120**. Among the capacitive loads of a source line are 1) a capacitance generated in a liquid crystal layer and an insulation layer whose electrodes are an entire source line and a counter substrate, 2) a capacitance generated in an insulation layer whose electrodes are a source line and a gate line at the intersection of the lines, 3) a capacitance generated in an insulation layer whose electrodes are a source line and a pixel electrode terminal parallel to the source line, and 4) a capacitance retained by a pixel transistor at the intersection of a source line and a gate line. The total sum of these capacitive loads 1) to 4), is equivalent to the capacitive load **120**.

Referring now to the timing chart of FIG. **12**, there is explained the power reduction system of a DAC **104** having the above-described construction. During the normal operation period Ti, the first switching signal P is low-level and thereby the first switch **117** is turned to ON state. As a result, the resistance elements of the DAC **104** are connected to the power supply terminal **118***a* and the power supply terminal **118***b*, and the electric current I flowing in the resistance elements **112***a* to **112***g* becomes I1 in the following Equation (1), and at this point, the electric power W consumed in the resistance elements **112***a* to **112***g* becomes W1 in the following Equation (2). During this normal operation period T1, the output switch is kept ON state, and thereby the output from the signal amplifier element **11** is fed to the output terminal **116**. The voltage at the output terminal **116** is determined by one of the second switches **114***a* to **114***h* controlled by the digital inputs DD1 to DD8, and one voltage between the voltage VH and the voltage VL, which is the area shown by slanted lines in FIG. **10**, is outputted as a driving voltage.

$$I1=(VH-VL)/\Sigma Rn \qquad \text{Equation (1)}$$

$$W1=(VH-VL)^2/\Sigma Rn \qquad \text{Equation (2)}$$

During the low power period T2, the first switch **117** is turned to OFF state. The electric current I flowing in the resistance elements **112***a* to **112***g* thereby becomes "0", and the electric power W consumed in the resistance elements **112***a* to **112***g* also becomes "0". Hence, the power consumption can be reduced during the low power period T2. The voltage at the output terminal **300** is indefinite. In addition, during the low power period T2, since the output switch **119** is turned to OFF state, the potential at the output terminal **116** is retained by the capacitive load **120**. Therefore, the low power period is not limited to the blanking period in one horizontal synchronizing period T, but can include a period in which the period necessary to change the voltage of the capacitive load **120** is excluded from one horizontal synchronizing period.

In the low power period T2, in the case where the pixel transistor is made OFF, the electric charge stored in the liquid crystal layer is, primarily, retained. Therefore, there is theoretically no need to hold the voltage of the capacitive load **120** by making the output switch **119** OFF. However, in practice, it is unable to completely cut off the liquid crystal layer and the source lines, and for that reason, there arises a need to retain the voltage of the capacitive load **120** by switching off the output switch **119**. If the signal amplifier **11** has such a construction that the output impedance becomes high when the driving power of the signal amplifier element **11** is cut off, the output switch **119** can be omitted and the voltage retention of the capacitive load **120** can be carried out by cutting off the driving power of the signal amplifier element **11**. However, if the signal amplifier **11** does not have such a construction that the output impedance becomes high when the driving power of the signal amplifier element **11** is cut off, it is necessary that a voltage variation of the capacitive load **120** be prevented by the output switch **119**.

In this embodiment, the electric current I can also be made "0", by short-circuiting the power supply terminal **118***a* and the power supply terminal **118***b*. In this case, a rush current is generated immediately after the short circuit and some electric power is generated. However, if the effect of power reduction by creating a low power period outweighs even with taking into account the power loss by the rush current, it is possible to attain the reduction of power consumption by short-circuiting the power supplies.

It is noted that although the first switch **117** is connected between the resistance element **112***g* and the power supply terminal **118***a* in the above example, but it may be connected between the resistance element **112***a* and the power supply terminal **118***b*.

(Embodiment 2-2)

FIG. **13** shows the construction of the DAC integrated in a driver circuit of the embodiment. This Embodiment 2-2 has a similar construction to the driver circuit of Embodiment 2-1, and the same reference characters are used for the corresponding parts. For this Embodiment 2-2, the signal amplifier **11** and the output **119**, both used in Embodiment 2-1, are eliminated, and instead, a storage circuit **121**A and a switch **121** are provided. In the storage circuit **121**A, a data in which digital signals DD1 to DD8 are all fixed to be logic "0" is stored. The switch **121** is responsive to the first switching signal P, and during the normal operation period T1, it feeds the digital data DD1 to DD8 to the second switches **114***a* to **114***h*, and during the low power period T2, it feeds the fixed data from the storage circuit **121**A to the second switches **114***a* to **114***h* in response to the first switching signal P. As a result, during the normal operation period T1, the second switches **114***a* to **114***h* are controlled by the digital data DD1 to DD8 from the decoder **111**, and a desired driving voltage is thereby obtained. During the low power period T2, all the second switches **114***a* to **114***h* are turned to OFF by the fixed data, resulting in an output impedance of the DAC being a high impedance, and therefore the potential of the capacitive load **120** is retained. The above-described construction, wherein the second switches

114*a* to 114*h* are provided in place of the output switch 119 and have the function of the output switch 119, is also capable of preventing a potential variation of the capacitive load 120 during the low power period T2.

(Embodiment 2-3)

FIG. 14 is a diagram showing the construction of the DAC integrated in a driver circuit of Embodiment 2-3, and FIG. 15 is a timing chart thereof. This Embodiment 2-3 has a similar construction to Embodiment 2-1, and the same reference characters are used for the corresponding parts. For this Embodiment 2-3, a third switch 117A is employed in place of the first switch 117 used in Embodiment 2-1. This third switch 117A is composed of an n-channel TFT and a p-channel TFT, and it is a switch for selecting one power supply from a power supply terminal 118*a* of a first high voltage power supply VHH and a power supply terminal 118*c* of a second high voltage power supply VHL having a lower voltage level than the first high voltage power supply VHH. The first switching signal P is fed to this third switch 117A, and the third switch 117A is so constructed that it is switched to the power supply terminal 118*c* when the first switching signal P is high-level and switched to the power supply terminal 118*a* when the first switching signal P is low-level.

Now referring to the timing chart of FIG. 15, there is explained the power saving system of the DAC having the aforementioned construction. During the normal operation period T1 of the DAC, the first switching signal P is low-level, and thereby the resistance elements in the DAC are connected to the power supply terminal 118*a* and the power supply terminal 118*b*. In this case, the electric current I flowing in the resistance elements 112*a* to 112*g* becomes I1 shown in the above Equation (1), and the electric power W consumed in these resistance elements becomes W1 shown in the above Equation (2).

During the normal operation period T1, the voltage of the output terminal 116 is connected to one of the second switches 114*a* to 114*h* controlled by the digital input data DD1 to DD8, and one of the voltages between the voltage VL and the voltage VHH is thereby outputted.

During the low power period T2, the first switching signal P is made to be high-level, and thereby the third switch 117A is switched to the power supply terminal 118*c*. As a result, the power supply terminal connected to the resistance element 112*g* is switched from the terminal 118*a* to the terminal 118*c*. Therefore, the electric current I flowing in the resistance elements 112*a* to 112*g* becomes I2 shown in the following Equation (3), and the electric power W consumed in the resistance elements 112*a* to 112*g* accordingly becomes W2 shown in the following Equation (4). Hence, the reduction in power consumption during the low power period T2 can be achieved.

$$I2=(VHL-VL)/\Sigma Rn \quad \text{Equation (3)}$$

$$W2=(VHL-VL)^2/\Sigma Rn \quad \text{Equation (4)}$$

Furthermore, during the low power period T2, since the output switch 119 is turned OFF, the potential of the output terminal 116 is retained by the capacitive load 120. Therefore, the low power period is not limited to the blanking period in one horizontal synchronizing period T, but can include a period in which the period necessary to change the voltage of the capacitive load 120 is excluded from one horizontal synchronizing period.

Additionally, during the low power period T2, the voltage of the output terminal 300 results in one of the voltages between VL and VHL. Further, the potentials at each point in the DAC become definite. Therefore, Embodiment 2-3 exhibits such excellent effects that it can reduce a sudden increase of a power supply current in re-throwing the power supply voltage and signal noises resulting from the sudden current increase because it is capable of making definite the potentials at each point in the DAC, although the amount of reduced electric power may not be as much as that of Embodiment 2-1.

(Embodiment 2-4)

FIG. 16 shows the construction of the DAC in Embodiment 2-4. This Embodiment 2-4 has a similar construction to Embodiment 2-3, and the same reference characters are used for the corresponding parts. In this Embodiment 2-4, the signal amplifier element 11 and the output 119, both used in Embodiment 2-3, are eliminated, and instead, a storage circuit 121A and a switch 121 are provided. In the storage circuit 121A, a data where the digital signals DD1 to DD8 are all fixed to be logic "0" is stored. In response to the first switching signal P, during the normal operation period, the switch 121 feeds the digital data DD1 to DD8 to the second switches 114*a* to 114*h*, and during the low power period T2, the switch 121 feeds the fixed data from the storage circuit 121A to the second switches 114*a* to 114*h*. As a result, during the normal operation period T1, the second switches 114*a* to 114*h* are controlled by the digital data DD1 to DD8 from the decoder 111, and a desired driving voltage is thereby obtained. During the low power period T2, all the second switches 114*a* to 114*h* are turned OFF by the fixed data, making the output impedance of the DAC high, and therefore the potential of the capacitive load 120 is retained. The above-described construction, wherein the second switches 114*a* to 114*h* are provided in place of the output switch 119 and have the function of the output switch 119, is also capable of preventing a potential variation of the capacitive load 120 during the low power period T2.

(Embodiment 2-5)

FIG. 17 illustrates the construction of a DAC in Embodiment 2-5, and FIG. 18 is a timing chart thereof. This DAC is an R-2R ladder type digital-to-analog converter circuit employing two types of resistance elements, one with a resistance value R, the other with a resistance value 2R. The DAC comprises resistance elements 130*a*, 130*b*, 130*c*, 130*d*, 131*a*, and 131*b*, fourth switches 132*a*, 132*b*, and 132*c*, and a second switching signal generator circuit 133. The fourth switches 132*a*, 132*b*, and 132*c* are provided for each bit of digital input data and alternatively select one connecting state between a connecting state to a high voltage power supply terminal 118*a* and a connecting state to a low voltage power supply terminal 118*c*. The second switching signal generator circuit 133 outputs a second switching signal for switching each fourth switch 132*a*, 132*b*, and 132*c*.

Each resistance value of the resistance elements 130*a* 130*b*, 130*c*, and 130*d* is 2R, while the resistance value of the resistance elements 131*a* and 131*b* is R. Each of the fourth switches 132*a*, 132*b*, and 132*c* is composed of an n-channel transistor and a p-channel transistor, and serves to determine the output voltage from the DAC.

The second switching signal generator circuit 133 comprises gates 134*a* to 134*c*. The gate 134*a* comprises an inverter 135 and a NOR gate 136. The inverter 135 inverts a digital input D0 and outputs the inverted data. An output signal from the inverter 135 and the first switching signal P are inputted to the NOR gate 136, and the NOR gate 136 outputs the second switching signal to the fourth switch 132*a*. The gate 134*b* has a similar construction to the gate 134*a*, and it comprises an inverter 137 and a NOR gate 138. The inverter 137 inverts a digital input D1 and outputs the

inverted data. An output signal from the inverter **137** and the first switching signal P are inputted to the NOR gate **138**, and the NOR gate **138** outputs the second switching signal to the fourth switch **132***b*. The gate **134***c* comprises an OR gate. A digital input D2 and the first switching signal P are inputted to the gate **134***c* and the gate **134***c* outputs the second switching signal to the fourth switch **132***c*.

Having the construction as described above, an output from the gate **134***a* is, regardless of whether the digital input D0 is logic "1" or logic "0", fixed at a low level during the low power period **T2**, in which the first switching signal is high-level. Likewise, an output from the gate **134***b* is, regardless of whether the digital input D1 is logic "1" or logic "0", fixed at low level during the low power period **T2**, in which the first switching signal is high-level. Further, an output from the gate **134***c* is, regardless of whether the digital input D2 is logic "1" or logic "0", fixed at high level throughout the low power period T2, in which the first switching signal is high-level.

By contrast, during the normal operation period T1, in which the first switching signal P is low-level, the output from each gate **134***a* to **134***c* changes according to the logic level of the digital inputs D0 to D2. Therefore, the fourth switches **132***a* to **132***c* are made to have a switching state corresponding to the digital input D0 to D2 by the second switching signals from the gates **134***a* to **134***c*. As a result, a desired output voltage is applied to an output terminal **116**.

It is to be noted that during the low power period T2, only the output from the **134***c* is high-level, and the outputs from the gate **134***a* and the gate **134***b* are low-level. That is, the outputs from the gates **134***a* to **134***c* are the identical to an input Data **5** (D2: "1", D1: "0", D0: "0"), which is described later, in the normal operation period T1, in which the first switching signal P is low-level.

In Table i below, there is shown a comparison between input data and electric currents I flowing in the resistance element network.

TABLE 1

Data No.	D2	D1	D0	Current value
Data 1	0	0	0	0
Data 2	0	0	1	0.328 (VH - VL)/R
Data 3	0	1	0	0.3125 (VH - VL)/R
Data 4	0	1	1	0.4531 (VH - VL)/R
Data 5	1	0	0	0.25 (VH - VL)/R
Data 6	1	0	1	0.4531 (VH - VL)/R
Data 7	1	1	0	0.3125 (VH - VL)/R
Data 8	1	1	1	0.328 (VH - VL)/R

As seen in Table 1, it is in the case of Data **6** (D2: "1", D1: "0", D0: "0") that the electric current I becomes the least value except in the case of the input data being "0".

Now referring to the timing chart of FIG. **18**, there is explained the power saving system of the DAC having the aforementioned construction. During the normal operation period **T1**, the first switching signal P is low-level, the fourth switches **132***a* to **132***c* are controlled in accordance with the input data D0 to D2, and the electric current I flowing between the power supply terminal **118***a* and **118***b* becomes an electric current value between "0" and I1 corresponding to the input data. The voltage at the output terminal **300** becomes a value between VL and VH corresponding to the input data. During the low power period, the first switching signal P becomes high-level and masks the gates **134***a* to **134***c*, and thereby the fourth switches **132***a* to **132***c* are set so as to result in Data **6**. As a result, the electric current I becomes I0, and the voltage at the output terminal **300** becomes a voltage V2, which is the voltage in the case of Data **5** (D2: "1", D1: "0", D0: "0"). Since the equivalent circuit of the DAC in the case of Data **5** is the one shown as the circuit diagram of FIG. **19**, it is understood that the voltage V2 is an median potential between VL and VH.

According to Table 1, in the case where the input data is Data **1**, the electric current becomes "0", and a consumed electric current thereby becomes the least value. However, the voltage at the output terminal **300** becomes VL, and therefore, in a transition from the low power period **T2** to the normal operation period **T1**, an average time necessary to change the voltage to a desired voltage becomes rather long. On the other hand, as in this embodiment, in the case of employing Data **5** as a fixed data, the electric current can be made the least value except in the case of the input data being Data **1**, and the potential at the output terminal **300** results in an approximately median value between VL and VH. Consequently, it is made possible to shorten the average time required for changing the voltage in the transition to the normal operation period T1, and additionally, to reduce a consumed power by a voltage variation.

It is noted that, in an R-2R ladder type DAC as used in this embodiment, the electric current at the median level results in the least value, and that the same effect can be obtained if the number of the input data bits is different from this example.

In this embodiment too, the low power period can be extended to a period in which the period required for making definite the voltage of the capacitive load **120** is excluded from one horizontal synchronizing period.

It is to be noted that, although in the example described above, the input data is fixed to be Data **5** by which the electric current results in the smallest value except in the case of Data 1, the present invention is not limited thereto. The input data may be set to be any input data by which the value of the electric current flowing in the resistance element network results in a smaller value than the median electric current value between the largest and the smallest. As described thus far, the reduction of power consumption can be achieved by employing such input data that can result in a electric current value smaller than the median electric current value, because, when the DAC is driven for a long period of time, the power consumption is made smaller than the average value.

(Embodiment 2-6)

FIG. **20** shows the construction of a DAC integrated in a driver circuit of Embodiment 2-6, and FIG. **20** is the timing chart thereof. This Embodiment 2-6 has a similar construction to Embodiment 2-5, and the same reference characters are used for the corresponding parts. In this Embodiment 2-6, a third switching signal generator circuit **133A** for generating a third switching signal is employed in place of the second switching generator circuit **133** used in Embodiment 2-5. This third switching signal generator circuit **133A** comprises gates **140***a* to **140***c*. The gate **140***a* comprises inverters **150** and **151**, a NOR gate **152**, and an OR gate **153**. The inverters **150** and **151** invert a digital input **D0** and output the inverted data. An output signal from the inverter **150** and the first switching signal P are inputted to the NOR gate **152**, and the NOR gate **152** outputs the third switching signal to the n-channel TFT of a switch **132***d*. An output signal from the inverter **151** and the first switching signal P are inputted to the OR gate **153**, and the OR gate **153** outputs the third switching signal to the p-channel transistor of a switch **132***d*. The gate **140***b* comprises inverters **154** and **155**, a NOR gate **156**, and an OR gate **157**. The inverters **154** and **155** invert the digital input D1 and output the inverted

data. An output signal from the inverter **154** and the first switching signal P are inputted to the NOR gate **156**, and the NOR gate **156** outputs the third switching signal to the n-channel TFT of a switch **132***e*. An output signal from the inverter **155** and the first switching signal P are inputted to the OR gate **157**, and the OR gate **157** outputs the third switching signal to the p-channel transistor of a third switch **132***e*. The gate **140**c comprises inverters **158** and **159**, a NOR gate **160**, and an OR gate **161**. The inverters **158** and **159** invert the digital input D2 and output the inverted data. An output signal from the inverter **158** and the first switching signal P are inputted to the NOR gate **160**, and the NOR gate **160** outputs the third switching signal to the n-channel TFT or a switch **132***f*. An output signal from the inverter **159** and the first switching signal P are inputted to the OR gate **161**, and the OR gate **161** outputs the third switching signal to the p-channel transistor of a switch **132***f*.

In this embodiment, as will be described later, controlled by the third switching signal generator circuit **133**A, fifth switches **132***d* to **132***f* are connected to either a high voltage power supply VH or a low voltage power supply VL corresponding to the digital input D0 to D2 during the normal operation period **T1**, and a desired driving voltage can be thus obtained.

During the low power period **T2**, since the first switching signal P is high-level, the output from the NOR gate **152** (which corresponds with the third switching signal) becomes low-level regardless of the logic level of the digital input **D0**. Likewise, the output from the OR gate **153** (which corresponds with the third switching signal) becomes high-level regardless of the logic level of the digital input D1. As a result, the fifth switch **132***d* is cut off from both the power supplies VH and VL. In a similar manner, the output from the NOR gate **156** (which corresponds with the third switching signal) is fixed at low level, and the output from the OR gate **157** (which corresponds with the third switching signal) is fixed at high level. As a result, the fifth switch **132***e* is cut off from both the power supplies VH and VL. Further, the output from the NOR gate **160** (which corresponds with the third switching signal) is fixed at low level, and the output from the OR gate **161** (which corresponds with the third switching signal) is fixed at high level. As a result, the fifth switch **132***f* is cut off from both the power supply VH and VL. Thus, the electric current flowing in the resistance elements in the DAC results in "0", and the reduction in power consumption can be achieved.

Referring now to the timing chart of FIG. **21**, there is explained the power saving system of the DAC having the above-described construction. During the normal operation period **T1**, the first switching signal P is low-level, the fifth switches **132***d* to **132***f* are controlled in response to the input data D0 to D2, and thereby the electric current I flowing in the resistance element network becomes an electric current value between "0" and I1 corresponding to the input data. The voltage at the output terminal **300** becomes a voltage value between VH and VL corresponding to the input data.

During the low power period **T2**, the first switching signal P is made to be high-level, and the fifth switches **132***d* to **132***f* are cut off from both the power supplies VL and VH. Therefore no power is supplied to the DAC, and a consumed power and a consumed current become "0". The voltage at the output terminal **300** becomes indefinite.

An output terminal **116** is cut off by an output switch **119**, and thereby the potential at the output terminal **116** is retained by the capacitive load **120**.

In this embodiment too, the low power period can be extended to a period in which the period required for making definite the voltage of the capacitive load **120** is excluded from one horizontal synchronizing period.

(Embodiment 2-7)

FIG. **22** is a circuit diagram showing the construction of the DAC of Embodiment 2-7, and FIG. **23** is the timing chart thereof. This Embodiment 2-7 has a similar construction to Embodiment 2-1, and the same reference characters are used for the corresponding parts. This Embodiment 2-7 differs from Embodiment 2-1 in that the DAC is composed of two digital-to-analog converter circuit sections. Now Embodiment 2-7 is detailed hereinafter. The DAC comprises a first DAC section **201** composed of a potentiometer type DAC and a second DAC section **202** composed of an R-2R ladder type DAC. The first DAC section **201** operates in response to more significant bits D2 and D3 of digital video input data. The second DAC section **202** comprises a first connecting terminal **220***a* which receives a higher voltage output from the first DAC section **201** and a second connecting terminal **220***b* which receives a lower voltage output from the first DAC section **201**. The second DAC section **202** uses a voltage between the first connecting terminal **220***a* and the second connecting terminal **220***b*, and operates in response to lesser significant bits D0 and D1 of the digital video input data. Hereinafter, the voltage of the first connecting terminal **220***a* is referred to as VH2 and the voltage of the second connecting terminal **220***b* is referred to as VL2.

The first DAC section **201** comprises resistance elements R4 to R7, a sixth switch TrP, seventh switches Tr4H to Tr7H, eighth switches Tr4L to Tr7L, and a selective circuit **203**. The selective circuit **203** decodes the more significant bits D2 and D3, and controls the seventh switches Tr4H to Tr7H and the eighth switches Tr4L to Tr7L by the decoded digital signals. The aforementioned sixth switch TrP is connected between the resistance element R7 and a power supply terminal **118***a*. In response to the first switching signal P, the sixth switch TrP is turned to ON state during the normal operation period T1 and OFF state during the low power period. Each seventh switch Tr4H to Tr7H is respectively connected between each connecting point of the resistance elements R4 to R7 and the first connecting terminal **220***a*, and each eighth switch Tr4L to Tr7L is respectively connected between each connecting point of the resistance elements R4 to R7 and the second connecting terminal **220***b*. The aforementioned resistance element **R01** has a resistance value of **r1**, and the resistance elements **R00**, **R0**, and **R1** have a resistance value of **r2**. The second DAC section **202** comprises resistance elements R0, R1, R00, and R01, and ninth switches **204** and **205** for alternatively selecting one connecting state between a connecting state to the first connecting terminal **220***a* and a connecting state to the second connecting terminal **220***b* in response to the lesser significant bits D0 and D1. The ninth switch **204** comprises a p-channel TFT Tr0L and a p-channel TFT Tr0H, and the ninth switch **205** comprises a p-channel TFT Tr1L and a p-channel TFT Tr1H.

An electric current I which is consumed in all the resistance elements in a DAC having such a construction is represented by the sum of an electric current I1 which flows in the resistance element R4 to R7 in the first DAC section **201** and an electric current I2 which flows in the resistance elements R0, R1, R00, and R01 in the second DAC section **202**. That is, I=I1+I2.

In this case, regardless of the input data D2 and D3, the electric current I1 is I1=(VH−VL)/(R7+R6+R5+R4). It is noted that, for the sake of convenience in illustration, each of the resistance values of the resistance elements R4 to R7

is represented by R4, R5, R6, and R7, respectively. Now, on the other hand, the electric current I2 varies according to the input data, as shown in Table 2 below, the minimum value being "0" and the maximum value being I2max=0.3125·(VH2−VL2)max/r1.

TABLE 2

Data No.	D1	D0	Electric current value
Data 1	0	0	0
Data 2	0	1	0.3125 (VH - VL)/R
Data 3	1	0	0.25 (VH - VL)/R
Data 4	1	1	0.3125 (VH - VL)/R

The operation of the above-mentioned circuit is now detailed now. During the normal operation period T1, the first switching signal P is low-level and the sixth switch TrP is turned to ON state. As a consequence, the electric current I is set at an electric current value between I1 and I0 (I0=I1+I2max) corresponding to a logic level of each of the input data D0 to D3. The potential of the output terminal 300 becomes a value corresponding to the input data D0 to D3 within the range between VL and VH.

During the low power period T2, the first switching signal P is switched to high level, and the sixth switch TrP is thereby turned to OFF state. As a result, the power supply VH is cut off, and the electric current I becomes "0", achieving the reduction of power consumption during the low power period T2. The potential at the output terminal 300 is indefinite, and the potential of the capacitive load 120 does not vary because the output switch 119 is turned OFF.

The reduction in power consumption is thus achieved by cutting off the power supply of the first DAC section 201, which is a voltage potentiometer type DAC allotted for more significant bits.

(Embodiment 2-8)

FIG. 24 is a circuit diagram showing the construction of the DAC of Embodiment 2-8, and FIG. 25 is the timing chart thereof. This Embodiment 2-8 has a similar construction to Embodiment 2-7, and the same reference characters are used for the corresponding parts. This Embodiment 2-8 employs a tenth switch 210 for alternatively selecting either a first high voltage power supply VHH or a second high voltage power supply VHL having a lower voltage level than the first high voltage power supply VHH, in place of the sixth switch TrP used in Embodiment 2-7. This tenth switch 210 is composed of an n-channel TFT and a p-channel TFT, and the first switching signal P is fed to each gate of the n-channel TFT and the p-channel TFT. Thereby, in the case of the first switching signal P being high-level, i.e. during the low power period T2, the second high voltage power supply VHL is selected, while in the case of the first switching signal P being low-level, i.e., during the normal operation period T1, the first high voltage power supply VHH is selected.

The operation of the DAC having the aforementioned construction is explained hereinafter. An electric current I consumed in all the resistance elements in the DAC is represented by the sum of an electric current I1 which flows in the resistance elements in the first DAC section 201 allotted for the more significant bits and an electric current I2 which flows in the resistance elements in the second DAC section 202 allotted for the lesser significant bits. That is, I=I1+I2.

During the normal operation period T1, regardless of the input data, the electric current I1 becomes I1=(VHH−VL)/(R7+R6+R5+R4). On the other hand, the electric current I2 varies according to the input data, as shown in the above Table 2, the minimum value being "0" and the maximum value being I2max=0.3125·(VHH2−VL2)max/r1, where r1 is a resistance value of the resistance element R01. Therefore, the electric current I varies within the range between I1 and I0 (I0=I1+I2max).

During the low power period T2, regardless of the input data, the electric current I1 becomes I1=(VHL−VL)/(R7+R6+R5+R4). I2max also becomes lower since (VH2−VL2) max becomes lower. In this case, when I1L=(VHL−VL)/(R7+R6+R5+R4) and I0L=I1L+I2max, the electric current I1 varies within the range between I1L and I0L. Hence, the reduction of power consumption during the low power period T2 can be achieved.

During the normal operation period T1, the voltage at the output terminal 300 is a potential between VL and VHH. However, during the low power period T2, it becomes a potential between VL and VH. For this reason, a source line is cut off by making the output switch 119 OFF so that the potential of the capacitive load 120 is retained.

The reduction in power consumption is thus achieved by selecting the power supplies of the first DAC section 201, which is a voltage potentiometer type DAC allotted for more significant bits.

(Embodiment 2-9)

FIG. 26 is a circuit diagram showing the construction of the DAC of Embodiment 2-9, and FIG. 27 is the timing chart thereof. This Embodiment 2-9 has a similar construction to Embodiment 2-8, and the same reference characters are used for the corresponding parts. In this Embodiment 2-9, the switch 210 for switching the power supply used in Embodiment 2-8 is eliminated. Instead, in the second DAC section 202, a fourth switching signal generator circuit 211 is provided. The fourth switching signal generator circuit 211 generates a fourth switching signal for controlling switching states of ninth switches 204 and 205, and outputs the fourth switching signal to the ninth switches 204 and 205. The fourth switching signal generator circuit 211 comprises an inverter 213, a NOR gate 214, and an OR gate 215. A bit D0 is inputted to the inverter 213. The output signal from the inverter 213 and the first switching signal P are inputted to the NOR gate 214, and the NOR gate 214 outputs the fourth switching signal to a p-channel TFT Tr0L and an n-channel TFT Tr0H. A bit D1 and the first switching signal P is inputted to the OR gate 215, and the OR gate 215 outputs the fourth switching signal to a p-channel TFT Tr1L and an n-channel TFT Tr1H. Having such a construction, during the normal operation period T1, the fourth switching signal generator circuit 211 outputs the fourth switching signal corresponding to digital video input data. By contrast, during the low power period T2, it fixes the lesser significant bits D0 and D1 of the digital video data to be a fixed data which results in the second least electric current value among the electric current values in the resistance element network, and outputs the fixed input data as the fourth switching signal.

The operation of the DAC having the aforementioned construction is explained hereinafter. An electric current I consumed in all the resistance elements in the DAC is represented by the sum of an electric current I1 which flows in the resistance elements in the first DAC section 201 and an electric current I2 which flows in the resistance elements in the second DAC section 202. That is, I=I1+I2.

In this case, regardless of the input data, the electric current I1 is I1=(VH−VL/(R7+R6+R5+R4). On the other hand, the electric current I2 varies according to the input data, as shown in the above Table 2, the minimum value being 0 and the maximum value being I2max=0.3125(VH2−VL2)max/r1.

During the normal operation period T1, the electric current I varies within the range between I1 and I0 (=I1+I2max). The potential of the terminal **300** is within the range between VL and VH.

During the low power period T2, the data D0 is masked to be "0" and the data D1 is masked to be "1". As a result, the electric current I2 becomes I2=0.25·(VH2−VL2)/r1. Naturally, I2 can be made smaller when the both data D0 and D1 are "0". However, in an R-2R ladder type DAC, the electric current becomes the second least when only the data D1 is fixed to be "1", and the output voltage can be more quickly changed to the desired voltage in a transition to the normal operation period T1 by giving a certain potential to each contact point in the circuit. It is noted that during the low power period T2, the potential of the capacitive load **120** does not vary since the output switch **119** is turned OFF.

The reduction of power consumption is thus achieved by switching the input data of the second DAC section, which is an R-2R ladder type DAC allotted for lesser significant bits.

(Embodiment 2-10)

FIG. **28** is a circuit diagram showing the construction of the DAC of Embodiment 2-10, and FIG. **29** is the timing chart thereof. This Embodiment 2-10 has a similar construction to Embodiment 2-7, and the same reference characters are used for the corresponding parts. In this Embodiment 2-9, the sixth switch TrP used in Embodiment 2-7 is eliminated. On the other hand, an eleventh switch TrPH is provided between the first connecting terminal **220***a* and an input of the second DAC section **202**, and a twelfth switch TrPL is provided between the second connecting terminal **220***b* and an input of the second DAC section **202**. The ON/OFF states of the eleventh switch TrPH and the twelfth switch TrPL are controlled by the first switching signal P.

The operation of the DAC having the aforementioned construction is explained hereinafter. An electric current I consumed in all the resistance elements in the DAC is represented by the sum of an electric current I1 which flows in the resistance elements in the first DAC section **201** allotted for the more significant bits and an electric current I2 which flows in the resistance elements in the second DAC section **202** allotted for the lesser significant bits. That is, I=I1+I2.

Regardless of the input data, the electric current I1 is I1=(VH−VL)/(R7+R6+R5+R4). On the other hand, the electric current I2 varies according to the input data, as shown in the above Table 2, the minimum value being "0" and the maximum value being I2max=0.3125(VH2−VL2)max/r1 in the case of two-bit data.

During the normal operation period T1, the electric current I varies within the range between I1 and I0 (=I1+I2max). During the low power period T2, the eleventh switch TrPH and the twelfth switch are turned OFF, and the electric current I2 thereby results in I2=0, and consequently the electric current I becomes I=I1.

The potential of the terminal **300** is within the range between VL and VH during the normal operation period T1, and it becomes indefinite during the low power period T2. The potential of the capacitive load **120** does not vary during the low power period T2 since the output switch **119** is turened OFF.

The reduction of power consumption is thus achieved by cutting off the power supply of the second DAC section, which is an R-2R ladder type DAC allotted for lesser significant bits.

(Embodiment 2-11)

FIG. **30** is a circuit diagram showing the construction of the DAC of Embodiment 2-11, and FIG. **31** is the timing chart thereof. This Embodiment 2-10 has a similar construction to Embodiment 2-9, and the same reference characters are used for the corresponding parts. In this Embodiment 2-11, two high voltage power supplies, a first high voltage power supply VHH and a second high voltage power supply VHL are employed in place of the high voltage power supply VH used in Embodiment 2-9. The second high voltage power supply VHL has a lower voltage level than the first high voltage power supply VHH. In addition, a tenth switch **210** is provided for selecting one power supply between the power supplies VHH and VHL.

The operation of the DAC having the aforementioned construction is explained hereinafter. An electric current I consumed in all the resistance elements in the DAC is represented by the sum of an electric current I1 which flows in the resistance elements in the first DAC section **201** allotted for the more significant bits and an electric current I2 which flows in the resistance elements in the second DAC section **202** allotted for the lesser significant bits. That is, I=I1+I2.

During the normal operation period T1, the electric current I1 is I1=(VHH−VL)/(R7+R6+R5+R4) regardless of the input data. On the other hand, the electric current I2 varies according to the input data, as shown in the above Table 2, the minimum value being "0" and the maximum value being I2max=0.3125(VH2−VL2)max/r1. Consequently, the electric current I varies within the range between I1 and I0(=I1+I2max).

During the low power period T2, the power supply VHH is switched to the power supply VHL, and the electric current I1 becomes I1=(VHL−VL)/(R7+R6+R5+R4). In addition, during the low power period T2, a data D0 is masked to be "0" and a data D1 is masked to be "1", and therefore the electric current I2 becomes I2=0.25·(VH2−VL2)/r1. As a result, the electric current I becomes smaller than that in the normal operation period T1. As in Embodiment 2-7, the data can be masked by selecting a logic. During the low power period T2, the potential of the capacitive load **120** does not vary since the output switch **119** is turned OFF.

The reduction of power consumption is thus achieved by selecting the power supplies of the first DAC section allotted for more significant bits, which is a voltage potentiometer type DAC, and by switching the input data of the second DAC section allotted for lesser significant bits, which is an R-2R ladder type DAC.

(Embodiment 2-12)

FIG. **32** is a circuit diagram showing the construction of the DAC of Embodiment 2-12, and FIG. **33** is the timing chart thereof. This Embodiment 2-12 has a similar construction to Embodiment 2-8, and the same reference characters are used for the corresponding parts. This Embodiment 2-12 differs from Embodiment 2-8 in that an eleventh connecting terminal **220***a* and a twelfth connecting terminal **220***b* are provided.

The operation of the DAC with the aforementioned construction is explained hereinafter. An electric current I consumed in all the resistance elements in the DAC is represented by the sum of an electric current I1 which flows in the resistance elements in the first DAC section **201** allotted for the more significant bits and an electric current I2 which flows in the resistance elements in the second DAC section **202** allotted for the lesser significant bits. That is, I=I1+I2.

During the normal operation period T1, the electric current I1 is I1=(VHH−VL)/(R7+R6+R5+R4) regardless of the input data. On the other hand, the electric current I2 varies

according to the input data, as shown in the above Table 2, the minimum value being "0" and the maximum value being I2max=0.3125(VH2−VL2)max/r1. Consequently, the electric current I varies within the range between I1 and I0 (=I1+I2max).

During the low power period T2, the power supply VHH is switched to the power supply VHL, and the electric current I1 becomes I1=(VHL−VL)/(R7+R6+R5+R4). In addition, the switches TrPH and TrPL are turned OFF, and thereby the electric current I2 becomes "0".

The potential of the terminal **300** is within the range between VL and VH during the normal operation period T1, and becomes indefinite during the low power period T2. The potential of the capacitive load **120** does not vary during the low power period T2 since the output switch **119** is turned OFF.

The reduction of power consumption is thus achieved by selecting the power supplies of the first DAC section allotted for more significant bits, which is a voltage potentiometer type DAC, and by cutting off the power supply of the second DAC section allotted for lesser significant bits, which is an R-2R ladder type DAC.

(Embodiment 2-13)

FIG. **34** shows the constructions of a portion of an array in the active matrix liquid crystal panel and of a portion of a driver circuit of Embodiment 2-13, and FIG. **35** is the timing chart thereof. In FIG. 34, it is shown that each one of DACs is connected to each one of source lines SL in the array, and that a power supply terminal **118***a* and a power supply terminal **118***b* are connected to each DAC. These DACs have a similar construction to the one shown in Embodiment 2-5. More specifically, a fifth switching signal generator circuit is provided in place of the first switching signal generator circuit **105**. The fifth switching signal generator circuit receives a horizontal synchronizing signal and generates a fifth switching signal for selecting between a precharge period mode, which is for a precharge to be carried out prior to writing a video data to a source line, and a remaining period mode, which is a period except the precharge period. In addition, a sixth switching signal generator circuit is provided in place of the second switching signal generator circuit for controlling the switching states of a group of the previously-mentioned fourth switches. The sixth switching signal generator circuit generates a sixth switching signal for controlling switching states of the fourth switches, and outputs the sixth switching signal to the fourth switches. The sixth switching signal generator circuit receives digital video data and the fifth switching signal from the above-mentioned fifth switching signal generator circuit, and during the above-mentioned remaining period, it outputs the sixth switching signal corresponding to the digital video data. During the above-mentioned precharge period, it fixes the input data to be any one of the data by which a value of the electric current flowing in the resistance element network results in a smaller value than the median electric current value between the largest and the smallest, and outputs the fixed input data as the sixth switching signal. As a result, during the low power period T2, a voltage V2 which is determined by the data which is masked by the fifth switching signal is outputted. It is noted that the output switch **119** is eliminated in this embodiment. Therefore, during the low power period T2, the voltage V2 is written to the source line SL as a precharge voltage.

In such an active matrix liquid crystal panel, it is necessary that a polarity of a source line voltage be inverted in a certain periodic cycle in order to apply an alternating voltage to the liquid crystal elements. The time required for this polarity inversion of the source line voltage depends on a capacity and resistance of the source line, but generally, it tends to be longer as the size and resolution of the LCD increases. If the polarity inversion of the source line voltage is carried out simultaneously with a writing of video data, a shortage of the writing of video data will be brought about in the case where the capacitance and resistance of the source line increases and thereby the time required for the polarity inversion is made longer.

In view of this, prior to the writing of video data, the polarity inversion of the source line is carried out by utilizing the period in which a gate of a pixel switch transistor for driving a liquid crystal element is turned OFF, generally during the blanking period of the horizontal synchronizing period. Such an operation is called a precharge. During this precharge period, a certain voltage with an inverted polarity is intentionally written to the source line, but at the same time, it is made possible to utilize the voltage V2 as a voltage for the precharge by making the fifth switching signal in the DAC high level and thereby switching over to the low power period. As a result, the improvement of image quality as well as the reduction of power consumption can be achieved at a time.

In the above example, although this embodiment is applied to the DAC in Embodiment 2-5, this embodiment is not limited thereto and can be suitably applied to the other embodiments.

(Embodiment 2-14)

FIG. **36** illustrates the construction of a driver circuit of Embodiment 2-14. This Embodiment 2-14 has a similar construction to Embodiment 2-1, and the same reference characters are used for the corresponding parts. In this Embodiment 2-14, a first switching signal generator circuit **105**A is employed in place of the first switching signal generator circuit **105** used in Embodiment 2-1. As shown in FIG. **37**, this first switching signal generator circuit **105**A comprises a delay circuit **315** and an AND gate **316**. The delay circuit **315** receives a horizontal synchronizing signal and delays the horizontal synchronizing signal for a predetermined delay time. The AND gate **316** outputs a first switching signal P when it obtains an AND condition of an output from the delay circuit **315** and the horizontal synchronizing signal. The delay circuit **315** comprises an integrator circuit **319**, and inverters **320***a* and **320***b*. The integrator circuit comprises a resistance element **317** that is formed by the impurity-containing semiconductor layer on the array substrate, and a capacitance element **318** that is formed by the insulation layer on the array substrate. The inverters **320***a* and **320***b* are composed of a TFT on the array substrate. The AND gate **316** is also composed of a TFT on the array substrate.

Referring now to the timing chart of FIG. **38**, there is detailed the workings of input signals in the first switching signal generator circuit **105**A having such a construction. When a horizontal synchronizing signal inputted to an input terminal **321** turns to high level, an output level of the integrator circuit **319**, which is composed of the resistance element **317** and capacitance element **318**, ascends in accordance with a time constant determined by the resistance element **317** and capacitance element **318**. Thereupon, when the output level of the integrator circuit **319** reaches a threshold voltage of the inverter **320***a*, an output of the inverter **320***a* turns from high level to low level. An output of the inverter **320***b* thereby turns from low level to high level. Thereafter, when the horizontal synchronizing signal turns to low level, the output level of the integrator circuit **319** descends in accordance with the time constant deter-

mined by the resistance element **317** and capacitance element **318**. Thereupon, when the output of the integrator circuit **319** reaches the threshold voltage of the inverter **320***a*, the output of the inverter **320***a* turns from low level to high level, and thereby the output of the inverter **320***b* turns from high level to low level. As a consequence, the output of the inverter **320***b* is delayed for a time TD determined by a time constant of the integrator circuit **319**. Thus, a signal in which the horizontal synchronizing signal and the output of the inverter **320***b*, which is a delayed horizontal synchronizing signal, are ANDed together, is outputted from the AND gate **316** as a first switching signal.

The delay time TD is the total of each delay time in the integrator circuit **319** and the inverters **320***a* and **320***b*. However, when compared with a delay time in the integrator circuit **319**, a delay time in the inverters **320***a* and **320***b* is so small that it is negligible. Therefore, only the delay time in the integrator circuit **319** should be taken into consideration. That is, the circuit should be arranged so that the delay by the integrator circuit **319** is dominant. Specifically, the capacitance value C should be set far smaller than the resistance value R of the resistance element **317**. Therefore, it is considered that the time constant of the integrator circuit **319** is determined by the resistance value R of the resistance element **317**, and thereby the delay time can be determined by the resistance value R of the resistance element **317**. Hence, when the resistance element **317** has a large resistance value, the first switching signal P results in a waveform shown by the solid line in FIG. **38**, and accordingly the delay time of the horizontal synchronizing signal becomes long as shown by the reference character TDRH. On the other hand, when the resistance element **317** has a small resistance value, the first switching signal P results in a waveform as shown by the dashed line in FIG. **38**, and accordingly the delay time of the horizontal synchronizing signal becomes short as shown by the reference character TDRL. It is noted that the length of the low power period also changes correspondingly, as illustrated in the following. When the resistance element **317** has a large resistance value, the low power period accordingly becomes short as shown by the reference character TRH, and conversely, when the resistance element **317** has a small resistance value, the low power period accordingly becomes long as shown by the reference character TRL.

In the case where the resistance elements on the array substrate have a large resistance value, the electric current in the DAC is small and thereby a time for charging a capacitive load **120**, which is connected to a source line SL via an output terminal **116**, becomes long. Therefore, in this case, it is preferable that the low power period T2 be relatively short. Even if the low power period T2 is short (i.e., the normal operation period T1 is long), the power consumption in the normal operation period T1 is still reduced since the resistance elements have a high resistance value. Hence, no adverse effect will be caused in the reduction of power consumption. On the other hand, in the case where the resistance elements on the array substrate have a small resistance value, the current in the DAC is large, and therefore the time required for charging a source lines SL becomes short. Therefore, in this case, it is preferable that the low power period T2 be relatively long. As has been described, there arises a necessity to change lengths of the normal operation period T1 and the low power period T2 corresponding to a resistance value of the resistance elements on the array substrate, in order to meet two requirements, one being the charge of the source line and the other being the reduction in power consumption. In such a case, the first switching signal generator circuit **105A** automatically adjusts the length of a high level period of the first switching signal P most suitably to meet those requirements. Hence, it is made possible to automatically adjust the power consumption optimally at any time, regardless of the precision of the resistance elements, by constructing the integrator circuit by the resistance element formed on the same array substrate as the resistance elements in the DAC are formed.

Now the effect of the first switching signal generator circuit **105A** is further detailed below.

The high level period of the first switching signal is defined as a period except the normal operation period (the normal operation period is a period in which a period to completely change a potential of a pixel electrode is added to a period to completely change a potential of a capacitive load connected to a source line SL in the entire period of one horizontal synchronizing period). The resistance value of the resistance element **317** is determined so that the period except the normal operation period equals to the high level period of the first switching signal. However, in practice, there occurs an error in the resistance value. This error brings about such adverse effects that a shortage of charging to the source line SL causes the deterioration of display characteristics and that a desired amount of power consumption cannot be obtained, since the length of the high level period of the first switching signal P results in a different length from a predetermined length. However, according to this embodiment, since the first switching signal generator circuit **105A** has such a construction as described above, it is made possible to avoid the above-mentioned adverse effects as well as the shortage of the charging to the source line SL, and thus an optimization of power consumption can be achieved.

For instance, in the case of a resistance value of each resistance element in the DAC being larger than a predetermined resistance value, a resistance value of the resistance element **317** is also larger than the predetermined value. On the other hand, in the case of the resistance value of each resistance element in the DAC being smaller than the predetermined resistance value, the resistance value of the resistance element **317** is also smaller than the predetermined value. The reason is that it is considered that the same degree of error will occur to both of the resistance elements since they are both formed by the impurity-containing semiconductor layer on the same array substrate.

In addition, in the case where a resistance value is larger than a predetermined value, an electric current flowing in the resistance elements of the DACs is made smaller during the normal operation period. As a result, the potential of the source line SL cannot be changed to a desired potential unless the high level period of the first switching signal P is precisely adjusted according to the resistance elements, and therefore, the deterioration of display characteristics will be incurred. However, according to this embodiment, a precise adjustment of the high level period (i.e., the low power period) of the first switching signal P can be achieved by constructing the first switching signal generator circuit **105A** in accordance with the construction shown in FIG. **37**. Thereby, the high level period becomes shorter than the original length, and accordingly, the normal operation period T1 becomes longer. Therefore, it is made possible to change the potential of the source line to a desired potential, and as a result to prevent the deterioration of display characteristics. It is noted that although the low power period is made shorter, the power consumption is practically not increased since the electric current in the normal operation period is reduced.

On the other hand, in the case where the resistance value is smaller than a predetermined value, the current flowing in the resistance elements in the DAC is made larger during the normal operation period. As a result, the power required for a normal operation is consumed even after the potential of the source line SL is changed to the desired potential, unless the high level period of the first switching signal P is precisely adjusted according to the resistance elements. It is a waste of power consumption when considered from the viewpoint of the reduction in power consumption. However, according to this embodiment, a precise adjustment of the high level period (i.e., the low power period) of the first switching signal P can be achieved by constructing the first switching signal generator circuit **105A** in accordance with the construction shown in FIG. **37**, and thereby the high level period is made longer (i.e., the normal operation period is made shorter) than the original length. The waste of power consumption can be thus avoided.

Hence, according to this embodiment, a variation of power consumption caused by a resistance value variation of the resistance elements in each manufactured array substrate can be compensated without relying on an adjustment by external circuits, and therefore the simplification of external circuits and the optimization of power consumption are easily achieved.

It is noted that, although an insulation layer on the array substrate is utilized for the capacitance element in this embodiment, a generally available capacitor component may be used for the capacitance element.

FIG. **39** is the timing chart showing the operation of the DAC in Embodiment 2-14. Although this Embodiment 2-14 differs from Embodiment 2-1 in that the first switching signal P is generated from the horizontal synchronizing signal, the operation of the DAC is basically identical to Embodiment 2-1.

(Embodiment 2-15)

FIG. **40** shows the construction of a DAC in Embodiment 2-15. This Embodiment 2-15 has a similar construction to Embodiment 2-3, and the same reference characters are used for the corresponding parts. In this Embodiment 2-15, the first switching signal generator circuit **105A** is employed in place of the first switching signal generator circuit **105** employed in Embodiment 2-3.

FIG. **41** is the timing chart showing the operations of the driver circuit. Although this Embodiment 2-15 differs from Embodiment 2-3 in that the first switching signal P is generated from the horizontal synchronizing signal, the operation of the DAC is basically identical to Embodiment 2-3. As well as Embodiment 2-14, this Embodiment 2-15 makes it possible to compensate the variation of power consumption caused by the resistance value variation of the resistance elements in each manufactured array substrate without relying on an adjustment by external circuits, and therefore easily achieves the simplification of external circuits and the optimization of power consumption.

(Embodiment 2-16)

FIG. **42** shows the construction of a DAC in Embodiment 2-16. This Embodiment 2-16 has a similar construction to Embodiment 2-5, and the same reference characters are used for the corresponding parts. In this Embodiment 2-16, the first switching signal generator circuit **105A** is employed in place of the first switching signal generator circuit **105** employed in Embodiment 2-5.

FIG. **43** is the timing chart showing the operations of the DAC. Although this Embodiment 2-15 differs from Embodiment 2-5 in that the first switching signal P is generated from the horizontal synchronizing signal, the operation of the DAC is basically identical to Embodiment 2-5. As well as Embodiment 2-14, this Embodiment 2-16 makes it possible to compensate the variation of power consumption caused by the resistance value variation of the resistance elements in each manufactured array substrate without relying on an adjustment by external circuits, and therefore easily achieves the simplification of external circuits and the optimization of power consumption.

(Embodiment 2-17)

FIG. **44** shows the construction of a DAC in Embodiment 2-17. This Embodiment 2-17 has a similar construction to Embodiment 2-6, and the same reference characters are used for the corresponding parts. In this Embodiment 2-17, the first switching signal generator circuit **105A** is employed in place of the first switching signal generator circuit **105** employed in Embodiment 2-6.

FIG. **45** is the timing chart showing the operations of the driver circuit. Although this Embodiment 2-17 differs from Embodiment 2-6 in that the first switching signal P is generated from the horizontal synchronizing signal, the operation of the DAC is basically identical to Embodiment 2-6. As well as Embodiment 2-14, this Embodiment 2-17 makes it possible to compensate the variation of power consumption caused by the resistance value variation of the resistance elements in each manufactured array substrate without relying on an adjustment by external circuits, and therefore easily achieves the simplification of external circuits and the optimization of power consumption.

(Embodiment 2-18)

FIG. **46** shows the construction of a DAC in Embodiment 2-18. This Embodiment 2-18 has a similar construction to Embodiment 2-7, and the same reference characters are used for the corresponding parts. In this Embodiment 2-17, the first switching signal generator circuit **105A** is employed in place of the first switching signal generator circuit **105** employed in Embodiment 2-7.

FIG. **47** is the timing chart showing the operations of the driver circuit. Although this Embodiment 2-17 differs from Embodiment 2-7 in that the first switching signal P is generated from the horizontal synchronizing signal, the operation of the DAC is basically identical to Embodiment 2-7. As well as Embodiment 2-14, this Embodiment 2-18 makes it possible to compensate the variation of power consumption caused by the resistance value variation of the resistance elements in each manufactured array substrate without relying on an adjustment by external circuits, and therefore easily achieves the simplification of external circuits and the optimization of power consumption.

(Embodiment 2-19)

FIG. **48** shows the construction of a driver circuit in Embodiment 2-19. This Embodiment 2-19 has a similar construction to Embodiment 2-8, and the same reference characters are used for the corresponding parts. In this Embodiment 2-19, the first switching signal generator circuit **105A** is employed in place of the first switching signal generator circuit **105** employed in Embodiment 2-8.

FIG. **49** is the timing chart showing the operations of the DAC. Although this Embodiment 2-19 differs from Embodiment 2-8 in that the first switching signal P is generated from the horizontal synchronizing signal, the operation of the DAC is basically identical to Embodiment 2-8. As well as Embodiment 2-14, this Embodiment 2-19 makes it possible to compensate the variation of power consumption caused by the resistance value variation of the resistance elements in each manufactured array substrate without relying on an adjustment by external circuits and therefore easily achieves the simplification of external circuits and the optimization of power consumption.

(Embodiment 2-20)

FIG. **50** shows the construction of a DAC in Embodiment 2-20. This Embodiment 2-20 has a similar construction to Embodiment 2-9, and the same reference characters are used for the corresponding parts. In this Embodiment 2-20, the first switching signal generator circuit **105**A is employed in place of the first switching signal generator circuit **105** employed in Embodiment 2-9.

FIG. **51** is the timing chart showing the operations of the DAC. Although this Embodiment 2-20 differs from Embodiment 2-9 in that the first switching signal P is generated from the horizontal synchronizing signal, the operation of the DAC is basically identical to Embodiment 2-9. As well as Embodiment 2-14, this Embodiment 2-20 makes it possible to compensate the variation of power consumption caused by the resistance value variation of the resistance elements in each manufactured array substrate without relying on an adjustment by external circuits, and therefore easily achieves the simplification of external circuits and the optimization of power consumption.

(Embodiment 2-21)

FIG. **52** shows the construction of a DAC in Embodiment 2-21. This Embodiment 2-21 has a similar construction to Embodiment 2-10, and the same reference characters are used for the corresponding parts. In this Embodiment 2-21, the first switching signal generator circuit **105**A is employed in place of the first switching signal generator circuit **105** employed in Embodiment 2-10.

FIG. **53** is the timing chart showing the operations of the DAC. Although this Embodiment 2-21 differs from Embodiment 2-10 in that the first switching signal P is generated from the horizontal synchronizing signal, the operation of the DAC is basically identical to Embodiment 2-10. As well as Embodiment 2-14, this Embodiment 2-21 makes it possible to compensate the variation of power consumption caused by the resistance value variation of the resistance elements in each manufactured array substrate without relying on an adjustment by external circuits, and therefore easily achieves the simplification of external circuits and the optimization of power consumption.

(Embodiment 2-22)

FIG. **54** shows the construction of a DAC in Embodiment 2-22. This Embodiment 2-22 has a similar construction to Embodiment 2-11, and the same reference characters are used for the corresponding parts. In this Embodiment 2-22, the first switching signal generator circuit **105**A is employed in place of the first switching signal generator circuit **105** employed in Embodiment 2-11.

FIG. **55** is the timing chart showing the operations of the DAC. Although this Embodiment 2-22 differs from Embodiment 2-11 in that the first switching signal P is generated from the horizontal synchronizing signal, the operation of the DAC is basically identical to Embodiment 2-11. As well as Embodiment 2-14, this Embodiment 2-22 makes it possible to compensate the variation of power consumption caused by the resistance value variation of the resistance elements in each manufactured array substrate without relying on an adjustment by external circuits, and therefore easily achieves the simplification of external circuits and the optimization of power consumption.

(Embodiment 2-23)

FIG. **56** shows the construction of a DAC in Embodiment 2-23. This Embodiment 2-23 has a similar construction to Embodiment 2-12, and the same reference characters are used for the corresponding parts. In this Embodiment 2-23, the first switching signal generator circuit **105**A is employed in place of the first switching signal generator circuit **105** employed in Embodiment 2-12.

FIG. **57** is the timing chart showing the operations of the DAC. Although this Embodiment 2-23 differs from Embodiment 2-12 in that the first switching signal P is generated from the horizontal synchronizing signal, the operation of the DAC is basically identical to Embodiment 2-12. As well as Embodiment 2-14, this Embodiment 2-23 makes it possible to compensate the variation of power consumption caused by the resistance value variation of the resistance elements in each manufactured array substrate without relying on an adjustment by external circuits, and therefore easily achieves the simplification of external circuits and the optimization of power consumption.

(Embodiment 2-24)

FIG. **58** is a circuit diagram showing the construction of another first switching signal generator circuit **105**B, and FIG. **59** is the timing chart showing the operation thereof. This first switching signal generator circuit **105***b* receives an inverted horizontal synchronizing signal, which has an inverted polarity to a horizontal synchronizing signal, and generates a first switching signal P. It is noted that in the DACs utilizing this first switching signal generator circuit **105**B, the inverted horizontal synchronizing signals are used in place of the horizontal synchronizing signals, and accordingly the first switching signal generator circuit **105**B is used. This first switching signal generator circuit **105**B has a similar construction to the first switching signal generator circuit **105**A, and the same reference characters are used for the corresponding parts. The first switching signal generator circuit **105**B differs from the first switching signal generator circuit **105**A in that a NOR gate **400** is provided in place of the AND gate **316**.

Referring now to the timing chart of FIG. **55**, there is explained hereinafter the workings of input signals in the first switching signal generator circuit **105**B having such a construction. When a horizontal synchronizing signal inputted to an input terminal **321** turns to high level, an output level of an integrator circuit **319**, which is composed of a resistance element **317** and capacitance element **318**, ascends in accordance with a time constant set by the resistance element **317** and capacitance element **318**. Thereupon, when the output level of the integrator circuit **319** reaches a threshold voltage of the inverter **320***a*, an output of the inverter **320***a* turns from high level to low level. An output of the inverter **320***b* thereby turns from low level to high level. Thereafter, when the horizontal synchronizing signal turns to low level, the output level of the integrator circuit **319** descends in accordance with the time constant determined by the resistance element **317** and capacitance element **318**. Thereupon, when the output of the integrator circuit **319** reaches the threshold voltage of the inverter **320***a*, the output of the inverter **320***a* turns from low level to high level, and thereby the output of the inverter **320***b* turns from high level to low level. As a consequence, the output of the inverter **320***b* is delayed for a time TD determined by a time constant of the integrator circuit **319**, as shown in FIG. **59**. Thus, an inverted signal of a logical sum of the inverted horizontal synchronizing signal and the output of the inverter **320***b*, which is a delayed inverted horizontal synchronizing signal, is outputted from the NOR gate **400** as the first switching signal.

In this first switching signal generator circuit **105**B, the first switching signal P is delayed by the R-C integrator circuit **319**. Therefore, as seen in the first switching signal generator circuit **105**A, when the resistance element **317** has a large resistance value, the first switching signal P results in a waveform shown by the solid line in FIG. **59**, and accordingly the delay time of the horizontal synchronizing

signal becomes long as shown by the reference character TDRH. On the other hand, when the resistance element **317** has a small resistance value, the first switching signal P results in a waveform as shown by the dashed line in FIG. **59**, and accordingly the delay time of the horizontal synchronizing signal becomes short as shown by the reference character TDRL. It is noted that the length of the low power period also changes correspondingly, as illustrated in the following. When the resistance element **317** has a large resistance value, the low power period accordingly becomes short as shown by the reference character TRH, and conversely, when the resistance element **317** has a small resistance value, the low power period accordingly becomes long as shown by the reference character TRL. Hence, the optimization of power consumption can be also achieved by employing the first switching signal generator circuit **105**B having such a construction.

It is noted that, in place of the circuit construction of FIG. **58**, it is also possible to employ a circuit construction in which an inverter for inverting an inverted horizontal synchronizing signal is provided and the first switching signal generator circuit **105**A is connected to the inverter succeedingly.

(Embodiment 2-25)

FIG. **60** is a circuit diagram showing the construction of further another first switching signal generator circuit **105**C. This first switching signal generator circuit **105**C has a similar construction to the first switching signal generator circuit **105**, and the same reference characters are used for the corresponding parts. In this first switching signal generator circuit **105**C, an integrator circuit **319**C is employed in place of the integrator circuit **319** employed in the first switching signal generator circuit **105**. This integrator circuit **319**C comprises a resistance element **317** and four capacitance elements **500***a*, **500***b*, **500***c*, and **500***d*. These capacitance elements are composed of the capacitive load **120**. The capacitance element **500***a* is a capacitance generated in a liquid crystal layer and insulation layer whose electrodes are an entire source line and a counter substrate. The capacitance element **500***b* is a capacitance generated in an insulation layer whose electrodes are a source line and a gate line at the intersection of these lines. The capacitance element **500***c* is a capacitance generated in an insulation layer whose electrodes are a source line and a pixel electrode terminal parallel to the source line. The capacitance element **500***d* is a capacitance retained by a pixel transistor at the intersection of a source line and a gate line. The normal operation period T1 is further optimized by forming the capacitance elements **500***a* to **500***d* by the capacitive load **120**. The reason is explained in detail hereinafter.

The normal operation period is determined by a driving ability of a driver circuit and the degree of an output load. The driving ability of a driver circuit entirely depends on the resistance value of the resistance elements composing the DAC. The degree of the output load is, seen from the driver circuit, the capacitive load of a source line. It is considered that there are four types of capacitive loads of a source line, which are 1) a capacitance generated in a liquid crystal layer and an insulation layer wherein the electrodes are an entire source line and a counter substrate, 2) a capacitance generated in an insulation layer wherein the electrodes are a source line and a gate line in the intersection of the lines, 3) a capacitance generated in an insulation layer wherein the electrodes are a source line and a pixel electrode terminal parallel to the source line, and 4) a capacitance retained by a pixel transistor at the intersection of a source line and a gate line. Therefore, the degree of the output load is determined by the total sum of these capacitive loads, 1) to 4).

When a driver circuit is integrally formed on the array substrate, in the present state of art, a variation in resistance elements and capacitance elements therein is inevitably caused. Since the resistance elements are formed in the impurity-containing semiconductor layer, the variation of the resistance value of the resistance elements is mainly caused by the degree of impurity implantation. The variation of the capacitance value of the capacitance elements is mainly caused by the quality and thickness of each insulation layer that forms each capacitance element. The variation of the resistance value is approximately from twice to five times, which is very large, while the variation of the capacitance value is approximately from several % to 10%, which is very small in comparison with the variation of the resistance value. These variations of the resistance value and capacitance value occurs in each manufactured substrate, and therefore the most suitable value of the normal operation period for each substrate is different. Therefore, in order to find an optimal normal operation period for each substrate and to determine the low power period, it is primarily required to reflect the variation of the resistance value. On the basis of this ground, Embodiments 2-14 to 2-24 described hereinbefore are intended to optimize the normal operation period by constructing the integrator circuits with taking into account the variation of the resistance value. As mentioned above, since the variation of the resistance value is far larger than that of the capacitance value, reflecting only the variation of the resistance value will suffice when realizing the optimization of the normal operation period.

However, a variation of electric power as large as approximately from several % to 10% cannot be suppressed unless the optimization is carried out by reflecting the capacitance variation. Therefore, it is preferable that the capacitance variation be also taken into account, in order to further improve the optimization of the normal operation period. For this reason, the further improved optimization of the reduction in power consumption can be achieved by reflecting the capacitance elements as well as the resistance elements when optimizing the low power period, i.e., detecting the normal operation period.

More specifically, in this embodiment, the resistance element that is formed by the same manner as is the resistance elements in the driver circuit and the capacitance elements that uses the same insulation layers as each of the above capacitive loads are employed in constructing an R-C integrator circuit so as to reflect a resistance value per unit area in a semiconductor layer and a capacitance value per unit area in each of the above capacitances, both values being the absolute values for each manufactured substrate. The normal operation period is pseudo-detected by a delay time of the output from the R-C integrator circuit, and the low power period is automatically determined accordingly. According to this construction, in driving the capacitive load by the driver circuit, the normal operation period becomes longer (=the low power period becomes shorter) as the resistance value increases, while the driving period becomes shorter (=the low power period becomes longer) as the resistance value decreases. In the R-C integrator circuit, likewise, the output delay becomes larger as the resistance value increases, while the output delay becomes smaller as the resistance value decreases. The output delay of the R-C integrator circuit thus reflects a variation of the length of the driving period caused by the variation of the resistance value.

On the other hand, as for the variation of the capacitance value, in driving the capacitive load by the driver circuit, the driving period becomes longer (=the low power period

becomes shorter) as the capacitive load increases, while the driving period becomes shorter (=the low power period becomes longer) as the capacitive load decreases. In the R-C integrator circuit, likewise, the output delay becomes larger as the capacitive load increases, while the output delay becomes smaller as the capacitive load decreases. The output delay of the R-C integrator circuit thus reflects a variation of the length of the driving period caused by the variation of the capacitive load.

As has been described, this embodiment can further optimize the normal operation period and the low power period when compared with the embodiments wherein only the resistance elements are taken into account and the capacitance loads are not.

It is noted that one dummy source line may be provided for the capacitive loads in the R-C integrator circuit for detecting the normal operation period.

(Other Remarks)

In Embodiments 2-1 to 2-25, although the amplifier element 11 continues to operate throughout one horizontal synchronizing period, the power supply thereto can be cut off during the low power period. This achieves further reduction of power consumption.

INDUSTRIAL APPLICABILITY

As has been described thus far, according to the present invention, DACs are integrated in an array substrate of an LCD, and thereby reduction in cost can be achieved by eliminating driver ICs from the components of an LCD. Moreover, it is made possible to eliminate a manufacturing step of mounting the driver ICs onto the array substrate, and as a result, reduction in the sizes and thickness of an LCD can be also achieved.

Furthermore, according to the present invention, the reduction in power consumption can be achieved by, in a low power period, cutting off or selecting a power supply to a DAC or by fixing an input data to be a data capable of reducing an electric current flowing in the resistance elements. Furthermore, since a potential of an output terminal is retained by a capacitive load, the low power period can include a period in which the period necessary to completely change the voltage of the capacitive load connected to the output terminal is excluded.

What is claimed is:

1. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from said digital-to-analog converter circuit is outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display via a current amplifier element having an impedance conversion function wherein a voltage amplification ratio of said current amplifier element is 1;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate.

2. A driver circuit for an active matrix liquid crystal display as in claim 1, wherein said semiconductor layer is composed of a non-single crystalline material including silicon and germanium, and contains an impurity which acts as a donor or an acceptor.

3. A driver circuit for an active matrix liquid crystal display as in claim 1, wherein said semiconductor layer is a non-single crystalline silicon layer and is at least one layer of an n-type layer and a p-type layer.

4. A driver circuit for an active matrix liquid crystal display as in claim 1, wherein said digital-to-analog converter circuit is an R-2R ladder type digital-to-analog converter circuit.

5. A driver circuit for an active matrix liquid crystal display as in claim 2, wherein said digital-to-analog converter circuit is an R-2R ladder type digital-to-analog converter circuit.

6. A driver circuit for an active matrix liquid crystal display as in claim 3, wherein said digital-to-analog converter circuit is an R-2R ladder type digital-to-analog converter circuit.

7. A driver circuit for an active matrix liquid crystal display as in claim 1, wherein said digital-to-analog converter circuit is a voltage potentiometer type digital-to-analog converter circuit.

8. A driver circuit for an active matrix liquid crystal display as in claim 2, wherein said digital-to-analog converter circuit is a voltage potentiometer type digital-to-analog converter circuit.

9. A driver circuit for an active matrix liquid crystal display as in claim 3, wherein said digital-to-analog converter circuit is a voltage potentiometer type digital-to-analog converter circuit.

10. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from each of said digital-to-analog converter circuits is directly outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate.

11. A driver circuit for an active matrix liquid crystal display comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from said digital-to-analog converter circuit is outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display via a current amplifier element having an impedance conversion function wherein a voltage amplification ratio of said current amplifier element is 1, said current amplifier element being mounted on said array substrate and a remaining portion of said driver circuit excluding said current amplifier element being formed on said array substrate;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate.

12. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from said digital-to-analog converter circuit is outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display via a current amplifier element having an impedance conversion function wherein a voltage amplification ratio of said current amplifier element is 1;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, wherein said digital-to-analog converter circuit comprises:

a first digital-to-analog converter circuit section which operates in response to one of more significant bit data and lesser significant bit data of digital video input data; and

a second digital-to-analog converter circuit section which uses an output voltage as a reference voltage and operates in response to the other one of more significant bit data and lesser significant bit data of digital video input data; and

wherein one of said digital-to-analog converter circuit sections is an R-2R ladder type digital-to-analog converter circuit, and the other one of said digital-to-analog converter circuit sections is a voltage potentiometer type digital-to-analog converter circuit.

13. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from said digital-to-analog converter circuit is outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display via a current amplifier element having an impedance conversion function wherein a voltage amplification ratio of said current amplifier element is 1;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit is composed of a voltage potentiometer type digital-to-analog converter circuit comprising:

a series circuit wherein a plurality of said resistance elements are connected in series, one end of said series circuit is connected to a high voltage power supply terminal, and the other end is connected to a low voltage power supply terminal;

a first switch connected between said one end of said series circuit and said high voltage power supply terminal or between said other end of said series circuit and said low voltage supply terminal, said first switch to be turned to an ON state during said normal operation period and to be turned to an OFF state during said remaining period in response to said first switching signal; and

a group of second switches wherein a switching state of each of said second switches is controlled in response to a digital video data, and each of said second switches is connected between a connecting point of each of said resistance elements and an output terminal of said digital-to-analog converter circuit.

14. A driver circuit for an active matrix liquid crystal display as in claim 13, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

15. A driver circuit for an active matrix liquid crystal display as in claim 13, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

16. A driver circuit for an active matrix liquid crystal display as in claim 13, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

17. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from said digital-to-analog converter circuit is outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display via a current

amplifier element having an impedance conversion function wherein a voltage amplification ratio of said current amplifier element is 1;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit is composed of a voltage potentiometer type digital-to-analog converter circuit comprising:

a series circuit wherein said resistance elements are connected in series, one end of said series circuit is commonly connected to a first high voltage power supply terminal and a second high voltage power supply terminal having a lower voltage level than said first high voltage power supply, and the other end is connected to a low voltage power supply terminal;

a third switch connected between one end of said series circuit and said power supply terminals, said third switch for switching an electrical connection of said one end of said series circuit in response to said first switching signal so that said one end of said series circuit is connected to said first high voltage power supply terminal during said normal operation period and is connected to said second high voltage power supply terminal during said remaining period; and

a group of second switches wherein a switching state of each of said second switches is controlled in response to a digital video data, and each of said second switches is connected between a connecting point of each of said resistance elements and an output terminal of said digital-to-analog converter circuit.

18. A driver circuit for an active matrix liquid crystal display as in claim **17**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

19. A driver circuit for an active matrix liquid crystal display as in claim **17**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

20. A driver circuit for an active matrix liquid crystal display as in claim **17**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

21. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from said digital-to-analog converter circuit is outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display via a current amplifier element having an impedance conversion function wherein a voltage amplification ratio of said current amplifier element is 1;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit is composed of an R-2R ladder type digital-to-analog converter circuit comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value;

a group of fourth switches, each provided for each bit of digital video data, for determining an output voltage by alternatively selecting between a connecting state with a high voltage power supply terminal and a connecting state with a low voltage power supply terminal; and

a second switching signal generator circuit for generating a second switching signal to control a switching state of each of said fourth switches and outputting said second switching signal to said group of fourth switches, wherein said second switching signal generator circuit receives said first switching signal and said digital video data, and outputs a data corresponding to said digital video input data as said second switching signal

during said normal operation period, and outputs a fixed data as said second switching signal during said remaining period, said fixed data causing a current value in said resistance element network to be not more than an median current value between a minimum current value and a maximum current value in said resistance element network.

22. A driver circuit for an active matrix liquid crystal display as in claim **21**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

23. A driver circuit for an active matrix liquid crystal display as in claim **21**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

24. A driver circuit for an active matrix liquid crystal display as in claim **21**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

25. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from said digital-to-analog converter circuit is outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display via a current amplifier element having an impedance conversion function wherein a voltage amplification ratio of said current amplifier element is 1;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit is composed of an R-2R ladder type digital-to-analog converter circuit comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value;

a group of fifth switches for determining an output voltage; and

a third switching signal generator circuit for generating a third switching signal to control a switching state of each of said fifth switches and outputting said third switching signal to said group of fifth switches, said third switching signal generator circuit comprising a storage circuit for storing a fixed data causing said group of fifth switches to be OFF state, wherein said third switching signal generator circuit receives said first switching signal and digital video data, and outputs during said normal operation period a data corresponding to said digital video data as said third switching signal, and outputs during said remaining period said fixed data stored in said storage circuit as said third switching signal so as to cut off the power supply to said resistance element network.

26. A driver circuit for an active matrix liquid crystal display as in claim **25**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

27. A driver circuit for an active matrix liquid crystal display as in claim **25**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

28. A driver circuit for an active matrix liquid crystal display as in claim **25**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

29. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from said digital-to-analog converter circuit is outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display via a current amplifier element having an impedance conversion function wherein a voltage amplification ratio of said current amplifier element is 1;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit comprises:

a first digital-to-analog converter circuit section which operates in response to more significant bits of digital video input data; and

a second digital-to-analog converter circuit section, which comprises a first connecting terminal receiving a higher voltage output from said first digital-to-analog converter circuit section and a second connecting terminal receiving a lower voltage output from said first digital-to-analog converter circuit section, which employs as a reference voltage a voltage between said first connecting terminal and said second connecting terminal, and which operates in response to lesser significant bits of said digital video input data;

said first digital-to-analog converter circuit section being composed of a voltage potentiometer type digital-to-analog converter circuit and said second digital-to-analog converter circuit section being composed of an R-2R ladder type digital-to-analog converter circuit;

said first digital-to-analog converter circuit section comprising:

a series circuit wherein a plurality of said resistance elements are connected in series, one end of said series circuit is connected to a high voltage power supply terminal, and the other end is connected to a low voltage power supply terminal;

a sixth switch connected between one end of said series circuit and said high voltage power supply terminal or between the other end of said series circuit and said low voltage power supply circuit, said sixth switch to be turned to an ON state during said normal operation period and to be turned to an OFF state during said remaining period in response to said first switching signal;

a group of seventh switches each connected between a connecting point of each of said resistance elements in said series circuit and said first connecting terminal, said seventh switches controlled by said more significant bits of said digital video input data; and

a group of eighth switches each connected between a connecting point of each of said resistance elements in said series circuit and said second connecting terminal, said eighth switches controlled by said more significant bits of said digital video input data;

said second digital-to-analog converter circuit section comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value; and

a group of ninth switches for alternatively selecting between a connecting state with said first connecting terminal and a connecting state with said second connecting terminal in response to said lesser significant bits of said digital video input data;

said driver circuit, wherein:

during said normal operation period, said sixth switch is turned to the ON state, a switching state of each of said seventh switches and a switching state of each of said eighth switches are controlled corresponding to said more significant bits of said digital video input data, and a switching state of each of said ninth switches is controlled corresponding to said lesser significant bits of said digital video input data; and

during said remaining period, said sixth switch is turned to the OFF state and said electrical connection with said capacitive load is cut off by said means for cutting off said electrical connection.

30. A driver circuit for an active matrix liquid crystal display as in claim **29**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

31. A driver circuit for an active matrix liquid crystal display as in claim **29**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

32. A driver circuit for an active matrix liquid crystal display as in claim **29**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

33. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from said digital-to-analog converter circuit is outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display via a current amplifier element having an impedance conversion function wherein a voltage amplification ratio of said current amplifier element is 1;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit comprises:

a first digital-to-analog converter circuit section which operates in response to more significant bits of digital video input data; and

a second digital-to-analog converter circuit section, which comprises a first connecting terminal receiving a higher voltage output from said first digital-to-analog converter circuit section and a second connecting terminal receiving a lower voltage output from said first digital-to-analog converter circuit section, which employs as a reference voltage a voltage between said first connecting terminal and said second connecting terminal, and which operates in response to lesser significant bits of said digital video input data;

said first digital-to-analog converter circuit section being composed of a voltage potentiometer type digital-to-analog converter circuit and said second digital-to-analog converter circuit section being composed of an R-2R ladder type digital-to-analog converter circuit;

said first digital-to-analog converter circuit section comprising:

a series circuit wherein a plurality of said resistance elements are connected in series, one end of said series circuit is commonly connected to a first high voltage power supply terminal and a second high voltage power supply terminal having a lower voltage level than said first high voltage power supply terminal via a tenth switch for selecting a power supply, said tenth switch controlled by said first switching signal, and the other end of said series circuit is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of said resistance elements in said series circuit and said first connecting terminal, said seventh switches controlled by said more significant bits of said digital video input data; and

a group of eighth switches each connected between a connecting point of each of said resistance elements in said series circuit and said second connecting terminal, said eighth switches controlled by said more significant bits of said digital video input data;

said second digital-to-analog converter circuit section comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value; and

a group of ninth switches for alternatively selecting between a connecting state with said first connecting terminal and a connecting state with said second connecting terminal in response to said lesser significant bits of said digital video input data;

said driver circuit wherein:

during said normal operation period, said tenth switch is switched to said first high voltage power supply terminal, a switching state of said seventh switches and a switching state of said eighth switches are controlled corresponding to said more significant bits of said digital video input data, and a switching state of said ninth switches is controlled corresponding to said lesser significant bits of said digital video input data; and

during said remaining period, said tenth switch is switched to said second high voltage power supply terminal and said electrical connection with a capacitive load is cut off by said means for cutting off said electrical connection.

34. A driver circuit for an active matrix liquid crystal display as in claim **33**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

35. A driver circuit for an active matrix liquid crystal display as in claim **33**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

36. A driver circuit for an active matrix liquid crystal display as in claim **33**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

37. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from said digital-to-analog converter circuit is outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display via a current amplifier element having an impedance conversion function wherein a voltage amplification ratio of said current amplifier element is 1;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit comprises:

a first digital-to-analog converter circuit section which operates in response to more significant bits of digital video input data; and

a second digital-to-analog converter circuit section, which comprises a first connecting terminal receiving a higher voltage output from said first digital-to-analog converter circuit section and a second connecting terminal receiving a lower voltage output from said first digital-to-analog converter circuit section, which employs as a reference voltage a voltage between said first connecting terminal and said second connecting terminal, and which operates in response to lesser significant bits of said digital video input data;

said first digital-to-analog converter circuit section being composed of a voltage potentiometer type digital-to-analog converter circuit and said second digital-to-analog converter circuit section being composed of an R-2R ladder type digital-to-analog converter circuit;

said first digital-to-analog converter circuit section comprising:

a series circuit wherein a plurality of said resistance elements are connected in series, one end of said series circuit is connected to a high voltage power supply terminal, and the other end is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of said resistance elements in said series circuit and said first connecting terminal, said seventh switches controlled by said more significant bits of said digital video input data; and

a group of eighth switches each connected between a connecting point of each of said resistance elements in said series circuit and said second connecting terminal, said eighth switches controlled by said more significant bits of said digital video input data;

said second digital-to-analog converter circuit section comprising: an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value;

a group of ninth switches provided for each of said lesser significant bits of said digital input data for alternatively selecting between a connecting state with said first connecting terminal and a connecting state with said second connecting terminal; and

a fourth switching signal generator circuit for generating a fourth switching signal to control a switching state of each of said ninth switches and outputting said fourth switching signal to said group of ninth switches, wherein said fourth switching signal generator circuit receives said lesser significant bits of said digital video input data and said first switching signal, and outputs during said normal operation period said fourth switching signal corresponding to said lesser significant bits of said digital video data, and outputs during said remaining period a fixed data as said fourth switching signal, said fixed data causing a current value in said resistance element network to be not more than the median current value between a minimum current value and a maximum current value in said resistance element network.

38. A driver circuit for an active matrix liquid crystal display as in claim **37**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

39. A driver circuit for an active matrix liquid crystal display as in claim **37**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

40. A driver circuit for an active matrix liquid crystal display as in claim **37**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

41. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from said digital-to-analog converter circuit is outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display via a current amplifier element having an impedance conversion function wherein a voltage amplification ratio of said current amplifier element is 1;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit comprises:

a first digital-to-analog converter circuit section which operates in response to more significant bits of digital video input data; and

a second digital-to-analog converter circuit section comprising a first connecting terminal receiving a higher voltage output from said first digital-to-analog converter circuit section, an eleventh switch connected between said first connecting terminal and a power supply input line connected to said first connecting terminal, a second connecting terminal receiving a lower voltage output from said first digital-to-analog converter circuit section, and a twelfth switch connected between said second connecting terminal and a power supply input line connected to said second connecting terminal, said second digital-to-analog converter circuit section employing as a reference voltage a voltage between said first connecting terminal and said second connecting terminal, and said second digital-to-analog converter operating in response to lesser significant bit of said digital video input data;

said first digital-to-analog converter circuit section being composed of a voltage potentiometer type digital-to-analog converter circuit and said second digital-to-analog converter circuit section being composed of an R-2R ladder type digital-to-analog converter circuit;

said first digital-to-analog converter circuit section comprising:

a series circuit wherein a plurality of said resistance elements are connected in series, one end of said series circuit is connected to a high voltage power supply terminal, and the other end is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of said resistance elements in said series circuit and said first connecting terminal, said seventh switches controlled by said more significant bits of said digital video input data; and

a group of eighth switches each connected between a connecting point of each of said resistance elements in said series circuit and said second connecting terminal, said eighth switches controlled by said more significant bits of said digital video input data;

said second digital-to-analog converter circuit section further comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value; and

a group of ninth switches provided for each of said lesser significant bits of said digital input data for alternatively selecting between a connecting state with said first connecting terminal and a connecting state with said second connecting terminal;

said driver circuit wherein:

during said normal operation period, said eleventh switch and said twelfth switch are turned to an ON state and a switching state of each of said seventh switches and a switching state of each of said eighth switches are controlled corresponding to said more significant bits of said digital video input data, and a switching state of each of said ninth switches is controlled corresponding to said lesser significant bits of said digital video input data; and

during said remaining period, said eleventh switch and said twelfth switch are turned to the OFF state and said electrical connection with said capacitive load is cut off by said means for cutting off said electrical connection.

42. A driver circuit for an active matrix liquid crystal display as in claim **41**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said

output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

43. A driver circuit for an active matrix liquid crystal display as in claim **41**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

44. A driver circuit for an active matrix liquid crystal display as in claim **41**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

45. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from said digital-to-analog converter circuit is outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display via a current amplifier element having an impedance conversion function wherein a voltage amplification ratio of said current amplifier element is 1;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit comprises:

a first digital-to-analog converter circuit section which operates in response to more significant bits of digital video input data; and

a second digital-to-analog converter circuit section, which comprises a first connecting terminal receiving a higher voltage output from said first digital-to-analog converter circuit section and a second connecting terminal receiving a lower voltage output from said first digital-to-analog converter circuit section, which employs as a reference voltage a voltage between said first connecting terminal and said second connecting terminal, and which operates in response to lesser significant bits of said digital video input data;

said first digital-to-analog converter circuit section being composed of a voltage potentiometer type digital-to-analog converter circuit and said second digital-to-analog converter circuit section being composed of an R-2R ladder type digital-to-analog converter circuit;

said first digital-to-analog converter circuit section comprising:

a series circuit wherein a plurality of said resistance elements are connected in series, one end of said series circuit is commonly connected to a first high voltage power supply terminal and a second high voltage power supply terminal having a lower voltage level than said first high voltage power supply terminal via a tenth switch for selecting a power supply, and the other end of said series circuit is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of said resistance elements in said series circuit and said first connecting terminal, said seventh switches controlled by said more significant bits of said digital video input data; and

a group of eighth switches each connected between a connecting point of each of said resistance elements in said series circuit and said second connecting terminal, said eighth switches controlled by said more significant bits of said digital video input data;

said second digital-to-analog converter circuit section comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value;

a group of ninth switches provided for each of said lesser significant bits of said digital input data for alternatively selecting between a connecting state with said first connecting terminal and a connecting state with said second connecting terminal; and

a fourth switching signal generator circuit for generating a fourth switching signal to control a switching state of each of said ninth switches and outputting said fourth switching signal to said group of ninth switches, wherein said fourth switching signal generator circuit receives said lesser significant bits of said digital video input data and said first switching signal, and outputs during said normal operation period said fourth switching signal corresponding to said lesser significant bits of said digital video data, and outputs during said remaining period a fixed data as said fourth switching signal, said fixed data causing a current value in said resistance element network to be not more than the median current value between a minimum current value

and a maximum current value in said resistance element network;

said driver circuit wherein:

during said normal operation period, said tenth switch is switched to said first high voltage power supply terminal, a switching state of said seventh switches and a switching state of said eighth switches are controlled corresponding to said more significant bits of said digital video input data, and a switching state of said ninth switches is controlled corresponding to said lesser significant bits of said digital video input data; and

during said remaining period, said tenth switch is switched to said second high voltage power supply terminal, said ninth switches are switched corresponding to said fixed input data, and said electrical connection with said capacitive load is cut off by said means for cutting off said electrical connection.

46. A driver circuit for an active matrix liquid crystal display as in claim **45**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

47. A driver circuit for an active matrix liquid crystal display as in claim **45**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

48. A driver circuit for an active matrix liquid crystal display as in claim **45**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

49. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from said digital-to-analog converter circuit is outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display via a current amplifier element having an impedance conversion function wherein a voltage amplification ratio of said current amplifier element is 1;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit comprises:

a first digital-to-analog converter circuit section which operates in response to more significant bits of digital video input data; and

a second digital-to-analog converter circuit section comprising a first connecting terminal receiving a higher voltage output from said first digital-to-analog converter circuit section, an eleventh switch connected between said first connecting terminal and a power supply input line connected to said first connecting terminal, a second connecting terminal receiving a lower voltage output from said first digital-to-analog converter circuit section, and a twelfth switch connected between said second connecting terminal and a power supply input line connected to said second connecting terminal, said second digital-to-analog converter circuit section employing as a reference voltage a voltage between said first connecting terminal and said second connecting terminal, and said second digital-to-analog converter operating in response to lesser significant bit of said digital video input data;

said first digital-to-analog converter circuit section being composed of a voltage potentiometer type digital-to-analog converter circuit and said second digital-to-analog converter circuit section being composed of an R-2R ladder type digital-to-analog converter circuit;

said first digital-to-analog converter circuit section comprising:

a series circuit wherein a plurality of said resistance elements are connected in series, one end of said series circuit is commonly connected to a first high voltage power supply terminal and a second high voltage power supply terminal having a lower voltage level than said first high voltage power supply terminal via a tenth switch for selecting a power supply, and the other end of said series circuit is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of said resistance elements in said series circuit and said first connecting terminal, said seventh switches controlled by said more significant bits of said digital video input data; and

a group of eighth switches each connected between a connecting point of each of said resistance elements in said series circuit and said second connecting terminal, said eighth switches controlled by said more significant bits of said digital video input data;

said second digital-to-analog converter circuit section comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value; and

a group of ninth switches provided for each of said lesser significant bits of said digital input data for alternatively selecting between a connecting state with said first connecting terminal and a connecting state with said second connecting terminal;

said driver circuit wherein:

during said normal operation period, said tenth switch is switched to said first high voltage power supply terminal, a switching state of said seventh switches and a switching state of said eighth switches are controlled corresponding to said more significant bits of said digital video input data and a switching state of said ninth switches is controlled corresponding to said lesser significant bits of said digital video input data; and

during said remaining period, said tenth switch is switched to said second high voltage power supply terminal, said eleventh switch and said twelfth switch are turned to the OFF state and said electrical connection with said capacitive load is cut off by said means for cutting off said electrical connection.

50. A driver circuit for an active matrix liquid crystal display as in claim **49**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

51. A driver circuit for an active matrix liquid crystal display as in claim **49**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

52. A driver circuit for an active matrix liquid crystal display as in claim **49**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

53. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from said digital-to-analog converter circuit is outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display via a current amplifier element having an impedance conversion function wherein a voltage amplification ratio of said current amplifier element is 1;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a fifth switching signal generator circuit which receives a predetermined reference signal and generates a fifth switching signal for selecting one of the modes between a precharge period mode for a precharge which is carried out prior to writing video data into a source line and a remaining period mode excluding said precharge period mode;

wherein said digital-to-analog converter circuit is composed of an R-2R ladder type digital-to-analog converter circuit comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value;

a group of fourth switches, each provided for each bit of digital video data, for determining an output voltage by alternatively selecting between a connecting state with a high voltage power supply terminal and a connecting state with a low voltage power supply terminal; and

a sixth switching signal generator circuit for generating a sixth switching signal to control a switching state of each of said fourth switches and outputting said sixth switching signal to said group of fourth switches, wherein said sixth switching signal generator circuit receives said fifth switching signal and digital video data, and outputs a data corresponding to said digital video data as said sixth switching signal during said remaining period, and outputs a fixed data as said sixth switching signal during said precharge period, said fixed data causing a current value in said resistance element network to be not more than an median current value between a minimum current value and a maximum current value in said resistance element network.

54. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from said digital-to-analog converter circuit is outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display via a current amplifier element having an impedance conversion function wherein a voltage amplification ratio of said current amplifier element is 1;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a fifth switching signal generator circuit which receives a predetermined reference signal and generates a fifth switching signal for selecting one of the modes between a precharge period mode for a precharge which is carried out prior to writing video data into a source line and a remaining period mode excluding said precharge period mode;

wherein said digital-to-analog converter circuit comprises:

a first digital-to-analog converter circuit section which operates in response to more significant bits of digital video input data; and

a second digital-to-analog converter circuit section, which comprises a first connecting terminal receiving a higher voltage output from said first digital-to-analog converter circuit section and a second connecting terminal receiving a lower voltage output from said first digital-to-analog converter circuit section, which employs as a reference voltage a voltage between said first connecting terminal and said second connecting terminal, and which operates in response to lesser significant bits of said digital video input data;

said first digital-to-analog converter circuit section being composed of a voltage potentiometer type digital-to-analog converter circuit and said second digital-to-analog converter circuit section being composed of an R-2R ladder type digital-to-analog converter circuit;

said first digital-to-analog converter circuit section comprising: a series circuit wherein a plurality of said resistance elements are connected in series, one end of said series circuit is commonly connected to a first high voltage power supply terminal and a second high voltage power supply terminal having a lower voltage level than said first high voltage power supply terminal via a tenth switch for selecting a power supply, and the other end of said series circuit is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of said resistance elements in said series circuit and said first connecting terminal, said seventh switches controlled by said more significant bits of said digital video input data; and

a group of eighth switches each connected between a connecting point of each of said resistance elements in said series circuit and said second connecting terminal, said eighth switches controlled by said more significant bits of said digital video input data;

said second digital-to-analog converter circuit section comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value;

a group of ninth switches provided for each of said lesser significant bits of said digital input data for alternatively selecting between a connecting state with said first connecting terminal and a connecting state with said second connecting terminal; and

a fourth switching signal generator circuit for generating a seventh switching signal to control a switching state of each of said ninth switches and outputting said seventh switching signal to said group of ninth switches, wherein said seventh switching signal generator circuit receives said fifth switching signal and said lesser significant bits of said digital video data, and outputs a data corresponding to said lesser significant bits of said digital video input data as said seventh switching signal during said remaining period, and outputs a fixed data as said seventh switching signal during said precharge period, said fixed data causing a current value in said resistance element network to be not more than an median current value between a minimum current value and a maximum current value in said resistance element network;

said driver circuit wherein:

during said remaining period, said tenth switch is switched to said first high voltage power supply terminal, a switching state of said seventh switches and a switching state of said eighth switches are controlled corresponding to said more significant bits of said digital video input data, and a switching state of said ninth switches is controlled corresponding to said lesser significant bits of said digital video input data; and

during said precharge period, said tenth switch is switched to said second high voltage power supply terminal, said ninth switches are switched corresponding to said fixed input data, and said electrical connection with said capacitive load is cut off by said means for cutting off said electrical connection.

55. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from each of said digital-to-analog converter circuits is directly outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit is composed of a voltage potentiometer type digital-to-analog converter circuit comprising:

a series circuit wherein a plurality of said resistance elements are connected in series, one end of said series circuit is connected to a high voltage power supply terminal, and the other end is connected to a low voltage power supply terminal;

a first switch connected between said one end of said series circuit and said high voltage power supply terminal or between said other end of said series circuit and said low voltage supply terminal, said first switch to be turned to an ON state during said normal operation period and to be turned to an OFF state during said remaining period in response to said first switching signal; and

a group of second switches wherein a switching state of each of said second switches is controlled in response to a digital video data, and each of said second switches is connected between a connecting point of each of said resistance elements and an output terminal of said digital-to-analog converter circuit.

56. A driver circuit for an active matrix liquid crystal display as in claim **55**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

57. A driver circuit for an active matrix liquid crystal display as in claim **55**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

58. A driver circuit for an active matrix liquid crystal display as in claim **55**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

59. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from each of said digital-to-analog converter circuits is directly outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit is composed of a voltage potentiometer type digital-to-analog converter circuit comprising:

a series circuit wherein said resistance elements are connected in series, one end of said series circuit is commonly connected to a first high voltage power supply terminal and a second high voltage power supply terminal having a lower voltage level than said first high voltage power supply, and the other end is connected to a low voltage power supply terminal;

a third switch connected between one end of said series circuit and said power supply terminals, said third switch for switching an electrical connection of said one end of said series circuit in response to said first switching signal so that said one end of said series circuit is connected to said first high voltage power supply terminal during said normal operation period and is connected to said second high voltage power supply terminal during said remaining period; and

a group of second switches wherein a switching state of each of said second switches is controlled in response to a digital video data, and each of said second switches is connected between a connecting point of each of said resistance elements and an output terminal of said digital-to-analog converter circuit.

60. A driver circuit for an active matrix liquid crystal display as in claim **59**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

61. A driver circuit for an active matrix liquid crystal display as in claim **59**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

62. A driver circuit for an active matrix liquid crystal display as in claim 59, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

63. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from each of said digital-to-analog converter circuits is directly outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit is composed of an R-2R ladder type digital-to-analog converter circuit comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value;

a group of fourth switches, each provided for each bit of digital video data, for determining an output voltage by alternatively selecting between a connecting state with a high voltage power supply terminal and a connecting state with a low voltage power supply terminal; and

a second switching signal generator circuit for generating a second switching signal to control a switching state of each of said fourth switches and outputting said second switching signal to said group of fourth switches, wherein said second switching signal generator circuit receives said first switching signal and said digital video data, and outputs a data corresponding to said digital video input data as said second switching signal during said normal operation period, and outputs a fixed data as said second switching signal during said remaining period, said fixed data causing a current value in said resistance element network to be not more than an median current value between a minimum current value and a maximum current value in said resistance element network.

64. A driver circuit for an active matrix liquid crystal display as in claim 63, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

65. A driver circuit for an active matrix liquid crystal display as in claim 63, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

66. A driver circuit for an active matrix liquid crystal display as in claim 63, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

67. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from each of said digital-to-analog converter circuits is directly outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first

switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit is composed of an R-2R ladder type digital-to-analog converter circuit comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value;

a group of fifth switches for determining an output voltage; and

a third switching signal generator circuit for generating a third switching signal to control a switching state of each of said fifth switches and outputting said third switching signal to said group of fifth switches, said third switching signal generator circuit comprising a storage circuit for storing a fixed data causing said group of fifth switches to be OFF state, wherein said third switching signal generator circuit receives said first switching signal and digital video data, and outputs during said normal operation period a data corresponding to said digital video data as said third switching signal, and outputs during said remaining period said fixed data stored in said storage circuit as said third switching signal so as to cut off the power supply to said resistance element network.

68. A driver circuit for an active matrix liquid crystal display as in claim **67**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

69. A driver circuit for an active matrix liquid crystal display as in claim **67**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

70. A driver circuit for an active matrix liquid crystal display as in claim **67**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

71. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from each of said digital-to-analog converter circuits is directly outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit comprises:

a first digital-to-analog converter circuit section which operates in response to more significant bits of digital video input data; and

a second digital-to-analog converter circuit section, which comprises a first connecting terminal receiving a higher voltage output from said first digital-to-analog converter circuit section and a second connecting terminal receiving a lower voltage output from said first digital-to-analog converter circuit section, which employs as a reference voltage a voltage between said first connecting terminal and said second connecting terminal, and which operates in response to lesser significant bits of said digital video input data;

said first digital-to-analog converter circuit section being composed of a voltage potentiometer type digital-to-analog converter circuit and said second digital-to-analog converter circuit section being composed of an R-2R ladder type digital-to-analog converter circuit;

said first digital-to-analog converter circuit section comprising:

a series circuit wherein a plurality of said resistance elements are connected in series, one end of said series circuit is connected to a high voltage power supply terminal, and the other end is connected to a low voltage power supply terminal;

a sixth switch connected between one end of said series circuit and said high voltage power supply terminal or between the other end of said series circuit and said low voltage power supply circuit, said sixth switch to be turned to an ON state during said normal operation

period and to be turned to an OFF state during said remaining period in response to said first switching signal;

a group of seventh switches each connected between a connecting point of each of said resistance elements in said series circuit and said first connecting terminal, said seventh switches controlled by said more significant bits of said digital video input data; and

a group of eighth switches each connected between a connecting point of each of said resistance elements in said series circuit and said second connecting terminal, said eighth switches controlled by said more significant bits of said digital video input data;

said second digital-to-analog converter circuit section comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value; and

a group of ninth switches for alternatively selecting between a connecting state with said first connecting terminal and a connecting state with said second connecting terminal in response to said lesser significant bits of said digital video input data;

said driver circuit, wherein:

during said normal operation period, said sixth switch is turned to the ON state, a switching state of each of said seventh switches and a switching state of each of said eighth switches are controlled corresponding to said more significant bits of said digital video input data, and a switching state of each of said ninth switches is controlled corresponding to said lesser significant bits of said digital video input data; and

during said remaining period, said sixth switch is turned to the OFF state and said electrical connection with said capacitive load is cut off by said means for cutting off said electrical connection.

72. A driver circuit for an active matrix liquid crystal display as in claim **71**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

73. A driver circuit for an active matrix liquid crystal display as in claim **71**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

74. A driver circuit for an active matrix liquid crystal display as in claim **71**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

75. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from each of said digital-to-analog converter circuits is directly outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit comprises:

a first digital-to-analog converter circuit section which operates in response to more significant bits of digital video input data; and

a second digital-to-analog converter circuit section, which comprises a first connecting terminal receiving a higher voltage output from said first digital-to-analog converter circuit section and a second connecting terminal receiving a lower voltage output from said first digital-to-analog converter circuit section, which employs as a reference voltage a voltage between said first connecting terminal and said second connecting terminal, and which operates in response to lesser significant bits of said digital video input data;

said first digital-to-analog converter circuit section being composed of a voltage potentiometer type digital-to-analog converter circuit and said second digital-to-analog converter circuit section being composed of an R-2R ladder type digital-to-analog converter circuit;

said first digital-to-analog converter circuit section comprising:

a series circuit wherein a plurality of said resistance elements are connected in series, one end of said series circuit is commonly connected to a first high voltage

power supply terminal and a second high voltage power supply terminal having a lower voltage level than said first high voltage power supply terminal via a tenth switch for selecting a power supply, said tenth switch controlled by said first switching signal, and the other end of said series circuit is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of said resistance elements in said series circuit and said first connecting terminal, said seventh switches controlled by said more significant bits of said digital video input data; and

a group of eighth switches each connected between a connecting point of each of said resistance elements in said series circuit and said second connecting terminal, said eighth switches controlled by said more significant bits of said digital video input data;

said second digital-to-analog converter circuit section comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value; and

a group of ninth switches for alternatively selecting between a connecting state with said first connecting terminal and a connecting state with said second connecting terminal in response to said lesser significant bits of said digital video input data;

said driver circuit wherein:

during said normal operation period, said tenth switch is switched to said first high voltage power supply terminal, a switching state of said seventh switches and a switching state of said eighth switches are controlled corresponding to said more significant bits of said digital video input data, and a switching state of said ninth switches is controlled corresponding to said lesser significant bits of said digital video input data; and

during said remaining period, said tenth switch is switched to said second high voltage power supply terminal and said electrical connection with a capacitive load is cut off by said means for cutting off said electrical connection.

76. A driver circuit for an active matrix liquid crystal display as in claim **75**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

77. A driver circuit for an active matrix liquid crystal display as in claim **75**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

78. A driver circuit for an active matrix liquid crystal display as in claim **75**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

79. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from each of said digital-to-analog converter circuits is directly outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit comprises:

a first digital-to-analog converter circuit section which operates in response to more significant bits of digital video input data; and

a second digital-to-analog converter circuit section, which comprises a first connecting terminal receiving a higher voltage output from said first digital-to-analog converter circuit section and a second connecting terminal receiving a lower voltage output from said first digital-to-analog converter circuit section, which employs as a reference voltage a voltage between said first connecting terminal and said second connecting terminal, and which operates in response to lesser significant bits of said digital video input data;

said first digital-to-analog converter circuit section being composed of a voltage potentiometer type digital-to-analog converter circuit and said second digital-to-analog converter circuit section being composed of an R-2R ladder type digital-to-analog converter circuit;

said first digital-to-analog converter circuit section comprising:

a series circuit wherein a plurality of said resistance elements are connected in series, one end of said series circuit is connected to a high voltage power supply terminal, and the other end is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of said resistance elements in said series circuit and said first connecting terminal, said seventh switches controlled by said more significant bits of said digital video input data; and

a group of eighth switches each connected between a connecting point of each of said resistance elements in said series circuit and said second connecting terminal, said eighth switches controlled by said more significant bits of said digital video input data;

said second digital-to-analog converter circuit section comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value;

a group of ninth switches provided for each of said lesser significant bits of said digital input data for alternatively selecting between a connecting state with said first connecting terminal and a connecting state with said second connecting terminal; and

a fourth switching signal generator circuit for generating a fourth switching signal to control a switching state of each of said ninth switches and outputting said fourth switching signal to said group of ninth switches, wherein said fourth switching signal generator circuit receives said lesser significant bits of said digital video input data and said first switching signal, and outputs during said normal operation period said fourth switching signal corresponding to said lesser significant bits of said digital video data, and outputs during said remaining period a fixed data as said fourth switching signal, said fixed data causing a current value in said resistance element network to be not more than the median current value between a minimum current value and a maximum current value in said resistance element network.

80. A driver circuit for an active matrix liquid crystal display as in claim **79**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

81. A driver circuit for an active matrix liquid crystal display as in claim **79**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

82. A driver circuit for an active matrix liquid crystal display as in claim **79**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

83. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from each of said digital-to-analog converter circuits is directly outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit comprises:

a first digital-to-analog converter circuit section which operates in response to more significant bits of digital video input data; and

a second digital-to-analog converter circuit section comprising a first connecting terminal receiving a higher voltage output from said first digital-to-analog converter circuit section, an eleventh switch connected between said first connecting terminal and a power supply input line connected to said first connecting terminal, a second connecting terminal receiving a lower voltage output from said first digital-to-analog converter circuit section, and a twelfth switch connected between said second connecting terminal and a power supply input line connected to said second connecting terminal, said second digital-to-analog converter circuit section employing as a reference voltage a voltage between said first connecting terminal and said second connecting terminal, and said second digital-to-analog converter operating in response to lesser significant bit of said digital video input data;

said first digital-to-analog converter circuit section being composed of a voltage potentiometer type digital-to-analog converter circuit and said second digital-to-analog converter circuit section being composed of an R-2R ladder type digital-to-analog converter circuit;

said first digital-to-analog converter circuit section comprising:

a series circuit wherein a plurality of said resistance elements are connected in series, one end of said series circuit is connected to a high voltage power supply terminal, and the other end is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of said resistance elements in said series circuit and said first connecting terminal, said seventh switches controlled by said more significant bits of said digital video input data; and

a group of eighth switches each connected between a connecting point of each of said resistance elements in said series circuit and said second connecting terminal, said eighth switches controlled by said more significant bits of said digital video input data;

said second digital-to-analog converter circuit section further comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value; and

a group of ninth switches provided for each of said lesser significant bits of said digital input data for alternatively selecting between a connecting state with said first connecting terminal and a connecting state with said second connecting terminal;

said driver circuit wherein:

during said normal operation period, said eleventh switch and said twelfth switch are turned to an ON state and a switching state of each of said seventh switches and a switching state of each of said eighth switches are controlled corresponding to said more significant bits of said digital video input data, and a switching state of each of said ninth switches is controlled corresponding to said lesser significant bits of said digital video input data; and

during said remaining period, said eleventh switch and said twelfth switch are turned to the OFF state and said electrical connection with said capacitive load is cut off by said means for cutting off said electrical connection.

84. A driver circuit for an active matrix liquid crystal display as in claim **83**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

85. A driver circuit for an active matrix liquid crystal display as in claim **83**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

86. A driver circuit for an active matrix liquid crystal display as in claim **83**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

87. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from each of said digital-to-analog converter circuits is directly outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit comprises:

a first digital-to-analog converter circuit section which operates in response to more significant bits of digital video input data; and

a second digital-to-analog converter circuit section, which comprises a first connecting terminal receiving a higher voltage output from said first digital-to-analog converter circuit section and a second connecting terminal receiving a lower voltage output from said first digital-to-analog converter circuit section, which employs as a reference voltage a voltage between said first connecting terminal and said second connecting terminal, and which operates in response to lesser significant bits of said digital video input data;

said first digital-to-analog converter circuit section being composed of a voltage potentiometer type digital-to-analog converter circuit and said second digital-to-analog converter circuit section being composed of an R-2R ladder type digital-to-analog converter circuit;

said first digital-to-analog converter circuit section comprising:

a series circuit wherein a plurality of said resistance elements are connected in series, one end of said series circuit is commonly connected to a first high voltage power supply terminal and a second high voltage power supply terminal having a lower voltage level than said first high voltage power supply terminal via a tenth switch for selecting a power supply, and the other end of said series circuit is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of said resistance elements in said series circuit and said first connecting terminal, said seventh switches controlled by said more significant bits of said digital video input data; and

a group of eighth switches each connected between a connecting point of each of said resistance elements in said series circuit and said second connecting terminal, said eighth switches controlled by said more significant bits of said digital video input data;

said second digital-to-analog converter circuit section comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value;

a group of ninth switches provided for each of said lesser significant bits of said digital input data for alternatively selecting between a connecting state with said first connecting terminal and a connecting state with said second connecting terminal; and

a fourth switching signal generator circuit for generating a fourth switching signal to control a switching state of each of said ninth switches and outputting said fourth switching signal to said group of ninth switches, wherein said fourth switching signal generator circuit receives said lesser significant bits of said digital video input data and said first switching signal, and outputs during said normal operation period said fourth switching signal corresponding to said lesser significant bits of said digital video data, and outputs during said remaining period a fixed data as said fourth switching signal, said fixed data causing a current value in said resistance element network to be not more than the median current value between a minimum current value and a maximum current value in said resistance element network;

said driver circuit wherein:

during said normal operation period, said tenth switch is switched to said first high voltage power supply terminal, a switching state of said seventh switches and a switching state of said eighth switches are controlled corresponding to said more significant bits of said digital video input data, and a switching state of said ninth switches is controlled corresponding to said lesser significant bits of said digital video input data; and

during said remaining period, said tenth switch is switched to said second high voltage power supply terminal, said ninth switches are switched corresponding to said fixed input data, and said electrical connection with said capacitive load is cut off by said means for cutting off said electrical connection.

88. A driver circuit for an active matrix liquid crystal display as in claim **87**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

89. A driver circuit for an active matrix liquid crystal display as in claim **87**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

90. A driver circuit for an active matrix liquid crystal display as in claim **87**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

91. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from each of said digital-to-analog converter circuits is directly outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a first switching signal generator circuit which receives a predetermined reference signal and generates a first

switching signal for alternatively selecting between a normal operation period and a remaining period; and

means for cutting off an electrical connection between said driver circuit and a capacitive load connected to a source line only during said remaining period in response to said first switching signal;

wherein said digital-to-analog converter circuit comprises:

a first digital-to-analog converter circuit section which operates in response to more significant bits of digital video input data; and

a second digital-to-analog converter circuit section comprising a first connecting terminal receiving a higher voltage output from said first digital-to-analog converter circuit section, an eleventh switch connected between said first connecting terminal and a power supply input line connected to said first connecting terminal, a second connecting terminal receiving a lower voltage output from said first digital-to-analog converter circuit section, and a twelfth switch connected between said second connecting terminal and a power supply input line connected to said second connecting terminal, said second digital-to-analog converter circuit section employing as a reference voltage a voltage between said first connecting terminal and said second connecting terminal, and said second digital-to-analog converter operating in response to lesser significant bit of said digital video input data;

said first digital-to-analog converter circuit section being composed of a voltage potentiometer type digital-to-analog converter circuit and said second digital-to-analog converter circuit section being composed of an R-2R ladder type digital-to-analog converter circuit;

said first digital-to-analog converter circuit section comprising:

a series circuit wherein a plurality of said resistance elements are connected in series, one end of said series circuit is commonly connected to a first high voltage power supply terminal and a second high voltage power supply terminal having a lower voltage level than said first high voltage power supply terminal via a tenth switch for selecting a power supply, and the other end of said series circuit is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of said resistance elements in said series circuit and said first connecting terminal, said seventh switches controlled by said more significant bits of said digital video input data; and

a group of eighth switches each connected between a connecting point of each of said resistance elements in said series circuit and said second connecting terminal, said eighth switches controlled by said more significant bits of said digital video input data;

said second digital-to-analog converter circuit section comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value; and

a group of ninth switches provided for each of said lesser significant bits of said digital input data for alternatively selecting between a connecting state with said first connecting terminal and a connecting state with said second connecting terminal;

said driver circuit wherein:

during said normal operation period, said tenth switch is switched to said first high voltage power supply terminal, a switching state of said seventh switches and a switching state of said eighth switches are controlled corresponding to said more significant bits of said digital video input data and a switching state of said ninth switches is controlled corresponding to said lesser significant bits of said digital video input data; and

during said remaining period, said tenth switch is switched to said second high voltage power supply terminal, said eleventh switch and said twelfth switch are turned to the OFF state and said electrical connection with said capacitive load is cut off by said means for cutting off said electrical connection.

92. A driver circuit for an active matrix liquid crystal display as in claim **91**, wherein said means for cutting off said electrical connection between said driver circuit and said capacitive load connected to said source line is such an output switch provided on an output side of said driver circuit that, in response to said first switching signal, said output switch is turned to an ON state during said normal operation period, and is turned to an OFF state during said remaining period so as to cut off said electrical connection.

93. A driver circuit for an active matrix liquid crystal display as in claim **91**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitor element, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

94. A driver circuit for an active matrix liquid crystal display as in claim **91**, wherein said first switching signal generator circuit receives a horizontal synchronizing signal, generates a first switching signal from said horizontal synchronizing signal, and outputs said first switching signal to said digital-to-analog converter circuit:

said first switching signal generator circuit comprising:

a delay circuit comprising an integrator circuit composed of a resistance element and a capacitance element composed of a capacitive load connected to a source line, said delay circuit for delaying said horizontal synchronizing signal for a predetermined delay time determined by a resistance value of said resistance element in said integrator circuit and a capacitance value of said capacitance element in said integrator circuit; and

a logic circuit wherein an output from said delay circuit and said horizontal synchronizing signal are ANDed together to output a resultant signal as said first switching signal.

95. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from each of said digital-to-analog converter circuits is directly outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a fifth switching signal generator circuit which receives a predetermined reference signal and generates a fifth switching signal for selecting one of the modes between a precharge period mode for a precharge which is carried out prior to writing video data into a source line and a remaining period mode excluding said precharge period mode;

wherein said digital-to-analog converter circuit is composed of an R-2R ladder type digital-to-analog converter circuit comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value;

a group of fourth switches, each provided for each bit of digital video data, for determining an output voltage by alternatively selecting between a connecting state with a high voltage power supply terminal and a connecting state with a low voltage power supply terminal; and

a sixth switching signal generator circuit for generating a sixth switching signal to control a switching state of each of said fourth switches and outputting said sixth switching signal to said group of fourth switches, wherein said sixth switching signal generator circuit receives said fifth switching signal and digital video data, and outputs a data corresponding to said digital video data as said sixth switching signal during said remaining period, and outputs a fixed data as said sixth switching signal during said precharge period, said fixed data causing a current value in said resistance element network to be not more than an median current value between a minimum current value and a maximum current value in said resistance element network.

96. A driver circuit for an active matrix liquid crystal display formed on an array substrate of said liquid crystal display, comprising:

a resistive dividing type digital-to-analog converter circuit, comprising a plurality of resistance elements and a plurality of switches related to said resistance elements;

said driver circuit constructed so that an output signal from each of said digital-to-analog converter circuits is directly outputted as a driving voltage for a liquid crystal display portion of said liquid crystal display;

said driver circuit characterized in that said resistance elements are composed of an impurity-containing semiconductor layer formed on said array substrate, and further comprising:

a fifth switching signal generator circuit which receives a predetermined reference signal and generates a fifth switching signal for selecting one of the modes between a precharge period mode for a precharge which is carried out prior to writing video data into a source line and a remaining period mode excluding said precharge period mode;

wherein said digital-to-analog converter circuit comprises:

a first digital-to-analog converter circuit section which operates in response to more significant bits of digital video input data; and

a second digital-to-analog converter circuit section, which comprises a first connecting terminal receiving a higher voltage output from said first digital-to-analog converter circuit section and a second connecting terminal receiving a lower voltage output from said first digital-to-analog converter circuit section, which employs as a reference voltage a voltage between said first connecting terminal and said second connecting terminal, and which operates in response to lesser significant bits of said digital video input data;

said first digital-to-analog converter circuit section being composed of a voltage potentiometer type digital-to-analog converter circuit and said second digital-to-analog converter circuit section being composed of an R-2R ladder type digital-to-analog converter circuit;

said first digital-to-analog converter circuit section comprising:

a series circuit wherein a plurality of said resistance elements are connected in series, one end of said series circuit is commonly connected to a first high voltage power supply terminal and a second high voltage power supply terminal having a lower voltage level than said first high voltage power supply terminal via a tenth switch for selecting a power supply, and the other end of said series circuit is connected to a low voltage power supply terminal;

a group of seventh switches each connected between a connecting point of each of said resistance elements in said series circuit and said first connecting terminal, said seventh switches controlled by said more significant bits of said digital video input data; and

a group of eighth switches each connected between a connecting point of each of said resistance elements in said series circuit and said second connecting terminal, said eighth switches controlled by said more significant bits of said digital video input data;

said second digital-to-analog converter circuit section comprising:

an R-2R ladder resistance element network composed of two types of said resistance elements, each type having a different resistance value;

a group of ninth switches provided for each of said lesser significant bits of said digital input data for alternatively selecting between a connecting state with said first connecting terminal and a connecting state with said second connecting terminal; and

a fourth switching signal generator circuit for generating a seventh switching signal to control a switching state of each of said ninth switches and outputting said seventh switching signal to said group of ninth switches, wherein said seventh switching signal generator circuit receives said fifth switching signal and said lesser significant bits of said digital video data, and outputs a data corresponding to said lesser significant bits of said digital video input data as said seventh switching signal during said remaining period, and outputs a fixed data as said seventh switching signal during said precharge period, said fixed data causing a

current value in said resistance element network to be not more than an-median current value between a minimum current value and a maximum current value in said resistance element network;

said driver circuit wherein:

during said remaining period, said tenth switch is switched to said first high voltage power supply terminal, a switching state of said seventh switches and a switching state of said eighth switches are controlled corresponding to said more significant bits of said digital video input data, and a switching state of said ninth switches is controlled corresponding to said lesser significant bits of said digital video input data; and

during said precharge period, said tenth switch is switched to said second high voltage power supply terminal, said ninth switches are switched corresponding to said fixed input data, and said electrical connection with said capacitive load is cut off by said means for cutting off said electrical connection.

* * * * *

US006384806B1

(12) **United States Patent**
Matsueda et al.

(10) **Patent No.: US 6,384,806 B1**
(45) **Date of Patent: May 7, 2002**

(54) **DIGITAL DRIVER CIRCUIT FOR ELECTRO-OPTICAL DEVICE AND ELECTRO-OPTICAL DEVICE HAVING THE DIGITAL DRIVER CIRCUIT**

(75) Inventors: **Yojiro Matsueda**, Chino (JP); **Michael J. Quinn**, London (GB)

(73) Assignee: **Seiko Epson Corporation**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/271,335**

(22) Filed: **Mar. 18, 1999**

(30) **Foreign Application Priority Data**

Mar. 24, 1998 (JP) 10-076336

(51) **Int. Cl.**[7] **G09G 3/36**
(52) **U.S. Cl.** **345/89**; 345/95; 345/691
(58) **Field of Search** 345/147, 148, 345/89, 92, 94–95, 208–209, 99, 691–693

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,317,401	A	* 5/1994	Dupont et al.	348/678
5,337,070	A	* 8/1994	Kitajima et al.	345/211
5,477,234	A	* 12/1995	Suzuki et al.	345/95
5,489,918	A	* 2/1996	Moiser	345/89
5,784,041	A	* 7/1998	Okada et al.	345/89
6,137,462	A	* 10/2000	Kim	345/94

FOREIGN PATENT DOCUMENTS

JP	A-2-295390	12/1990
JP	A-5-100629	4/1993
JP	A-5-100630	4/1993
JP	A-6-180562	6/1994
JP	A-9-54309	2/1997
JP	A-9-244588	9/1997

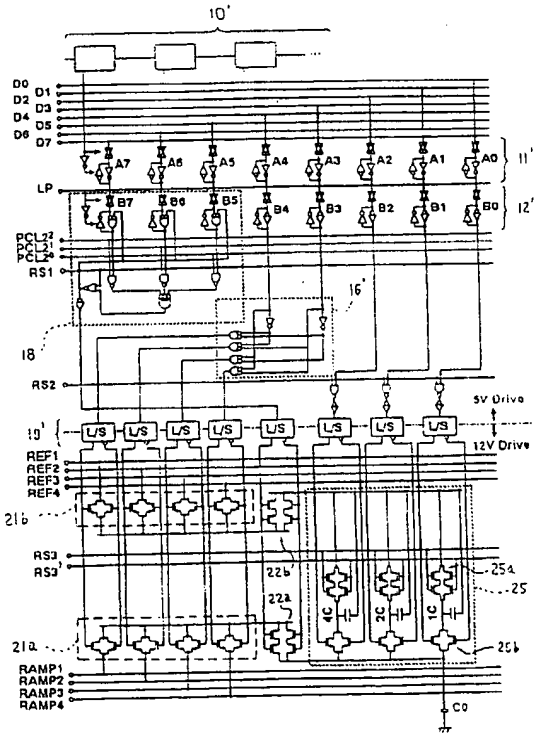
* cited by examiner

Primary Examiner—Lun-Yi Lao
(74) *Attorney, Agent, or Firm*—Oliff & Berridge, PLC

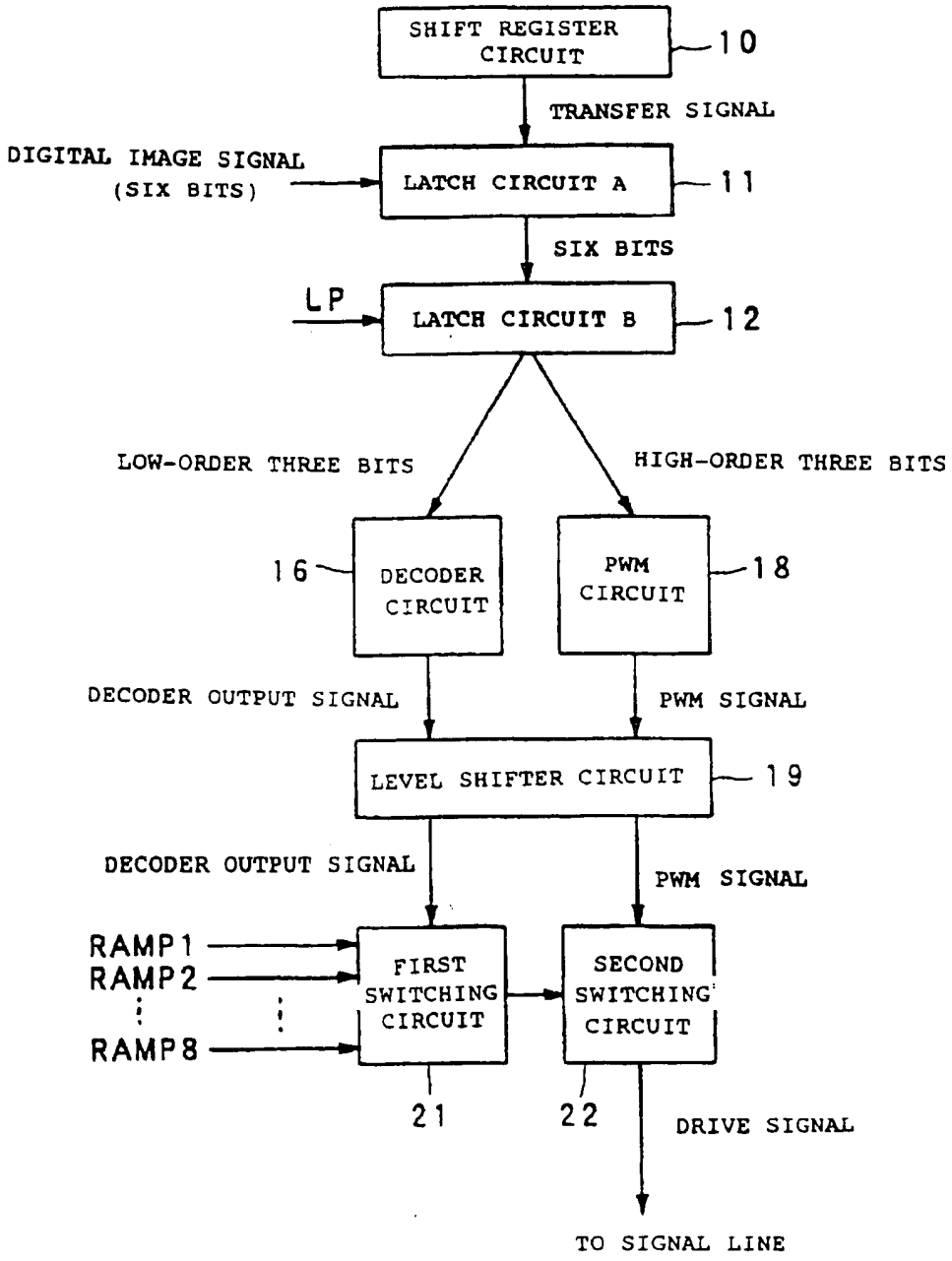
(57) **ABSTRACT**

A digital driver circuit and method for driving a liquid-crystal device or other electro-optical display device. Drive performance of the electro-optical device is improved while keeping power consumption low. The digital driver circuit receives a digital image signal as an input and generates an analog drive signal. A series selection circuit selects one series from plural series of standard multi-ramp waves having voltages that change in steps with the passage of time depending on the value of a low-order bit of the digital image signal. A time selection circuit selects, on a time axis, a voltage that changes in steps in at least the selected series of standbard multi-ramp waves depending on the value of a high-order bit of the digital image signal.

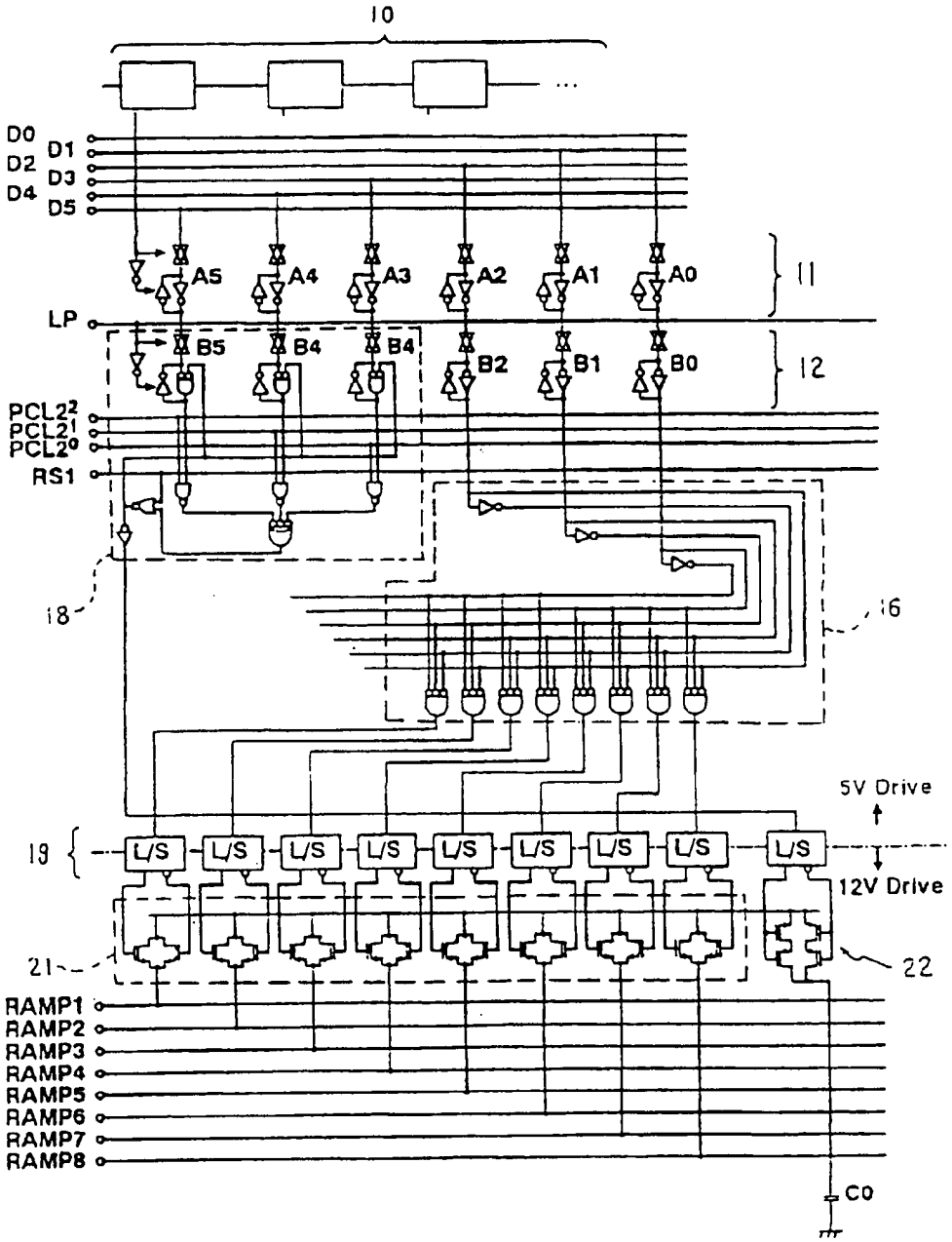
6 Claims, 21 Drawing Sheets



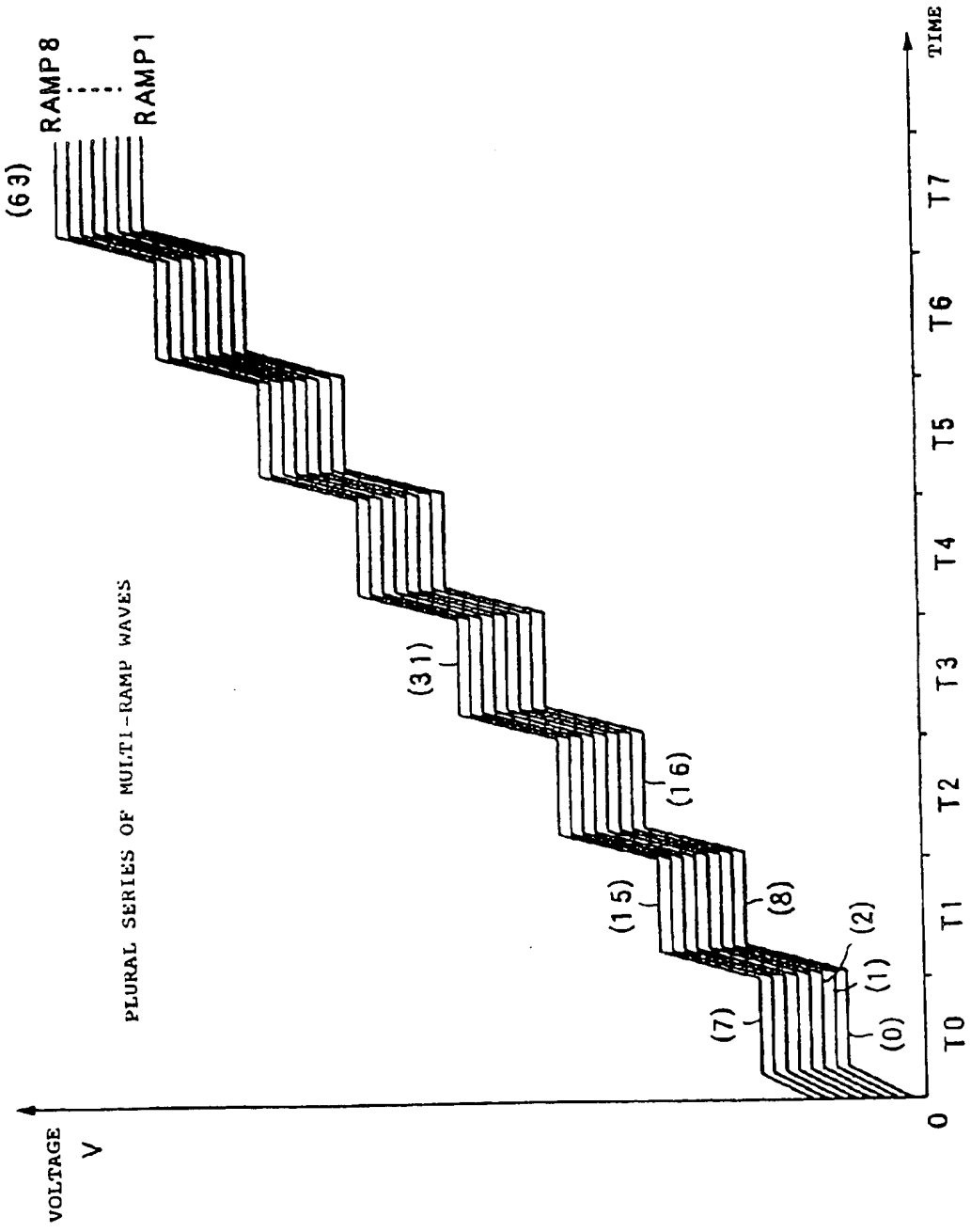
[FIG. 1]


SHIFT REGISTER CIRCUIT
10
TRANSFER SIGNAL
DIGITAL IMAGE SIGNAL (SIX BITS)
LATCH CIRCUIT A
11
SIX BITS
LP
LATCH CIRCUIT B
12
LOW-ORDER THREE BITS
HIGH-ORDER THREE BITS
16
DECODER CIRCUIT
PWM CIRCUIT
18
DECODER OUTPUT SIGNAL
PWM SIGNAL
LEVEL SHIFTER CIRCUIT
19
DECODER OUTPUT SIGNAL
PWM SIGNAL
RAMP1
RAMP2
RAMP8
FIRST SWITCHING CIRCUIT
SECOND SWITCHING CIRCUIT
21
22
DRIVE SIGNAL
TO SIGNAL LINE

[FIG. 2]


10
D0
D1
D2
D3
D4
D5
A5
A4
A3
A2
A1
A0
11
LP
B5
B4
B4
B2
B1
B0
12
PCL2²
PCL2¹
PCL2⁰
RS1
18
16
5V Drive
19
L/S
12V Drive
21
22
RAMP1
RAMP2
RAMP3
RAMP4
RAMP5
RAMP6
RAMP7
RAMP8
C0

[FIG. 3]


RAMP8
RAMP1
(63)
(31)
(16)
(15)
(8)
(7)
(2)
(1)
(0)
T0
T1
T2
T3
T4
T5
T6
T7
TIME
0
VOLTAGE
V
PLURAL SERIES OF MULTI-RAMP WAVES

[FIG. 4]

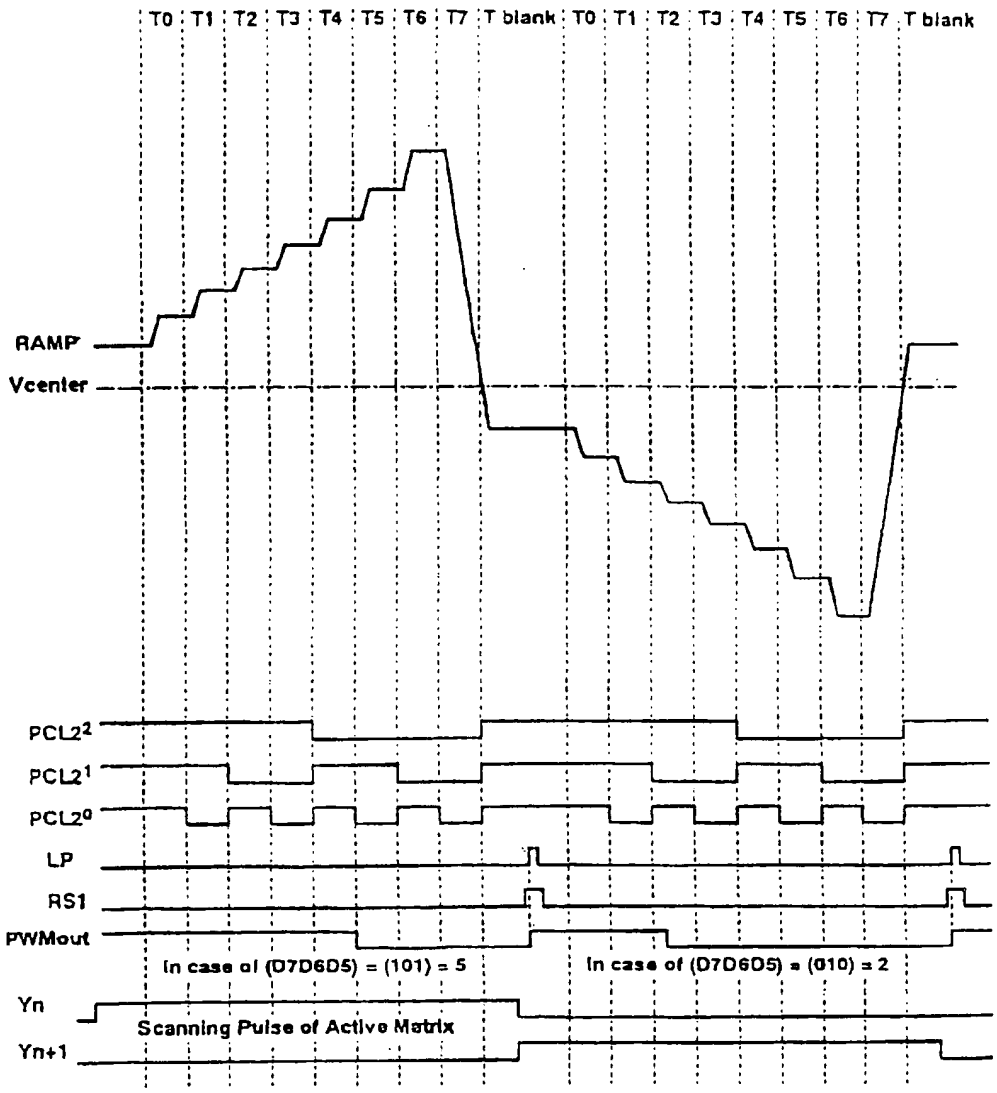

T0 T1 T2 T3 T4 T5 T6 T7 T blank T0 T1 T2 T3 T4 T5 T6 T7 T blank
RAMP
Vcenter
PCL2²
PCL2¹
PCL2⁰
LP
RS1
PWMout
In case of (D7D6D5) = (101) = 5
In case of (D7D6D5) = (010) = 2
Yn
Scanning Pulse of Active Matrix
Yn+1

FIG. 5 (A)

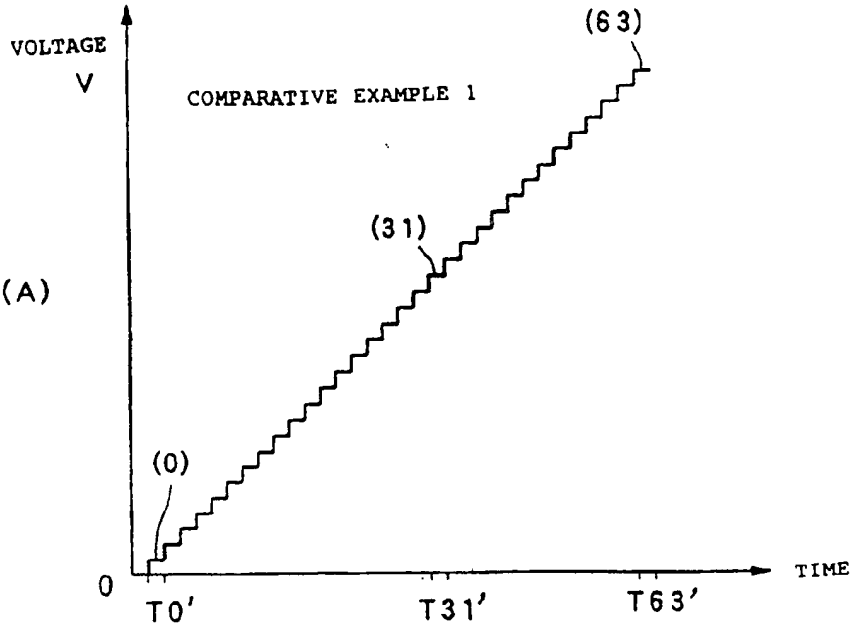
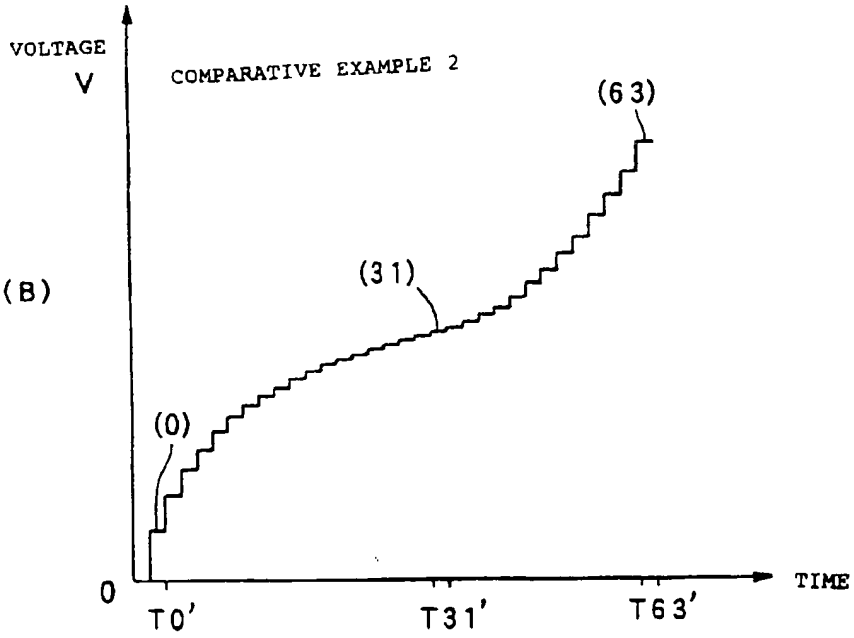
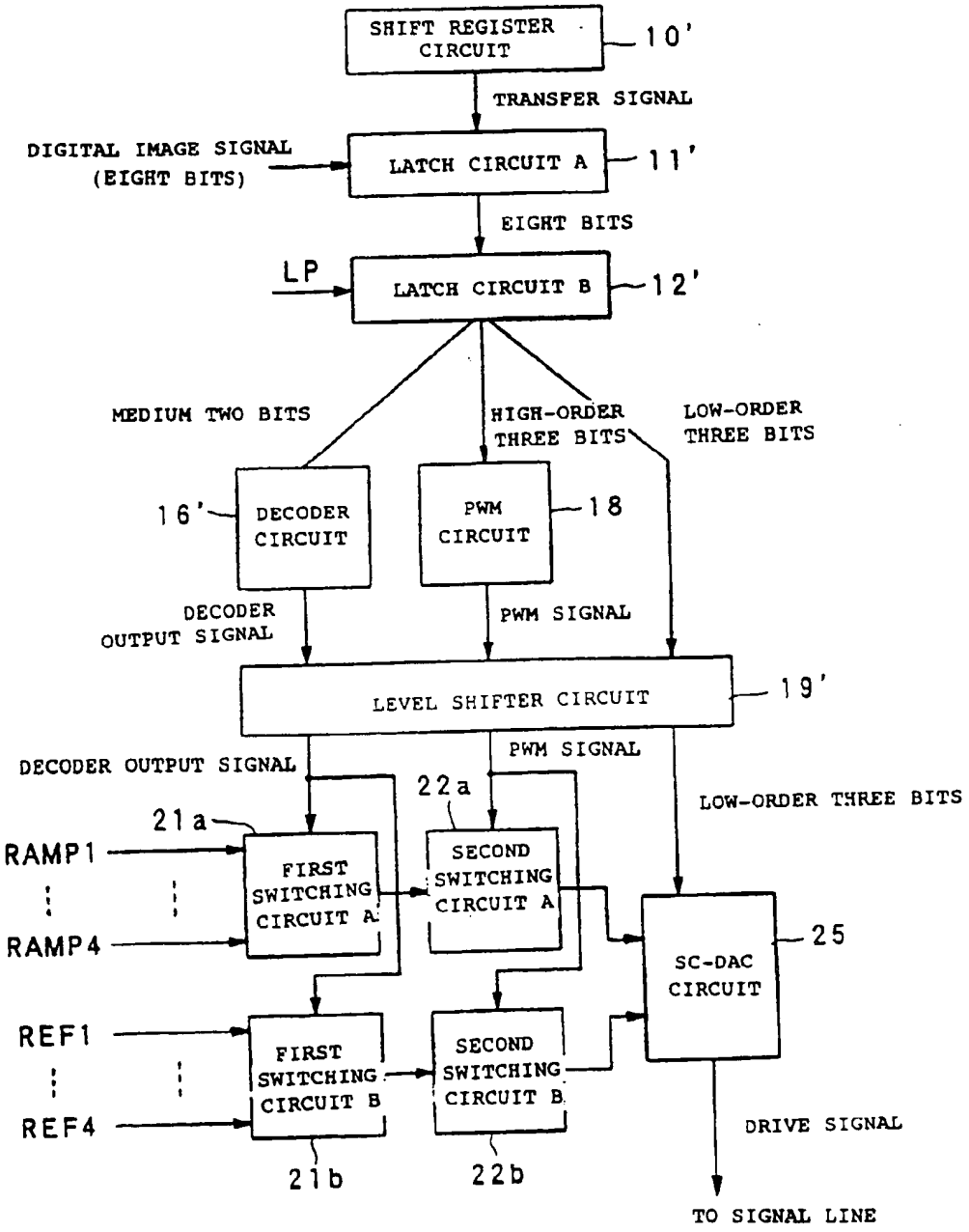

VOLTAGE
V
COMPARATIVE EXAMPLE 1
(63)
(31)
(0)
0
TIME
T0'
T31'
T63'

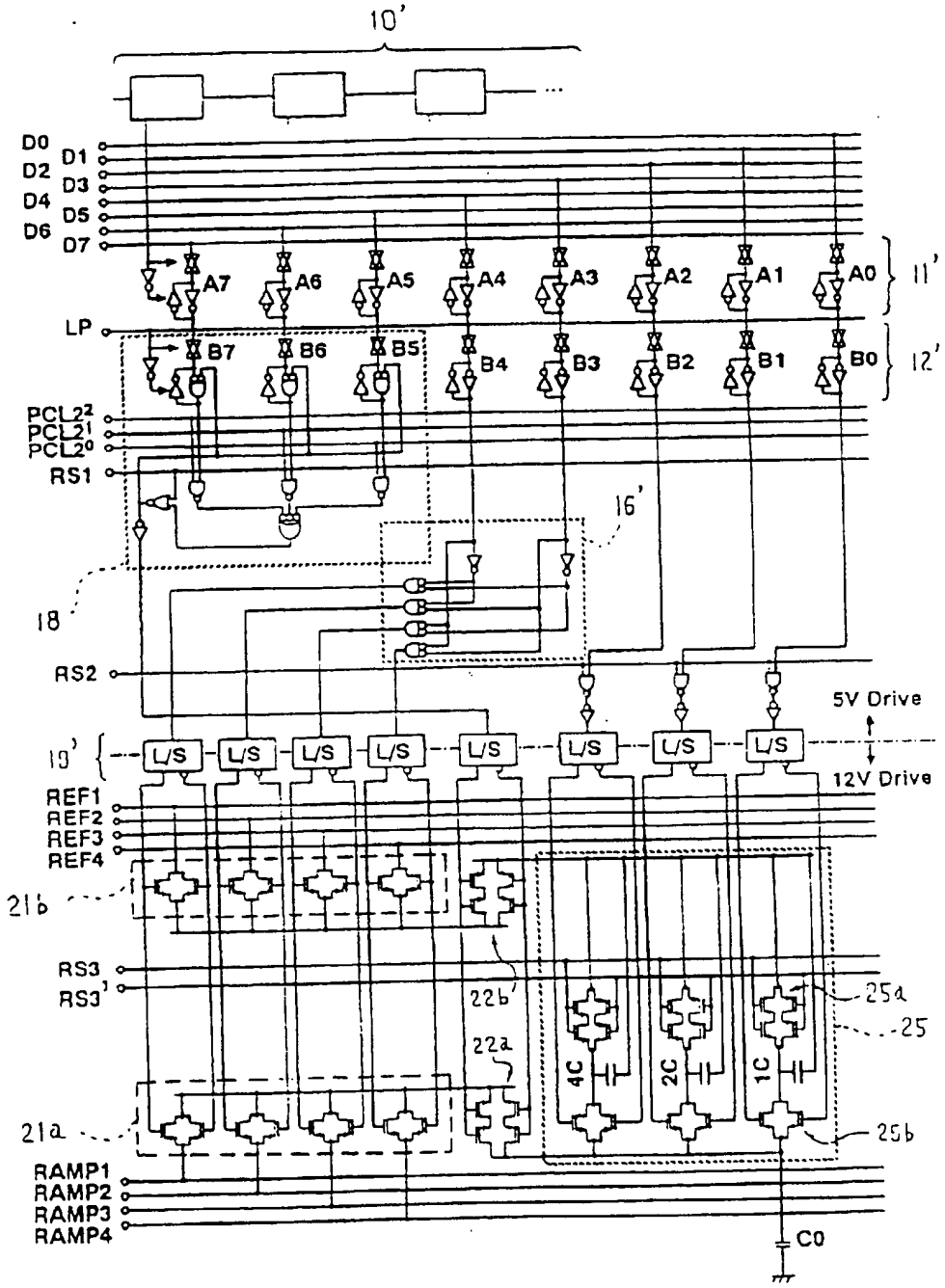
FIG. 5 (B)


VOLTAGE
V
COMPARATIVE EXAMPLE 2
(63)
(31)
(0)
0
TIME
T0'
T31'
T63'

[FIG. 6]


SHIFT REGISTER CIRCUIT
10'
TRANSFER SIGNAL
DIGITAL IMAGE SIGNAL (EIGHT BITS)
LATCH CIRCUIT A
11'
EIGHT BITS
LP
LATCH CIRCUIT B
12'
MEDIUM TWO BITS
HIGH-ORDER THREE BITS
LOW-ORDER THREE BITS
16'
DECODER CIRCUIT
PWM CIRCUIT
18
DECODER OUTPUT SIGNAL
PWM SIGNAL
LEVEL SHIFTER CIRCUIT
19'
DECODER OUTPUT SIGNAL
PWM SIGNAL
LOW-ORDER THREE BITS
21a
22a
RAMP1
RAMP4
FIRST SWITCHING CIRCUIT A
SECOND SWITCHING CIRCUIT A
SC-DAC CIRCUIT
25
REF1
REF4
FIRST SWITCHING CIRCUIT B
SECOND SWITCHING CIRCUIT B
DRIVE SIGNAL
21b
22b
TO SIGNAL LINE

[FIG. 7]


10'
D0
D1
D2
D3
D4
D5
D6
D7
A7
A6
A5
A4
A3
A2
A1
A0
11'
LP
B7
B6
B5
B4
B3
B2
B1
B0
12'
PCL2²
PCL2¹
PCL2⁰
RS1
16'
18'
RS2
5V Drive
19'
L/S
12V Drive
REF1
REF2
REF3
REF4
21b
RS3
RS3'
22b'
22a
25a
25
4C
2C
1C
21a
25b
RAMP1
RAMP2
RAMP3
RAMP4
C0

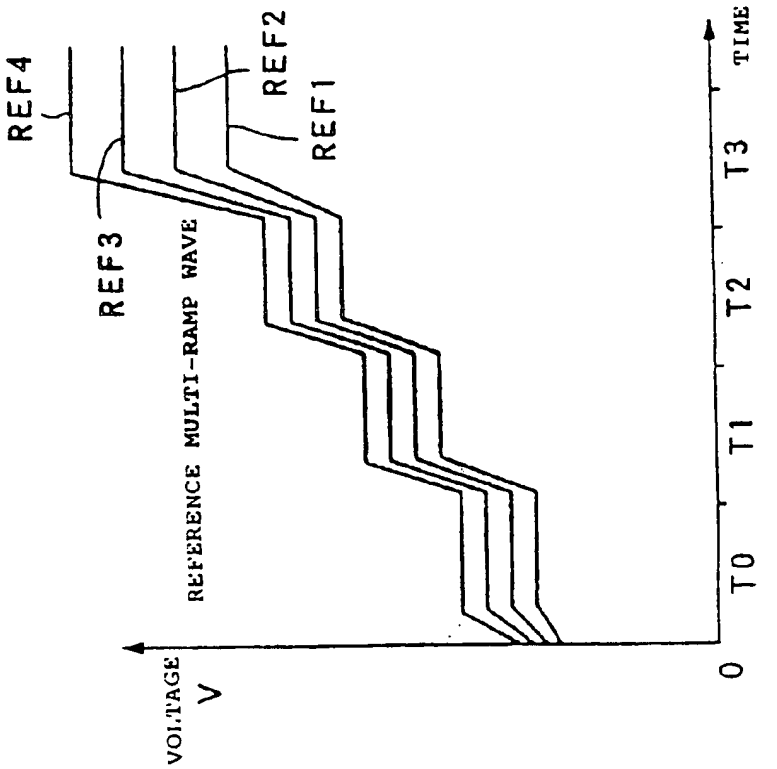

REF4
REF3
REF2
REF1
REFERENCE MULTI-RAMP WAVE
VOLTAGE
V
0
T0
T1
T2
T3
TIME

FIG. 8B

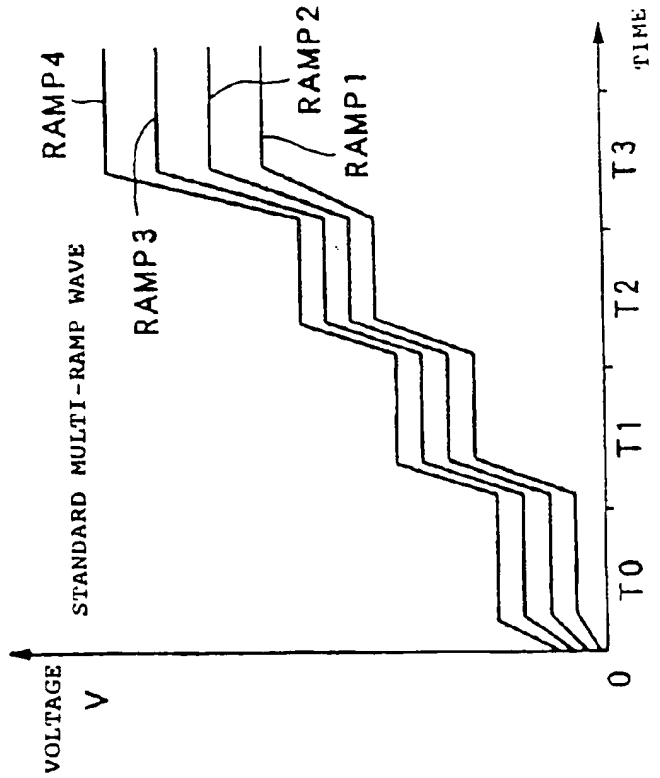
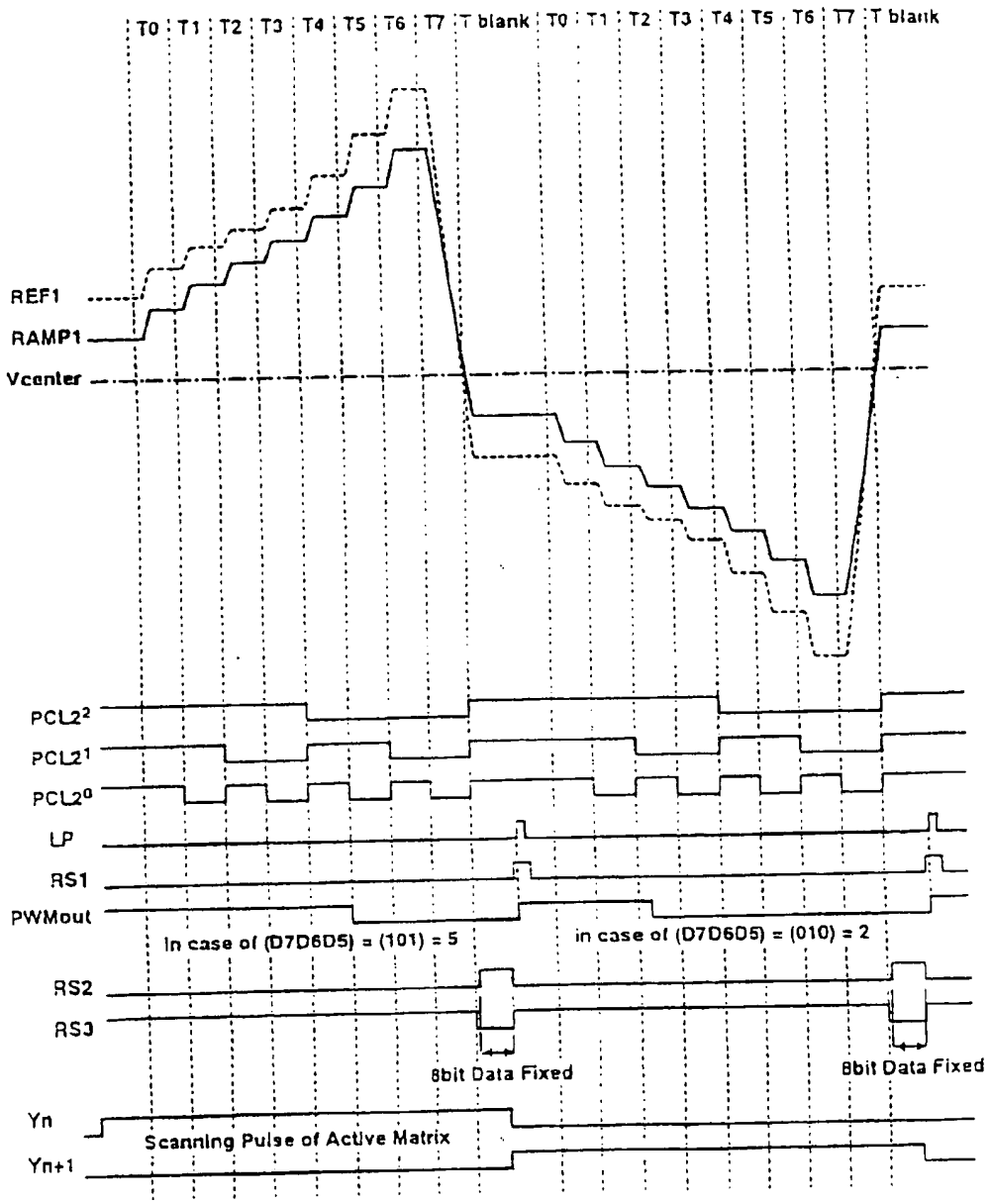
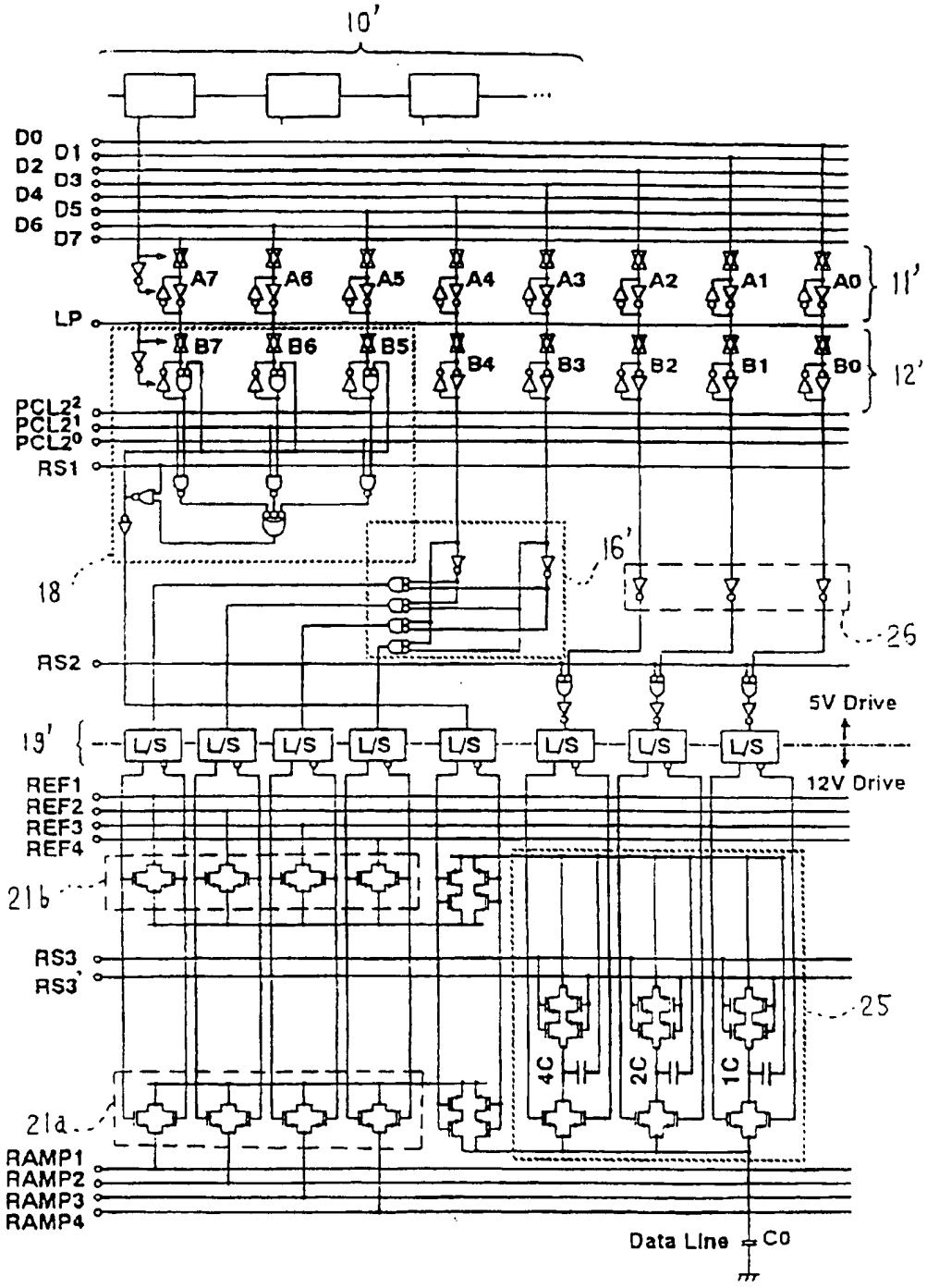

RAMP4
RAMP3
RAMP2
RAMP1
STANDARD MULTI-RAMP WAVE
VOLTAGE
V
0
T0
T1
T2
T3
TIME

FIG. 8A

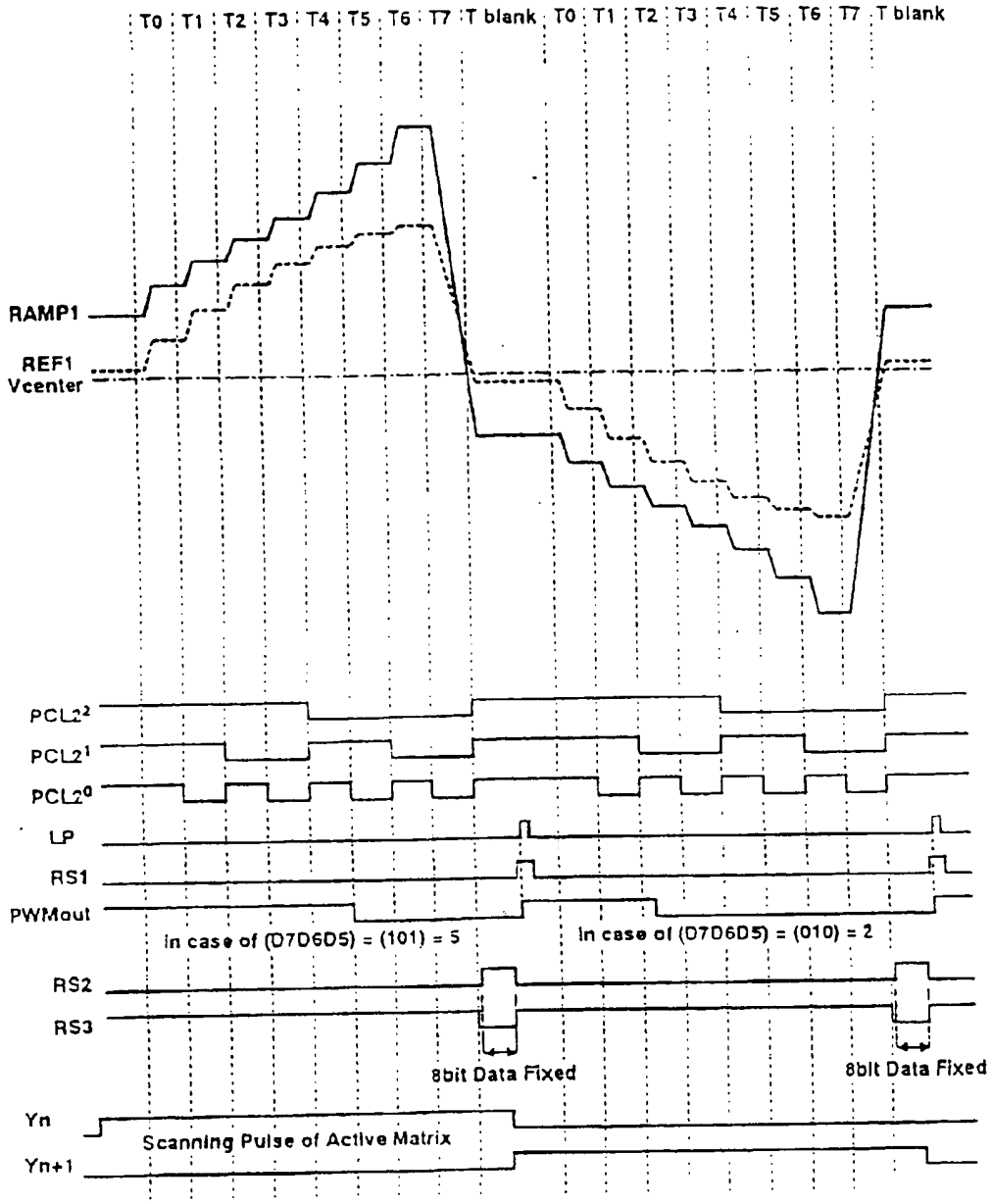
[FIG.9]


T0 T1 T2 T3 T4 T5 T6 T7 T blank T0 T1 T2 T3 T4 T5 T6 T7 T blank
REF1
RAMP1
Vcenter
PCL2²
PCL2¹
PCL2⁰
LP
RS1
PWMout
In case of (D7D6D5) = (101) = 5
in case of (D7D6D5) = (010) = 2
RS2
RS3
8bit Data Fixed
8bit Data Fixed
Yn
Yn+1
Scanning Pulse of Active Matrix

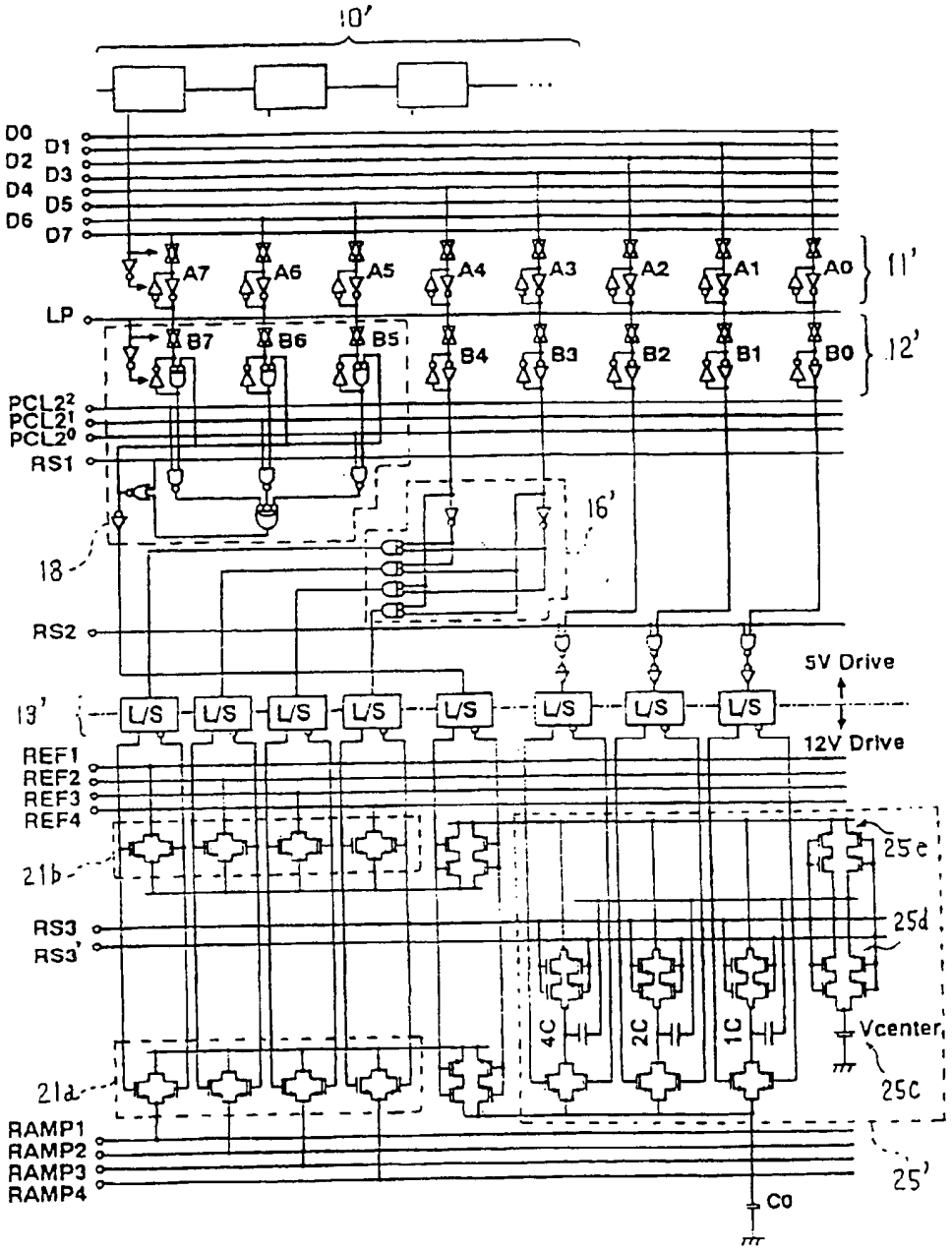
[FIG. 10]


10'
D0
D1
D2
D3
D4
D5
D6
D7
A7
A6
A5
A4
A3
A2
A1
A0
11'
LP
B7
B6
B5
B4
B3
B2
B1
B0
12'
PCL2²
PCL2¹
PCL2⁰
RS1
18
16'
26
RS2
5V Drive
19'
L/S
12V Drive
REF1
REF2
REF3
REF4
21b
RS3
RS3'
25
4C
2C
1C
21a
RAMP1
RAMP2
RAMP3
RAMP4
Data Line
C0

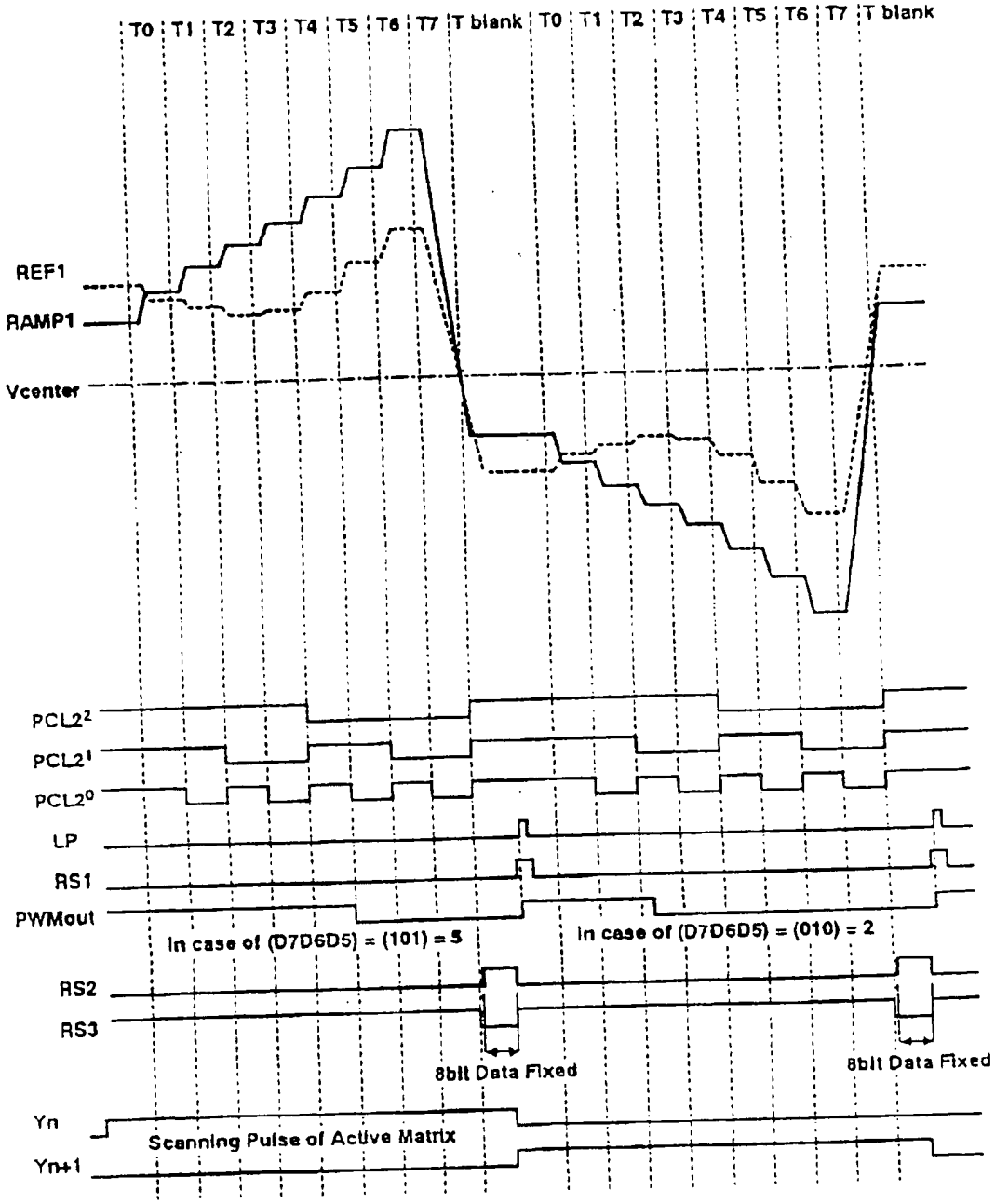
[FIG. 11]


T0 T1 T2 T3 T4 T5 T6 T7 T blank T0 T1 T2 T3 T4 T5 T6 T7 T blank
RAMP1
REF1
Vcenter
PCL2²
PCL2¹
PCL2⁰
LP
RS1
PWMout
In case of (D7D6D5) = (101) = 5
In case of (D7D6D5) = (010) = 2
RS2
RS3
8bit Data Fixed
8bit Data Fixed
Yn
Yn+1
Scanning Pulse of Active Matrix

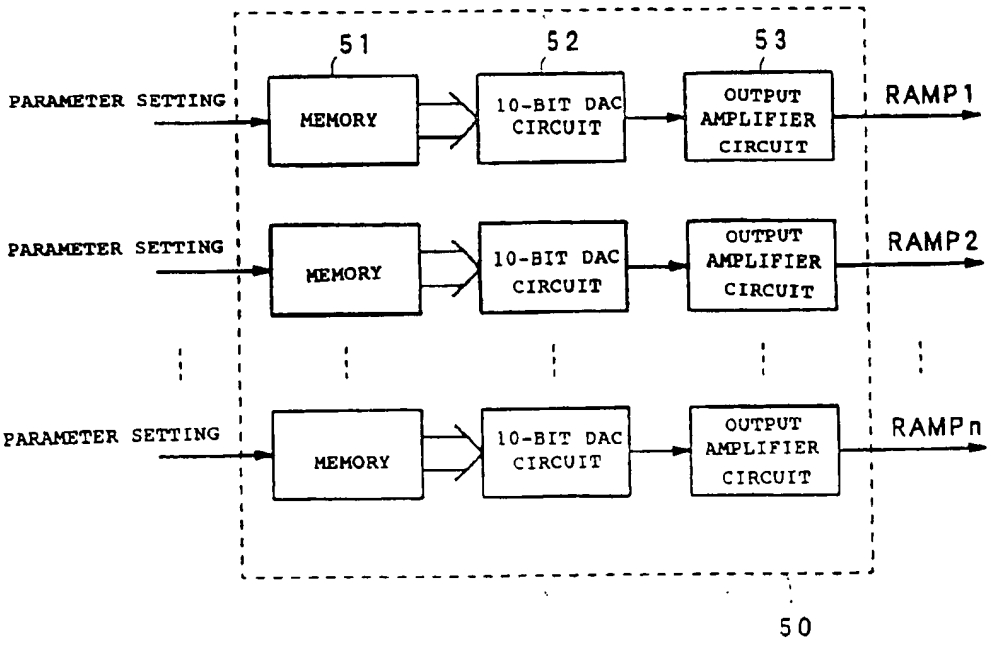
[FIG. 12]


10'
D0
D1
D2
D3
D4
D5
D6
D7
A7
A6
A5
A4
A3
A2
A1
A0
11'
LP
B7
B6
B5
B4
B3
B2
B1
B0
12'
PCL2²
PCL2¹
PCL2⁰
RS1
16'
18
RS2
5V Drive
13'
L/S
12V Drive
REF1
REF2
REF3
REF4
21b
25e
RS3
RS3'
25d
4C
2C
1C
Vcenter
21a
25c
RAMP1
RAMP2
RAMP3
RAMP4
25'
Co

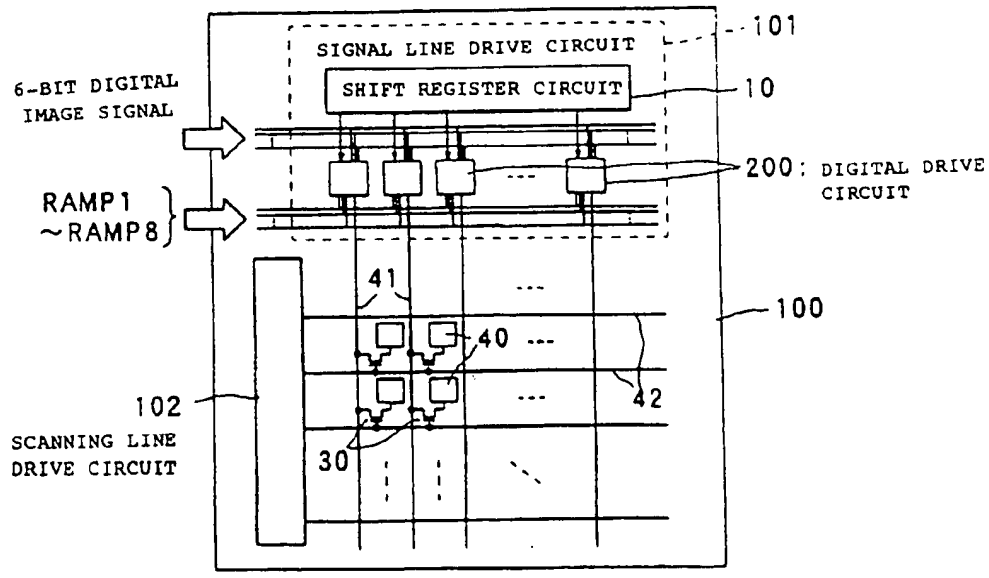
[FIG. 13]


T0 T1 T2 T3 T4 T5 T6 T7 T blank T0 T1 T2 T3 T4 T5 T6 T7 T blank
REF1
RAMP1
Vcenter
PCL2²
PCL2¹
PCL2⁰
LP
RS1
PWMout
In case of (D7D6D5) = (101) = 5
In case of (D7D6D5) = (010) = 2
RS2
RS3
8bit Data Fixed
8bit Data Fixed
Yn
Yn+1
Scanning Pulse of Active Matrix

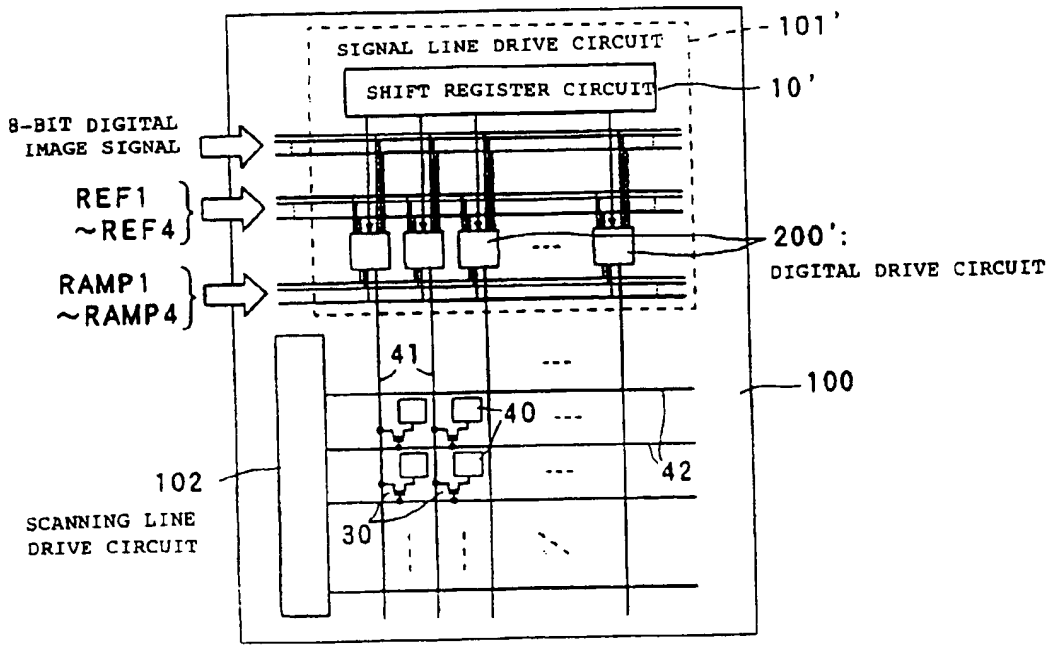
[FIG. 14]


51
52
53
PARAMETER SETTING
MEMORY
10-BIT DAC CIRCUIT
OUTPUT AMPLIFIER CIRCUIT
RAMP1
PARAMETER SETTING
MEMORY
10-BIT DAC CIRCUIT
OUTPUT AMPLIFIER CIRCUIT
RAMP2
PARAMETER SETTING
MEMORY
10-BIT DAC CIRCUIT
OUTPUT AMPLIFIER CIRCUIT
RAMPn
50

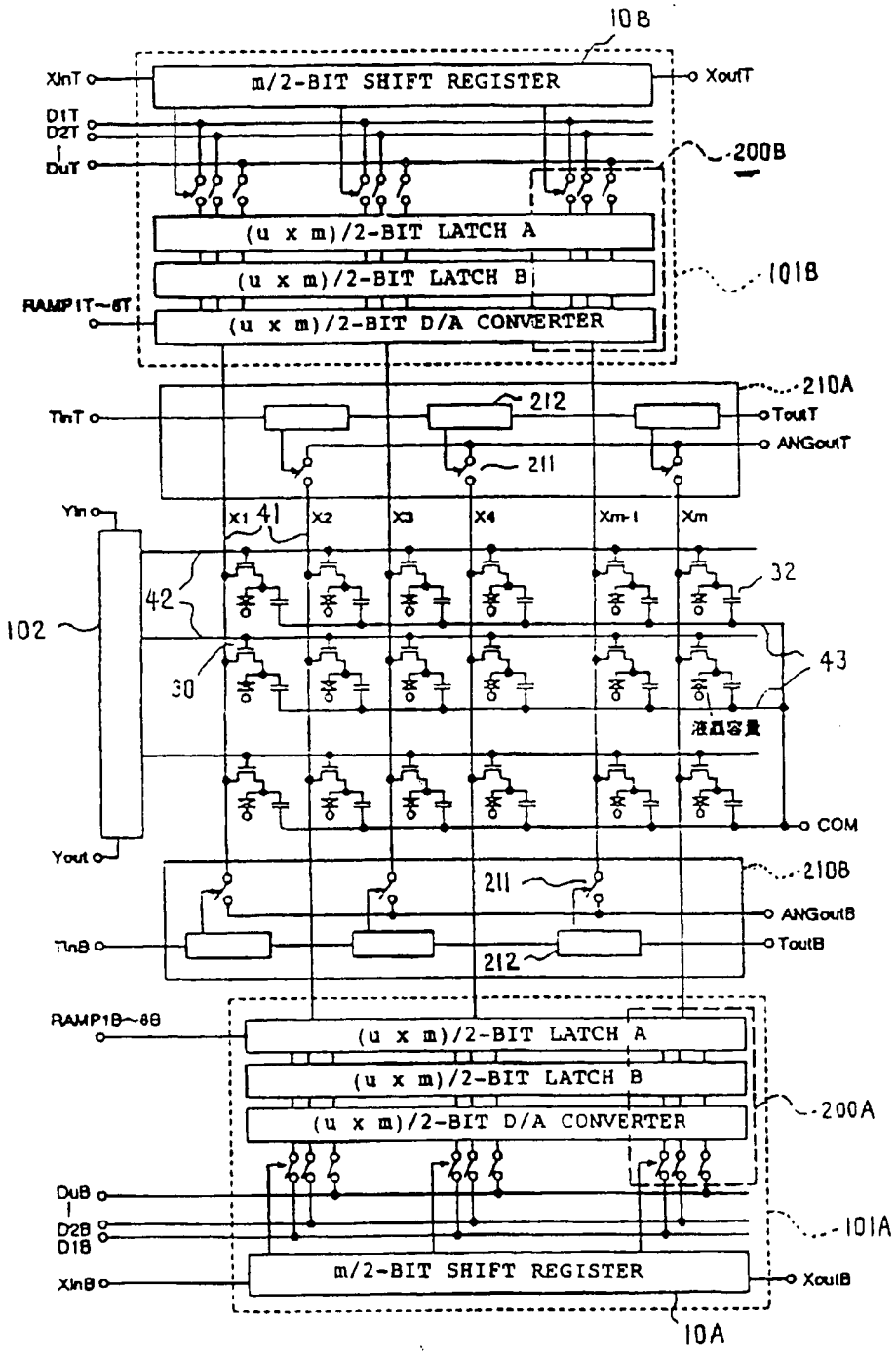
[FIG. 15]


101
SIGNAL LINE DRIVE CIRCUIT
SHIFT REGISTER CIRCUIT
10
6-BIT DIGITAL IMAGE SIGNAL
200: DIGITAL DRIVE CIRCUIT
RAMP1 ~RAMP8
41
40
100
42
102
SCANNING LINE DRIVE CIRCUIT
30

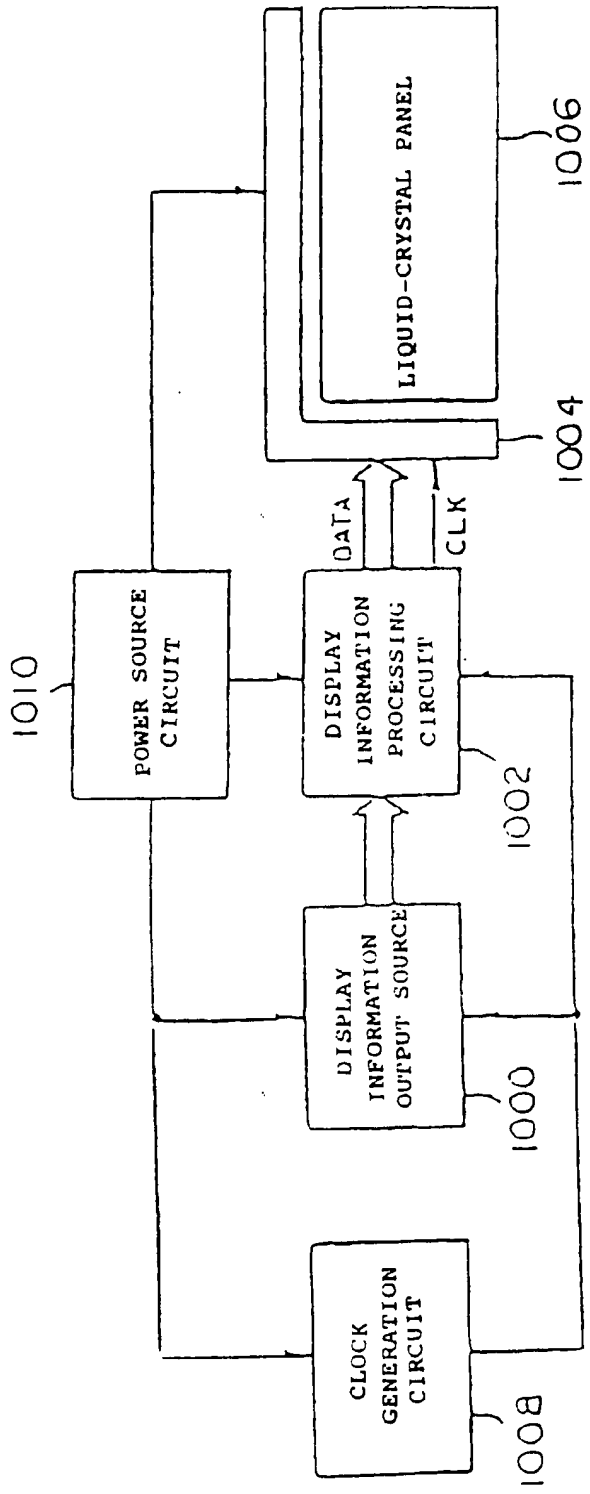
[FIG. 16]


SIGNAL LINE DRIVE CIRCUIT
101'
SHIFT REGISTER CIRCUIT
10'
8-BIT DIGITAL IMAGE SIGNAL
REF1 ~REF4
RAMP1 ~RAMP4
200': DIGITAL DRIVE CIRCUIT
41
40
42
100
102
SCANNING LINE DRIVE CIRCUIT
30

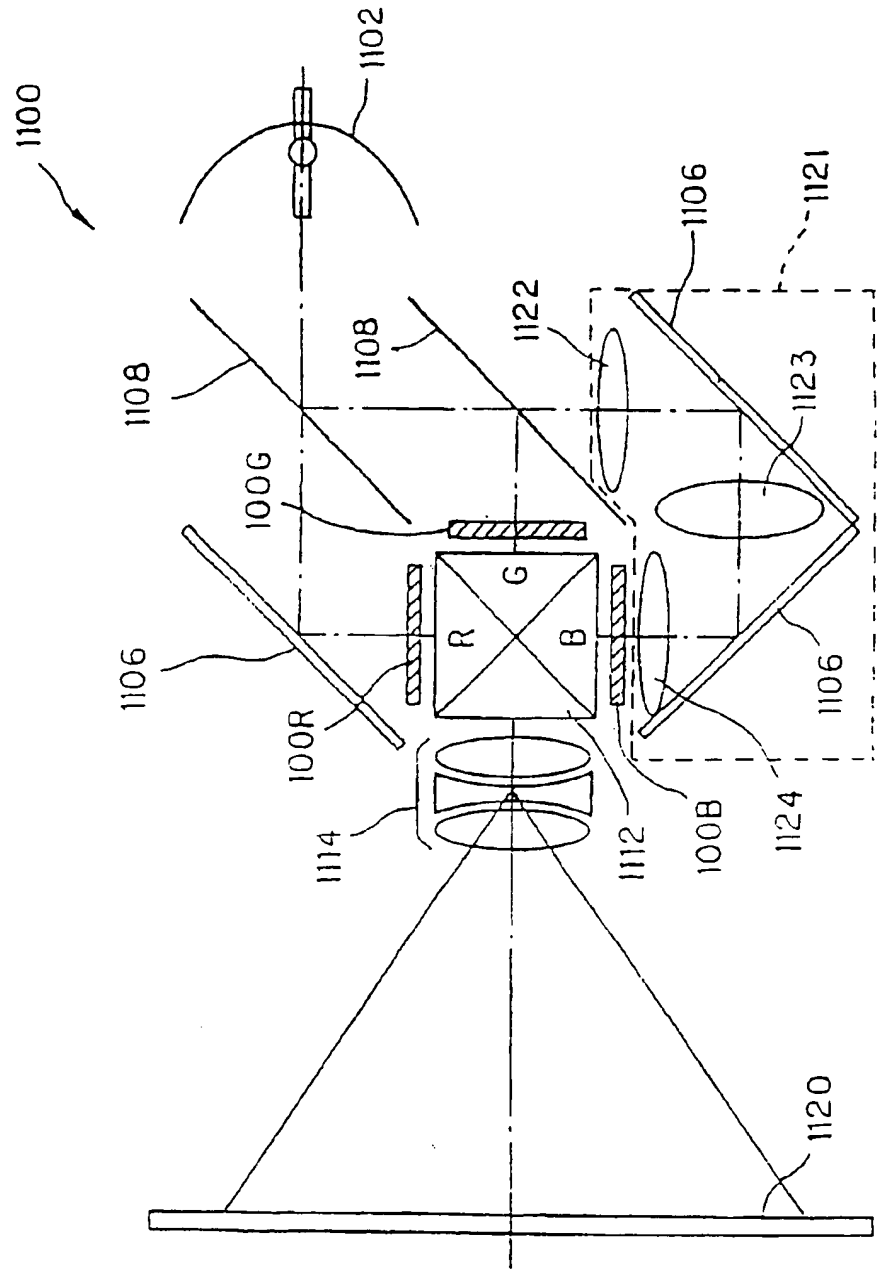
[FIG. 17]


108
XInT
m/2-BIT SHIFT REGISTER
XoutT
D1T
D2T
DuT
200B
(u x m)/2-BIT LATCH A
(u x m)/2-BIT LATCH B
101B
RAMP1T~8T
(u x m)/2-BIT D/A CONVERTER
210A
212
TInT
ToutT
ANGoutT
211
Yin
X1 41
X2
X3
X4
Xm-1
Xm
42
32
102
30
43
液晶容量
COM
Yout
210B
211
ANGoutB
TInB
ToutB
212
RAMP1B~8B
(u x m)/2-BIT LATCH A
(u x m)/2-BIT LATCH B
(u x m)/2-BIT D/A CONVERTER
200A
DuB
D2B
D1B
101A
XInB
m/2-BIT SHIFT REGISTER
XoutB
10A

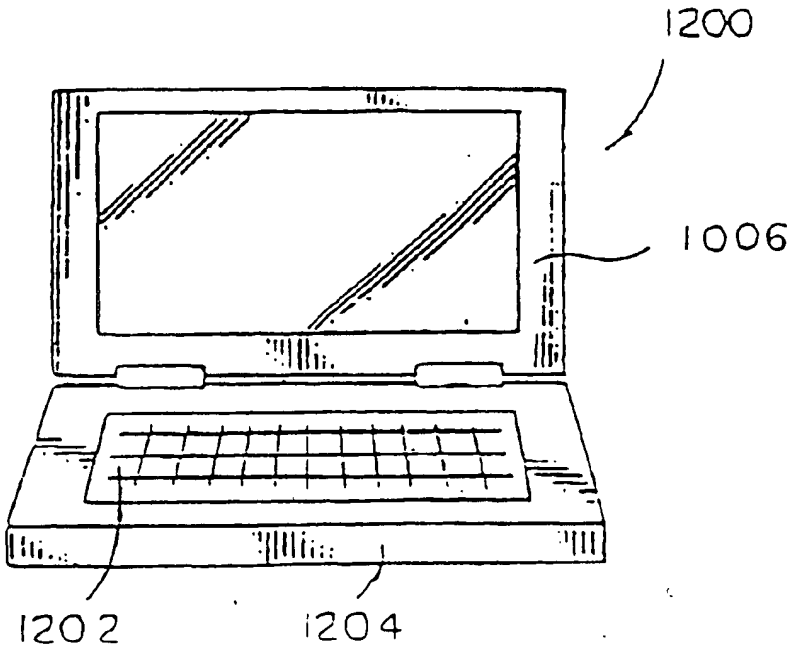
[FIG. 18]


LIQUID-CRYSTAL PANEL
1006
1004
DATA
CLK
POWER SOURCE CIRCUIT
1010
DISPLAY INFORMATION PROCESSING CIRCUIT
1002
DISPLAY INFORMATION OUTPUT SOURCE
1000
CLOCK GENERATION CIRCUIT
1008

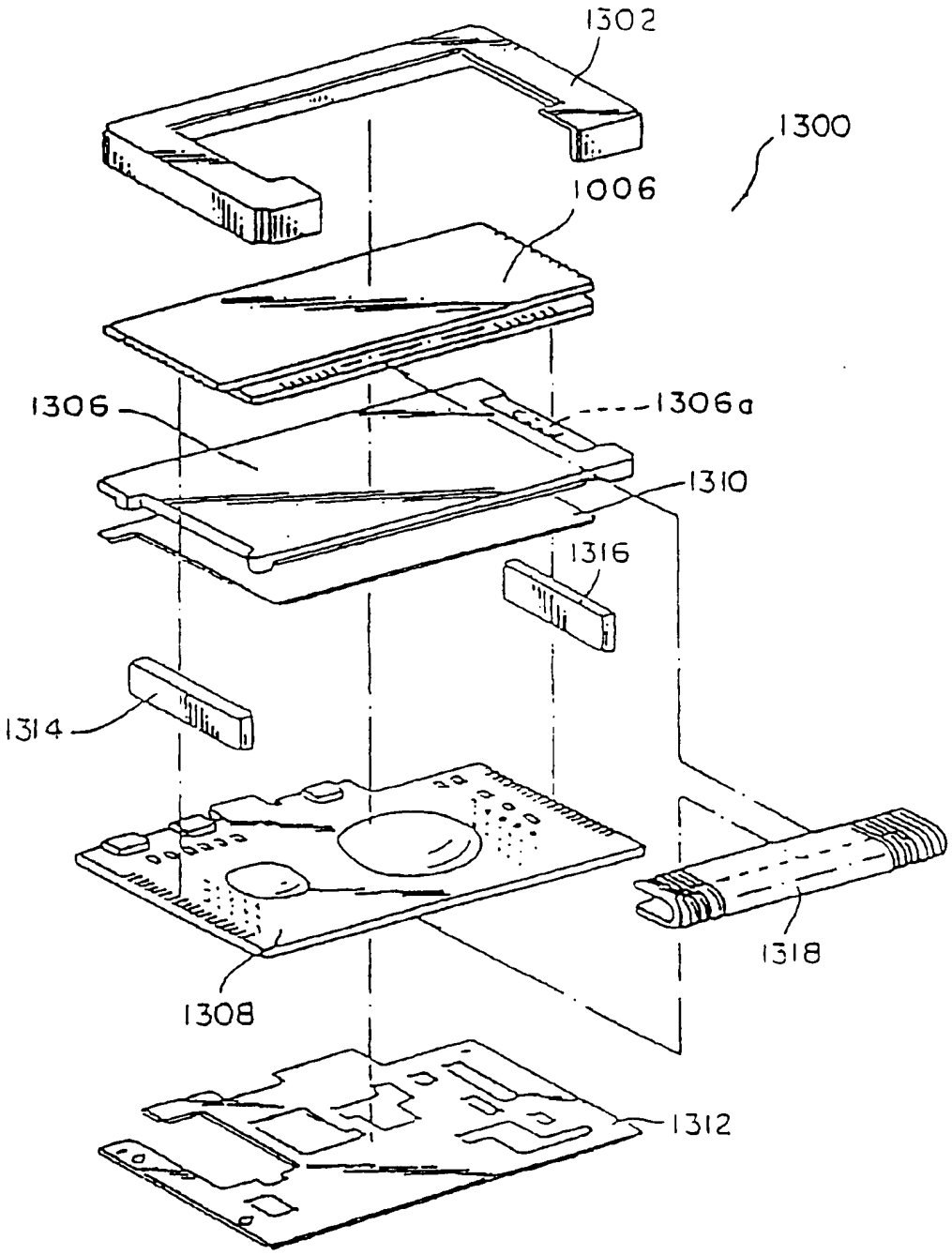
[FIG. 19]


1100
1102
1106
1121
1122
1108
1108
1123
100G
G
R
B
1106
1106
100R
1114
1112
100B
1124
1120

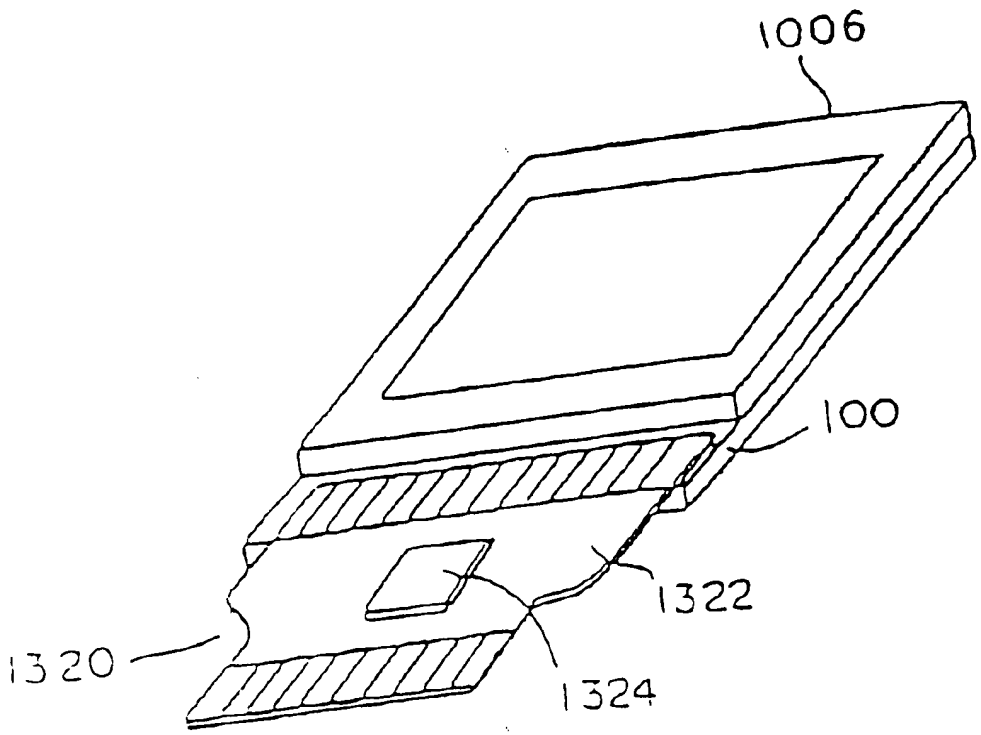
[FIG. 20]



[FIG. 21]



[FIG. 22]



DIGITAL DRIVER CIRCUIT FOR ELECTRO-OPTICAL DEVICE AND ELECTRO-OPTICAL DEVICE HAVING THE DIGITAL DRIVER CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of Invention

The present invention is directed to a digital driver circuit suitably used to drive an electro-optical device, such as a liquid-crystal device, using a TFT active matrix drive scheme, an electro-optical device having the digital driver circuit, and an electronic apparatus having the electro-optical device. More particularly, the invention is directed to a digital driver circuit or the like which receives a digital image signal as an input and uses multi-ramp waves to generate an analog drive signal.

2. Description of Related Art

Digital driver circuits which receive a digital image signal as an input and drive a display panel such as a liquid-crystal panel, to create a gradation display are known. For example, a digital driver circuit including an SC-DAC (Switched Capacitor—Digital to Analog Converter) circuit for selectively performing charge sharing or charge pumping of charges that accumulate in a plurality of capacitors having different capacities by a switching element depending on a digital image signal to generate plural voltage levels have been used. The SC-DAC circuit outputs plural voltage levels to a signal line of the display panel as drive signals corresponding to respective gradation levels, so that a gradation display can be realized. Typically, the digital driver circuit of the form including the SC-DAC circuit is externally connected to a display panel.

As another example of a digital driver circuit for driving a display panel such that a gradation display can be generated, a digital driver circuit of a form including a serial divided-voltage resistor circuit is disclosed in Japanese Unexamined Patent Publication No. 9-54309. In this form, a serial divided-voltage resistor circuit divides a plurality of reference voltages depending on a digital image signal to generate plural voltage levels, and the voltages are output to the signal line of a display panel as drive signals corresponding to respective gradation levels, so that a gradation display can be created.

In addition, as another example of a digital driver circuit for driving a display panel such that a gradation display can be generated, a digital driver circuit having a form including a PWM (pulse width modulation) circuit and using a ramp wave (saw-tooth wave) voltage is disclosed in Japanese Unexamined Patent Publication No. 9-244588. In this formation, the digital image signal is subjected to pulse width modulation by the PWM circuit to generate pulse signals having pulse widths corresponding to the digital image signals. A ramp wave is selected on a time axis depending on the pulse width to generate plural voltage levels, and the voltages are output to the signal line of the display panel as drive signals corresponding to respective gradation levels, so that a gradation display can be created.

In a digital driver circuit of this type, a general demand for a simplified circuit arrangement or for low power consumption is strong, and at the same time, a demand for drive performance to be high even with an increase of the size of a display panel. In particular, γ-correction required depending on a non-linear gradation characteristic for drive signal voltages in a display panel, such as a liquid-crystal panel, must be accurately performed by a circuit arrangement that is as simple as possible.

However, according to a digital driver circuit of a form including the conventional SC-DAC circuit, in order to make drive performance high, a large-capacity capacitor is required. For this reason, for example, the digital driver circuit is actually limited to driving a liquid-crystal panel having a size of about 5" in diagonal length. More specifically, it is difficult for the digital driver circuit to drive a display panel, such as a liquid-crystal panel, having a size larger than the above size. In particular, in a display panel having a digital driver circuit built therein, this formation in which a large capacitor must be formed on a substrate is not appropriate from the viewpoint of total circuit area or pixel pitch.

According to the conventional digital driver circuit including a serial divided-voltage resistor circuit, in order to improve drive performance, power consumption in each resistor inevitably increases with an increase in current. For this reason, the digital driver circuit cannot have a low power consumption. At the same time, a switching element, such as a thin film transistor, for performing switching control of the resistors must be increased in size to improve drive performance, and the area of the entire circuit increases. In particular, in a display panel having a digital driver circuit being built therein, a large number of resistors and large-size thin film transistors or the like must be formed on a substrate, which is not appropriate from the viewpoint of circuit area or pixel pitch.

In addition, according to the conventional digital driver circuit of a form including a PWM circuit, control of the voltage of a ramp wave with respect to time must be extremely accurately performed to correctly generate a gradation display. Therefore, an amplifier for supplying a ramp wave requires high performance, must be able to rapidly saturate a voltage for a signal line at a correct timing depending on a pulse signal, and also must create a highly accurate waveform for the ramp wave. Practically, it is very difficult to realize this type of circuit. Since a large-power ramp wave must be input at a low output impedance to improve drive performance, a problem that power consumption in the digital driver circuit is considerably high occurs. In particular, when y-correction for a digital image signal is required, problems can occur. More specifically, when as a scheme of γ-correction, any one of (i) a scheme in which the duty of a PWM base clock is changed for a gradation level depending on the characteristics of a display panel, (ii) a scheme in which a ramp wave for a time axis is changed into an S shape depending on the characteristics of a display panel, and (iii) a scheme in which a pseudo-S-shaped ramp waveform depending on the characteristics of a display panel is formed by a voltage which exactly gradually changes is selected, a voltage must be controlled at an accuracy that is higher than that used when γ-correction is not performed. Therefore, it is practically almost impossible that voltages for driving a plurality of signal lines are assured by the digital driver circuit of this formation. For this reason, the digital driver circuit of this formation is not typically used.

The present invention has been made in consideration of the problems described above, and has as its problem to provide a digital driver circuit having relatively low power consumption and relatively high performance, an electro-optical device having the digital driver circuit, and an electronic apparatus having the electro-optical device.

SUMMARY OF THE INVENTION

The invention provides a digital driver circuit that receives a digital image signal of n (n is a natural number not

less than 2) bits as an input and generates an analog drive signal corresponding to the digital image signal to output to a signal line of an electro-optical device. The digital driver circuit includes a series selection circuit that selects one series from plural series of standard multi-ramp waves having voltages which change in steps with the passage of time depending on the value of y (y is a natural number) bits of the n bits. A time selection circuit selects, on a time axis, a voltage which changes in steps in at least the selected series of standard multi-ramp waves depending on the value of x (x is a natural number) bits whose bit position is higher than that of the y bits of the n bits. The drive signal is output based on the selected voltage in the selected series.

One series is selected from the plural series of standard multi-ramp waves depending on the value of the y bits (e.g., medium or least significant three bits, four bits, or the like) of the n bits (e.g., six bits, 8 bits, 16 bits, or the like). On the other hand, the voltage which changes in steps in at least the selected series of standard multi-ramp waves is selected on the time axis depending on the value of the x bits (e.g., most significant three bits, four bits, or the like) whose bit position is higher than the y bits of the n bits. The series selection and the voltage selection may be simultaneously performed, or one of them may be performed first. When the series selection and the voltage selection are combined with each other as described above, voltages (i.e., drive signals) corresponding to the values of digital image signals are generated. For this reason, the step-form change in voltage in each of the series of standard multi-ramp waves is a relatively large change at every step, and the change in voltage at each step is maintained over a relatively long time period. Therefore, the accuracies of timings required for the series of standard multi-ramp waves become considerably low. In addition, even if the performance of the amplifier for supplying the standard multi-ramp waves is low, a time margin which is sufficient to saturate a signal line with the voltages of drive signals can be assured.

More specifically, when a drive signal is generated by using a constant voltage (saturation voltage) which is achieved after each ramp wave rises without using a voltage at the leading edge of the ramp wave, a sharp rising characteristic with respect to the corresponding ramp wave is not necessary. As a result, drive performance of the digital driver circuit can be improved by using a circuit having a relatively low through rate while the power consumption is made low, and compensation for temperature or the like can also be easily performed. Furthermore, such a circuit can be formed having a relatively small circuit area and a relatively simple structure. Therefore, the present invention is applied as a digital driver circuit, having high drive performance, for driving an electro-optical device such as a large-size display panel, or a digital driver circuit which can be built in an electro-optical device and has a small size and low power consumption.

In one aspect of the invention, a time selection circuit includes a PWM circuit for generating pulse signals having different pulse widths depending on the value of the x bits, and a first switching circuit for selecting the voltage on a time axis depending on the pulse widths. The series selection circuit includes a decoder for decoding the value of the y bits and a second switching circuit for selecting the series depending on the decoded value.

Pulse signals having different pulse widths are generated by the PWM circuit depending on the value of the x bits first, and, depending on the pulse widths, a voltage which changes in steps in the standard multi-ramp waves is selected on the time axis by the first switching circuit, e.g., a thin film transistor. On the other hand, in the series selection circuit, the value of the y bits is decoded by the decoder, and, depending on the decoded value, a series of standard multi-ramp waves is selected by the second switching circuit, e.g., a thin film transistor. Therefore, selection of standard multi-ramp waves and selection of a voltage can be performed with high reliability by using a combination of the PWM circuit, the decoder, and the switching circuit. When this arrangement is employed, high drive performance can also be realized while suppressing power consumption to a low level.

In one aspect of the invention, the selected voltage in the selected series is output as the drive signal. Thus, a selected voltage in the selected series of standard multi-ramp waves can be directly output as a drive signal. Therefore, when the number (n) of bits of a digital image signal is small, i.e., about six, a voltage is selected on the time axis depending on, e.g., three high-order bits, and a series of standard multi-ramp waves is selected depending on three low-order bits. In this manner, the digital driver circuit is especially effective from the viewpoint that a simple circuit arrangement and a simple selection scheme can be used.

In one aspect of the invention, the digital driver circuit includes a voltage change circuit that changes the selected voltage in the selected series depending on the value of z (z is a natural number) bits whose bit position is lower than that of the y bits of the n bits, and the changed voltage is output as the drive signal.

The selected voltage in the selected series of standard multi-ramp waves is changed by the voltage change circuit depending on the value of the z bits (e.g., least significant three bits, four bits, or the like) whose bit position is lower than that of the y bits. The changed voltage is output as a drive signal. Therefore, when the number (n) of bits of a digital image signal is large, i.e., about eight, a voltage is selected on the time axis depending on three high-order bits, a series of standard multi-ramp waves is selected depending on two medium bits, and the selected voltage is slightly changed depending on three low-order bits. In this manner, the digital driver circuit is effective from the viewpoint that multi-gradation can be realized with low power consumption and high drive performance.

In one aspect of the invention, the voltage change circuit includes an SC-DAC circuit for increasing and decreasing the selected voltage in the selected series depending on the value of the z bits, the series selection circuit for further selecting one series of plural series of reference multi-ramp waves for causing the SC-DAC circuit to increase and decrease the selected voltage, and the time selection circuit for further selecting, on a time axis, a voltage which changes in steps in at least the selected series of reference multi-ramp waves depending on the value of the x bits.

One series of the plural series of reference multi-ramp waves for causing the SC-DAC circuit to increase and decrease the selected voltage is further selected depending on the value of the y bits. On the other hand, in the time selection circuit, the voltage which changes in steps in at least the selected series of reference multi-ramp waves is further selected on the time axis depending on the value of the x bits. The series selection and the voltage selection may be simultaneously performed, or one of them may be performed first. In the voltage change circuit, the selected voltage in the selected series of standard multi-ramp waves is increased and decreased by the SC-DAC circuit depending on the value of the z bits. Therefore, when the number (n) of bits of a digital image signal is large, i.e., about eight,

a voltage selected depending on three least significant bits is slightly changed by using the SC-DAC circuit. In this manner, the digital driver circuit is effective from the viewpoint that multi-gradation can be realized with low power consumption and high drive performance. In particular, the present invention, which performs only fine adjustment of the voltage of a drive signal by using the SC-DAC circuit, can considerably increase the limit of drive performance in comparison with the prior art in which all the gradation levels are realized by using an SC-DAC circuit. Therefore, the present invention is suitable as a digital driver circuit to be built in a display panel which generally has a limited size and has limited space for forming an excessively large capacitor therein.

In one aspect of the invention, the SC-DAC circuit performs charge sharing using a plurality of capacitors depending on the value of the z bits on the basis of the selected voltage in the selected series of standard multi-ramp waves and the selected voltage in the selected series of reference multi-ramp waves.

Charge sharing using a plurality of capacitors is performed by the SC-DAC circuit depending on the value of the z bits on the basis of the selected voltage in the selected series of standard multi-ramp waves and the selected voltage in the selected series of reference multi-ramp waves. Therefore, a voltage between the voltage of the standard multi-ramp waves and the voltage of the reference multi-ramp waves corresponding to the standard multi-ramp waves can be output by charge sharing.

In one aspect of the invention, the voltage change circuit further comprises an inversion circuit that inverts the value of the z bits to input the value to the SC-DAC circuit, and the SC-DAC circuit performs voltage subtraction by charge sharing depending on the inverted value of the z bit.

The value of the z bits is inverted by the inversion circuit first, and the inverted value of the z bits is input to the SC-DAC circuit. At this time, in the SC-DAC circuit, voltage subtraction is performed by charge sharing depending on the inverted value of the z bit. Therefore, the voltage between the voltage of standard multi-ramp waves and the voltage of reference multi-ramp waves which correspond to the standard multi-ramp waves and is lower than the voltage of the standard multi-ramp waves at the same time can be output by voltage subtraction. In this manner, when the voltage of the reference multi-ramp waves is set to be lower than that of the standard multi-ramp wave, the reference multi-ramp waves in the digital driver circuit can be easily handled, and an amplifier having low performance can be advantageously used to generate the reference multi-ramp wave.

In one aspect of the invention, the SC-DAC performs charge pumping using a plurality of capacitors depending on the value of the z bits on the basis of the selected voltage in the selected series of standard multi-ramp waves and the selected voltage in the selected series of reference multi-ramp waves.

Charge pumping using a plurality of capacitors is performed by the SC-DAC circuit depending on the value of the z bits on the basis of the selected voltage in the selected series of standard multi-ramp waves and the selected voltage in the selected series of reference multi-ramp waves. More specifically, for example, the difference between the potential of the selected series of reference multi-ramp waves is added to the potential of the selected series of standard multi-ramp waves by a selected capacitor. Therefore, a large voltage can be applied with a small capacitance by charge pumping. For this reason, the capacitors can be reduced in size, so that an area occupied by the circuit can be reduced.

In one aspect of the invention, voltages of the plural series of standard multi-ramp waves increase or decrease every predetermined time unit in a period in which the voltages steadily increase or decrease in steps. The magnitudes of the voltages of the plural series of standard multi-ramp waves in the same time unit are constant in all time units in the period, and the maximum value of the voltages of the plural series of standard multi-ramp waves in one time unit is set to be smaller than the minimum value of the voltages of the standard multi-ramp waves in another time unit following the corresponding one time unit.

In the plural series of standard multi-ramp waves, a voltage having discrete values at predetermined intervals properly appears in one of the time units of one of the plural series of standard multi-ramp waves. For this reason, when a series of standard multi-ramp waves is selected, and the voltage of the selected series is selected on a time axis, a voltage which efficiently has discrete values can be obtained. The voltage is directly output as a drive signal, or a multi-gradation-level drive signal can be output on the basis of the voltage.

In one aspect of the invention, a multi-ramp wave generation circuit generates the plural series of standard multi-ramp waves.

The plural series of standard multi-ramp waves are generated by the multi-ramp wave generation circuit arranged in the digital driver circuit. Therefore, in particular, standard multi-ramp waves are not required to be supplied from an external circuit. The digital driver circuit including an SC-DAC circuit may further include a reference multi-ramp wave generation circuit that generates plural series of reference multi-ramp waves. The digital driver circuit may also be formed such that one or both of the standard multi-ramp waves and the reference multi-ramp waves are supplied from outside of the digital driver circuit.

In one aspect of the invention, the multi-ramp wave generation circuit adjusts the voltages of the plural series of standard multi-ramp waves to perform γ-correction of the digital image signal to the electro-optical device.

The voltage of the plural series of standard multi-ramp waves are adjusted by the multi-ramp wave generation means to perform γ-correction of the digital image signal to the electro-optical device, such as a display panel. In this case, the step-form changes in voltages of the series of standard multi-ramp waves are changes which increase in steps over a relatively long time period. For this reason, when the γ-correction is to be performed, the accuracies of timings required for the standard multi-ramp waves can be low. Therefore, by using a multi-ramp wave generation circuit having a relatively low through rate, γ-correction can be performed at a high accuracy while keeping power consumption low and improving drive performance.

In one aspect of the invention, the voltages of the plural series of standard multi-ramp waves are adjusted to perform γ-correction of the digital image signal to the electro-optical device, such as a display panel. In this case, the step-form changes in voltages of the series of standard multi-ramp waves ares changes which increase every step and the voltages at each step are maintained over a relatively long period of time. For this reason, when γ-correction is to be performed, the accuracies of timings required for the standard multi-ramp waves may be low. Therefore, by using a multi-ramp wave generation circuit having a relatively low through rate, γ-correction can be performed at a high accu-

racy while keeping power consumption low and improving drive performance.

In one aspect of the invention, an electro-optical device includes a digital driver circuit of the invention. Since the electro-optical device includes a digital driver circuit of the present invention, a large-size electro-optical device can be realized with low power consumption.

In one aspect of the invention, the electro-optical device is a liquid-crystal device having a thin film transistor as a switching element in each pixel and using a TFT active matrix drive scheme. The series selection circuit and the series time selection circuit are thin film transistors, respectively.

Since the series selection circuit and the series time selection circuit in the digital driver circuit for driving a liquid-crystal device using the TFT active matrix drive scheme are constituted by thin film transistors, respectively, various elements and circuits can be constituted by thin film transistors in the device. For this reason, the electro-optical device is advantageous in structure. In particular, such a digital driver circuit can be formed as a relatively simple circuit formed on a TFT matrix substrate, using thin film transistors, and having a relatively small circuit area. Thus, a liquid-crystal device which has a large screen, but low power consumption and uses the TFT active matrix drive scheme can be realized. In addition, when the digital drive circuit is formed such that the voltages of standard multi-ramp waves are adjusted to perform γ-correction, a multi-gradation-level, high-quality display operation can be performed while performing γ-correction at a high accuracy.

In one aspect of the invention, an electronic apparatus, such as a television set, a satellite navigation system, an electronic organizer, or a portable telephone set which has a large size and low power consumption and includes the electro-optical device according to the invention can perform a multi-gradation-level, high-quality display operation or the like.

The invention also provides a method for driving an electro-optical device. A series of standard multi-ramp waves, having voltages that change in steps with a passage of time, is selected based on y bits of an n bit digital image signal. A voltage in the selected series of standard multi-ramp waves is then selected based on x bits of the digital image signal. The x bits of the digital image signal have a higher bit position than the y bits. An analog drive signal is output to an electro-optical device based on the selected voltage.

The operations and other aspects of the present invention will be apparent from the embodiments to be described below.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing the arrangement of a digital driver circuit according to a first embodiment of the present invention.

FIG. 2 is a circuit diagram of a digital driver circuit according to the first embodiment.

FIG. 3 is a waveform chart of plural series of standard multi-ramp waves used in the digital driver circuit according to the first embodiment.

FIG. 4 is a timing chart of various signals in the digital driver circuit according to the first embodiment.

FIG. 5A is a basic waveform chart of a series of multi-ramp waves in a comparative example.

FIG. 5B is a waveform chart of one series of multi-ramp waves in a comparative example for performing γ-correction.

FIG. 6 is a block diagram showing the arrangement of a digital driver circuit according to the second embodiment of the present invention.

FIG. 7 is a circuit diagram of the digital driver circuit according to the second embodiment.

FIG. 8A is a waveform chart of plural series of standard multi-ramp waves used in the digital driver circuit according to the second embodiment.

FIG. 8B is a waveform chart of reference multi-ramp waves.

FIG. 9 is a timing chart of various signals in the digital driver circuit according to the second embodiment.

FIG. 10 is a circuit diagram of a digital driver circuit according to a third embodiment of the present invention.

FIG. 11 is a timing chart of various signals in the digital driver circuit according to the third embodiment.

FIG. 12 is a circuit diagram of a digital driver circuit according to a fourth embodiment of the present invention.

FIG. 13 is a timing chart of various signals in the digital driver circuit according to the fourth embodiment.

FIG. 14 is a block diagram of a multi-ramp wave generation circuit for generating standard multi-ramp waves in the embodiments.

FIG. 15 is a block diagram of a first embodiment of a liquid-crystal device according to the present invention.

FIG. 16 is a block diagram of a second embodiment of a liquid-crystal device according to the present invention.

FIG. 17 is a block diagram of a third embodiment of a liquid-crystal device according to the present invention.

FIG. 18 is a schematic block diagram of an embodiment of an electronic apparatus according to the present invention.

FIG. 19 is a sectional view of a liquid crystal projector serving as an example of the electronic apparatus.

FIG. 20 is a front view of a personal computer serving as another example of the electronic apparatus.

FIG. 21 is an exploded perspective view of a pager serving as an example of the electronic apparatus.

FIG. 22 is a perspective view of a liquid-crystal device using a TCP and serving as an example of the electronic apparatus.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Embodiments of the present invention will be described below with reference to the drawings.

A digital driver circuit according to a first embodiment of the present invention will be described with reference to FIG. 1 to FIG. 5. FIG. 1 is a block diagram of the digital driver circuit, and FIG. 2 is a circuit diagram showing the detailed arrangement of the digital driver circuit. FIG. 3 is a waveform chart showing an example of standard multi-ramp waves used in the first embodiment, and FIG. 4 is a timing chart of various signals in the first embodiment. FIG. 5 includes waveform charts showing standard multi-ramp waves in comparative examples.

The first embodiment described below is a digital driver circuit which receives a 6-bit digital image signal as an input and generates an analog drive signal corresponding to the digital image signal for output to a signal line of an electrooptical device, e.g., a liquid-crystal panel portion in a liquid-crystal device. In particular, the first embodiment has an arrangement in which one series of eight series of standard multi-ramp waves is selected depending on three

low-order bits of the digital image signal, and the voltage of the selected standard multi-ramp waves is selected on a time axis depending on three high-order bits.

Referring to FIG. **1**, the digital driver circuit includes a latch circuit A **11** for latching 6-bit digital image signals by a transfer signal from a corresponding stage of a shift register circuit **10** having the number of stages corresponding to a plurality of digital driver circuits. A latch circuit B **12** latches all six bits of the digital image signal latched by the latch circuit A **11** at the timing of a latch pulse signal LP. A decoder circuit **16** decodes three low-order bits latched by the latch circuit B **12**, and a PWM circuit **18** performs pulse width modulation on the basis of three high-order bits latched by the latch circuit B **12**. A level shifter circuit **19** raises the voltage levels of a decoder output signal from the decoder circuit **16** and a PWM signal from the PWM circuit **18**. A first switching circuit **21** selectively outputs one of standard multi-ramp waves RAMP1 to RAMP8 whose voltages change in the form of steps with the passage of time depending on the decoder output signal input from the decoder circuit **16** through the level shifter circuit **19**. A second switching circuit **22** selects the voltage, changing in steps, of the standard multi-ramp waves selectively output from the first switching circuit **21** on a time axis depending on the pulse width of a PWM signal input from the PWM circuit **18** through the level shifter circuit **19** to output the voltage to a signal line of a liquid-crystal panel as a drive signal.

Referring to FIG. **2**, 6-bit digital image signals D0 to D5 (it is assumed that D0 and D5 denote a low-order bit and a high-order bit, respectively) are input from an external image signal source to the digital driver circuit. PWM basic clocks $PCL2^0$, $PCL2^1$, and $PCL2^2$ are input for pulse width modulation in the PWM circuit **18** from a clock generation circuit externally connected to or incorporated in the digital driver circuit. The eight series of standard multi-ramp waves RAMP1 to RAMP8 are input from a multi-ramp generation circuit externally connected to or incorporated in the digital driver circuit.

The latch circuit A **11** comprises a plurality of latch units A0 to A5 corresponding to respective bits of the digital image signals D0 to D5 and that each include a transmission gate and an inverter. Transfer signals from the corresponding stages of the shift register circuit **10** are input to the latch units A0 to A5, respectively. The latch circuit A **11** latches the digital image signals D0 to D5 at the timings of the transfer signals.

The latch circuit B **12** comprises a plurality of latch units B0 to B5 corresponding to respective bits of the digital image signals D0 to D5 and each include a transmission gate and an inverter. A latch pulse LP is input to the latch units B0 to B5. The latch circuit B **12** is formed to latch digital image signals D0 to D5 from the latch circuit A **11** at the timing of the latch pulse signal LP.

The 3-bit decoder circuit **16** decodes three low-order bits (D0 to D2) of the digital image signals D0 to D5. The first switching circuit **21**, which includes a plurality of thin film transistors, selectively supplies one of the eight series of standard multi-ramp waves RAMP1 to RAMP8 to the input terminal of the second switching circuit **22** depending on the 3-bit decoder output signals. Thus, for example, the decoder circuit **16** and the first switching circuit **21** form a series selection circuit.

The 3-bit PWM circuit **18** generates 3-bit PWM signals having different pulse widths depending on the value of high-order x bits (D3 to D5) on the basis of the PWM basic clocks $PCL2^0$, $PCL2^1$, and $PCL2^2$. The second switching circuit **22**, which includes a plurality of thin film transistors, selectively supplies the voltage of the standard multi-ramp waves supplied through the first switching circuit **21** to the signal line depending on the pulse widths of the 3-bit PWM signals. Thus, for example, the PWM circuit **18** and the second switching circuit **22** form a time selection circuit. When a reset signal RS1 is input from a control circuit (not shown), the PWM circuit **18** is reset. Reference symbol C0 connected to the output of the second switching circuit **22** denotes a capacitor that includes a signal line, a pixel electrode, and the like in a liquid-crystal panel.

The level shifter circuit **19** raises the voltage levels of a PWM signal and a decoder output signal each having a power supply voltage of, e.g., 5 V to 12 V. The values of these power source voltages are not limited to 5 V or 12 V. In addition, if a switching operation in the switching circuit **21** or **22** can be sufficiently performed at, e.g., 5 V, the digital driver circuit may be formed without the level shifter circuit **19**.

Concrete examples of the waveforms of the eight series of standard multi-ramp waves RAMP1 to RAMP8 are shown in FIG. **3**. FIG. **3** is a graph showing the voltage values of the plural series of multi-ramp waves RAMP1 to RAMP8 to a time axis including time units T0 to T7. In FIG. **3**, reference numerals (0), (1), (2), . . . , (63) denote the values (values of decimal numbers) of the digital image signals corresponding to the voltages.

As shown in FIG. **3**, the voltages of the eight series of standard multi-ramp waves RAMP1 to RAMP8 increase or decrease (increase in one period shown in FIG. **3**) every predetermined time unit Ti (i=0, 1, . . . , 7) in one period (T0 to T7) in which the voltages steadily increase or decrease in the form of steps. The magnitudes of the voltages of the standard multi-ramp waves RAMP1 to RAMP8 in the same time unit Ti are constant in all the time units Ti in one period (T0 to T7). More specifically, when the voltage of a multi-ramp RAMPj (j=1, 2, . . . , 8) in the time unit Ti is represented by V (j,i), V(1,i)<V(2,i)<. . . <V(8,i) is established in any time unit Ti. In addition, in a period (T0 to T7), the maximum value of the voltages of the plural series of standard multi-ramp waves in one time unit Ti, i.e., the voltage V(8,i) of the multi-ramp wave RAMP8 is set to be smaller than V(1,i+1) which is the voltage of the multi-ramp wave RAMP8. More specifically, V(8,i)<V(1,i+1) is established with respect to any time unit Ti.

Since the waveforms of the standard multi-ramp waves RAMP1 to RAMP8 are regularly ruled, voltages which have discrete values at predetermined intervals properly appear in one of the time units T1 in one of the standard multi-ramp waves RAMP1 to RAMP8. For this reason, when the standard multi-ramp waves RAMP1 to RAMP8 are selected, and the voltage of the standard multi-ramp waves are selected on a time axis, voltages which have discrete values can be efficiently obtained.

The operation of the embodiment arranged as described above will be described below with reference to the timing chart in FIG. **4**. In the example in FIG. **4**, it is assumed that the 6-bit value of a digital image signal is (101000) in one first-half period (left half), and is (010000) in one second-half period (right half).

Referring to FIG. **4**, in one first-half period, on one side, the value of low-order bits (000) is decoded by the decoder circuit **16**, and the standard multi-ramp wave RAMP1 is selected by the first switching circuit **21** depending on the decode output signal. The standard multi-ramp wave

RAMP1 is supplied to the input terminal of the second switching circuit **22**. On the other hand, the PWM circuit **18** generates a 3-bit PWM signal (PWMout) whose level is heightened to T4 (i.e., the fifth time unit) in correspondence with the value "5" of the three high-order bits (101) on the basis of the PWM basic clocks $PCL2^0$, $PCL2^1$, and $PCL2^2$ to supply the PWM signal to the control terminal (i.e., the gate electrode of each thin film transistor) of the second switching circuit **22**. The voltage in the time unit T4 of the standard multi-ramp wave RAMP1 supplied to the input terminal is output from the second switching circuit **22** to the signal line as a drive signal voltage.

In a time unit Thlank subsequent to the first-half period, the next digital image signal is latched by the latch circuit B **12**, and the PWM circuit **18** is reset by the reset signal RS1.

In the second-half period, on one side, the value of low-order bits (000) is decoded by the decoder circuit **16**, and the standard multi-ramp wave RAMP1 is selected by the first switching circuit **21** depending on the decode output signal. The standard multi-ramp wave RAMP1 is supplied to the input terminal of the second switching circuit **22**. On the other side, the PWM circuit **18** generates a 3-bit PWM signal whose level is heightened to Ti (i.e., the second time unit) in correspondence with the value "2"of three high-order bits (010) on the basis of the PWM basic clocks $PCL2^0$, $PCL2^1$, and $PCL2^2$ to supply the PWM signal to the control terminal of the second switching circuit **22**. The voltage in the time unit T2 of the standard multi-ramp wave RAMP1 supplied to the input terminal is output from the second switching circuit **22** to the signal line as a drive signal voltage.

In a time unit Thlank subsequent to the second-half period, the next digital image signal is latched by the latch circuit B **12**, and the PWM circuit **18** is reset by the reset signal RS1.

In the first embodiment, the drive signal output as described above is supplied to the signal line of a liquid-crystal panel using a TFT active matrix drive scheme. In this case, one horizontal scanning period in which a scanning signal Yn for driving a nth pixel row is supplied is caused to correspond to one period (T0 to T7) described above. In FIG. **4**, the Thlank positioned between the time unit T7 in one first-half period and the time unit T0 in one second-half period corresponds to a horizontal retrace line period, and one horizontal scanning period= T0+T1+. . . +T7+ Tblank is established. As shown in FIG. **3** and FIG. **4**, the standard multi-ramp waves are inverted in polarity in one period (T0 to T7) because a scanning line inversion drive scheme for inverting a drive voltage polarity every scanning line is performed in driving of the liquid-crystal panel.

As described above, according to the embodiment, selection of the standard multi-ramp waves RAMP1 to RAMP8 and selection of voltages on a time axis (i.e., selection of the time units T0 to T7) are combined with each other to generate drive signals corresponding to the values of the digital image signals D0 to D5. For this reason, step-form changes in voltage in the standard multi-ramp waves RAMP1 to RAMP8 are changes which increase in steps over a relatively long time period.

Two single series of standard multi-ramp waves which makes a gradation display possible in a digital driver circuit of a form using PWM and ramp waves is shown in FIGS. **5**(A) and **5**(B) as comparative examples. In the comparative example in FIG. **5**(A), the voltage changes every time unit Ti' (I=0 to 63), and respective changes in voltage are slight changes. The comparative example in FIG. **5**(B) shows one series of multi-ramp waves which makes γ-correction possible by changes in voltage. In this comparative example, the voltage changes every time unit Ti' (I=0 to 63), and, especially, changes in voltage near a central voltage are very slight changes.

As is apparent from comparison between FIG. **3** and FIGS. **5**(A) and **5**(B), if drive signals having the same number of gradation levels are obtained, step-form changes in voltage in the standard multi-ramp waves RAMP1 to RAMP8 according to the embodiment are changes which increase in steps over a relatively long time period in comparison with the standard multi-ramp waves in the comparative example. For example, it is assumed that the number of series is represented by M (M: natural number) and that a change in voltage for each step in case of one series of standard multi-ramp waves in FIGS. **5**(A) and **5**(B) is represented by ΔV. In FIG. **3**, a change in voltage for each step required to realize gradation changes having the same fineness is large, i.e., ΔV×M. In addition, it is assumed that a time of one step in case of one series of standard multi-ramp waves in FIGS. **5**(A) and **5**(B) is represented by ΔT. In FIG. **3**, a time of one step required to realize gradation changes having the same fineness is long, i.e., ΔT×M.

In addition, when γ-correction is performed by a change in voltage of a multi-ramp wave, only the intervals between the plural series of multi-ramp waves RAMP1 to RAMP8 shown in FIG. **3** and the angles of the multi-ramp waves RAMP1 to RAMP8 slightly change. In comparison with the comparative example shown in FIG. **5**(B), if drive signals having the same number of gradation levels are obtained, a change in voltage for each step can be increased, and a long time can be set for each step.

Therefore, according to the embodiment, the accuracies of timings required for the standard multi-ramp waves RAMP1 to RAMP8 is considerably lower. In addition, even if the performance of an amplifier for supplying the standard multi-ramp waves RAMP1 to RAMP8 is low, a time margin which is sufficient to saturate the capacitor C0 constituted by a signal line or the like of the display panel with the voltages of drive signals can be assured. More specifically, since drive signals are generated by using constant voltages (saturation voltages) which are achieved after ramp waves rise without using voltages included in the standard multi-ramp waves RAMP1 to RAMP8 and generated at the leading edges of the ramp waves, sharp rising characteristics with respect to the corresponding ramp waves are not necessary. This is considerably advantageous when plural signal lines of a large number of signal lines arranged for each pixel column of a display panel or all the signal lines are simultaneously driven.

As a result, according to the digital driver circuit according to the embodiment, drive performance can be improved by using a circuit having a relatively low through rate while the power consumption is made low, and compensation for temperature or the like can also be easily performed. Furthermore, such a circuit can be formed having a relatively small circuit area and a relatively simple structure. Therefore, the embodiment is applied as a digital driver circuit, having high drive performance, for driving a large-size display panel, or a digital driver circuit which can be built in a liquid-crystal panel and has a small size and low power consumption.

In the first embodiment, in particular, a selected voltage in selected standard multi-ramp waves is directly output as a drive signal. For this reason, when the number of bits of a digital image signal is small, i.e., about six, the digital drive circuit is especially advantageous from the viewpoint that a

circuit arrangement and a selection scheme may be relatively simple. In addition, not only a voltage-drive type electro-optical device such as a liquid-crystal panel can be driven by a voltage signal, but also, by making current supply performance for standard multi-ramp waves, a current-drive type electro-optical device such as an EL (electroluminescence) panel can be driven.

A digital drive circuit according to the second embodiment of the present invention will be described below with reference to FIG. **6** to FIG. **9**. FIG. **6** is a block diagram of a digital driver circuit according to the second embodiment, and FIG. **7** is a circuit diagram showing a more detailed arrangement of the digital driver circuit. FIG. **8** includes waveform charts showing standard multi-ramp waves and reference multi-ramp waves used in the second embodiment, and FIG. **9** is a timing chart of various signals in the second embodiment. The same reference numerals in the first embodiment shown in FIGS. **1**, **2**, and **4** denote the same elements and signals in FIG. **6** to FIG. **9**, and a description thereof is omitted.

In the second embodiment to be described below, a digital driver circuit receives 8-bit digital image signals as inputs and generates analog drive signals corresponding to the digital image signals to be output to a signal line of an electrooptical device, e.g., a liquid crystal panel. One series of four series of standard multi-ramp waves is selected depending on two medium bits of the digital image signals, and the voltage of the selected standard multi-ramp wave is selected on a time axis depending on three high-order bits to obtain a voltage having rough gradation. Thereafter, on the basis of the voltage having rough gradation, a voltage having fine gradation is obtained by an SC-DAC circuit.

Referring to FIG. **6**, the digital driver circuit according to the second embodiment includes a latch circuit A **11'** for latching 8-bit digital image signals by a transfer signal from a corresponding stage of a shift register circuit **10'** having a number of stages corresponding to a plurality of digital driver circuits. A latch circuit B **12'** latches the eight bits of the digital image signal latched by the latch circuit A **11'** at the timing of a latch pulse signal LP. A decoder circuit **16'** decodes two medium bits latched by the latch circuit B **12'**, and a PWM circuit **18** performs pulse width modulation on the basis of three high-order bits latched by the latch circuit B **12'**. A level shifter circuit **19'** raises the voltage levels of a decoder output signal from the decoder circuit **16'** and a PWM signal from the PWM circuit **18**. A first switching circuit A **21***a* selectively outputs one of four series of standard multi-ramp waves RAMP1 to RAMP4 whose voltages change in steps with the passage of time depending on the decoder output signal input from the decoder circuit **16'** through the level shifter circuit **19'**. A second switching circuit A **22***a* selects a voltage, changing in the form of steps, of the standard multi-ramp waves selectively output from the first witching circuit A **21***a* on a time axis depending on the pulse width of a PWM signal input from the PWM circuit **18** through the level shifter circuit **19**. The digital driver circuit according to the second embodiment further comprises an SC-DAC circuit **25** which increases and decreases the voltage selected by the second switching circuit A **22***a* depending on the value of three low-order bits input through the level shifter circuit **19'** to output the voltage as a drive signal to a signal line. To the digital driver circuit, plural series of reference multi-ramp waves REF1 to REF4 corresponding to the multi-ramp waves RAMP1 to RAMP4 and used as reference when the voltage is increased and decreased by the SC-DAC circuit **25** are input. The digital driver circuit further comprises a first switching circuit B **21***b* that selectively outputs one of the reference multi-ramp waves REF1 to REF4 depending on a decoder output signal input from the decoder circuit **16'** through the level shifter circuit **19'**, and a second switching circuit B **22***b* that selects a voltage, changing in the form of steps, of the reference multi-ramp waves selectively output from the second switching circuit B **22***b* on a time axis depending on the pulse width of a PWM signal input from the PWM circuit **18** through the level shifter circuit **19'**. In the second embodiment, the SC-DAC circuit **25** is an example voltage change circuit that changes the voltage selected by the second switching circuit A **22***a* depending on the value of three low-order bits.

Referring to FIG. **7**, 8-bit digital image signals D0 to D7 (it is assumed that D0 and D7 denote a low-order bit and a high-order bit, respectively), PWM basic clocks $PCL2^0$, $PCL2^1$, and $PCL2^2$, the four series of standard multi-ramp waves RAMP1 to RAMP4, and the four series of reference multi-ramp waves REF1 to REF4 are input to the digital driver circuit.

The latch circuit A **11'** includes a plurality of latch units A0 to A7 corresponding to respective bits of the digital image signals D0 to D7 and each including a transmission gate and an inverter. Transfer signals from the shift register circuit **10'** are sequentially input to the latch units A0 to A7. The latch circuit A **11'** is formed to latch the digital image signals D0 to D5 at the timings of the transfer signals.

The latch circuit B **12'** includes a plurality of latch units B0 to B7 corresponding to respective bits of the digital image signals D0 to D7 and each including a transmission gate and an inverter. A latch pulse LP is input to the latch units B0 to B7. The latch circuit B **12'** latches digital image signals D0 to D7 from the latch circuit A **11'** at the timing of the latch pulse signal LP.

The 2-bit decoder circuit **16'** decodes two medium bits (D3, D4) of the digital image signals D0 to D7. The first switching circuit A **21***a*, which includes a plurality of thin film transistors, selectively supplies one of the standard multi-ramp waves RAMP1 to RAMP4 to the input terminal of the second switching circuit A **22***a* depending on the 2-bit decoder output signals. In this example, the decoder circuit **16'** and the first switching circuit A **21***a* for a series selection circuit. The first switching circuit B **21***b* formed in the same manner as that of the first switching circuit A **21***a* selectively supplies one of the reference multi-ramp waves REF1 to REF4 to the input terminal of the second switching circuit B **22***b* depending on the 2-bit decoder output signal.

The second switching circuit A **22***a*, which includes a plurality of thin film transistors, is formed such that the voltage of standard multi-ramp waves supplied through the first switching circuit A **21***a* is selectively supplied to a standard voltage terminal of the SC-DAC circuit **25** depending on the pulse widths of 3-bit PWM signals. In this example, the PWM circuit **18** and the second switching circuit A **22***a* form a time selection circuit. The second switching circuit B **22***b* formed in the same manner as that of the second switching circuit A **22***a* is formed such that the voltage of reference multi-ramp waves supplied through the first switching circuit B **21***b* is selectively supplied to a reference voltage terminal of the SC-DAC circuit **25** depending on the pulse widths of 3-bit PWM signals.

The SC-DAC circuit **25** includes three capacitors having a capacitor ratio of 4C: 2C: 1C. Each capacitor is reset such that a reset TFT **25***a* is rendered conductive by a reset signal RS3 and an inversion signal thereof. When the reset signal RS3 is set at a low level, the reset TFT **25***a* is rendered

non-conductive, and the voltage of reference multi-ramp waves selectively supplied from the second switching circuit B **22***b* is accumulated in each capacitor. A switching TFT **25***b* is rendered conductive depending on the value of three low-order bits input through the level shifter circuit **19'**, and the voltage accumulated in each capacitor is added to standard multi-ramp waves selectively supplied from the second switching circuit A **22***a*.

The level shifter circuit **19'** raises the voltage levels of a PWM signal and a decoder output signal each having a power supply voltage of, e.g., 5 V, to 12 V.

Examples of the waveforms of the standard multi-ramp waves RAMP1 to RAMP4 and the reference multi-ramp waves REF1 to REF4 corresponding thereto are shown in FIG. **8**. For convenience, FIG. **8** includes graphs showing the voltages of multi-ramp waves corresponding to time units **T0** to **T3**.

In the examples in FIG. **8**, the reference multi-ramp waves are respectively set to be higher than the voltages of the corresponding standard multi-ramp waves such that the voltages of the corresponding standard multi-ramp waves can be raised by voltage-addition type charge sharing in the SC-DAC circuit **25**.

The operation of the embodiment arranged as described above will be described below with reference to the timing chart in FIG. **9**.

Referring to FIG. **9**, as in case of the first embodiment described with reference to FIG. **4**, in one first-half period, the voltage of the standard multi-ramp wave RAMP1 in the time unit **T4** is output from the second switching circuit A **22***a*, and, in one second-half period, the voltage of the standard multi-ramp wave RAMP1 in a time unit **T2** is output from the second switching circuit A **22***a* At the same time, in one first-half period, the voltage of the reference multi-ramp waves in the time unit **T4** is output from the second switching circuit B **22***b*, and in one second-half period, the voltage of the reference multi-ramp waves in the time unit **T2** is output from the second switching circuit B **22***b*.

In the second embodiment, in particular, three low-order bits are input to the SC-DAC circuit **25** through the level shifter circuit **19'** at the timing of a reset signal **RS2**. In a period in which the reset signal **RS3** is set at a low level, the voltages accumulated in the capacitors of the SC-DAC circuit **25** are added to the standard multi-ramp waves output from the second switching circuit A **22***a* by charge sharing depending on the value of the three low-order bits. More specifically, in case of charge sharing, in the capacitors of the SC-DAC circuit **25**, opposing electrode sides are shifted by "Vref−Vcenter" (Vref: the voltage of a selected reference multi-ramp wave REF) with connection performed by a switch (TFT), thereby adding the voltage to the standard multi-ramp wave RAMP.

As described above, in the second embodiment, for 8-bit digital image signals, a voltage is selected on a time axis depending on the three high-order bits, a series of standard multi-ramp waves is selected depending on the two medium bits, and a voltage selected depending on the three low-order bits is finely adjusted. For this reason, the second embodiment is effective from the viewpoint that multi-gradation is realized with low power consumption and high drive performance,

In the embodiment, since only fine adjustment of the drive signal is performed by the SC-DAC circuit **25**, the limit of drive performance can be considerably increased in comparison with the prior art in which all gradation levels are realized by using an SC-DAC circuit. Therefore, the embodiment is suitable as a digital driver circuit to be built in a liquid-crystal panel which generally has a limited size and has limited space for forming an excessively large capacitor therein.

In the embodiment, in particular, charge sharing using a plurality of capacitors is performed by the SC-DAC circuit **25** depending on the value of three low-order bits on the basis of a selected voltage in selected standard multi-ramp waves and a selected voltage in selected reference multi-ramp waves. Therefore, a voltage between the voltage of the standard multi-ramp waves and the voltage of the reference multi-ramp waves corresponding to the standard multi-ramp waves can be output by charge sharing.

A digital drive circuit according to the third embodiment of the present invention will be described below with reference to FIG. **10** and FIG. **11**. FIG. **10** is a block diagram of the digital driver circuit according to the third embodiment. FIG. **11** is a timing chart of various signals in the third embodiment. The same reference numerals in the second embodiment shown in FIG. **7** and FIG. **9** denote the same constituent elements and the same signals in FIG. **10** to FIG. **11**, and a description thereof will be omitted.

Referring to FIG. **10**, the digital driver circuit of the third embodiment is different from that of the second embodiment in that an inversion circuit **26** is arranged to invert three low-order bits output from a latch circuit B **12'**. The other arrangement of the third embodiment is the same as that of the second embodiment.

The SC-DAC circuit **25** performs voltage subtraction by charge sharing using reference multi-ramp waves depending on the value of the inverted three low-order bits. As shown in FIG. **11**, the other operation is the same as that in the second embodiment.

Therefore, voltages between the voltages of standard multi-ramp waves RAMP1 to RAMP4 and the voltages of reference multi-ramp waves REF1 to REF4, which are respectively lower than the voltages of the standard multi-ramp waves at the same time, can be output by voltage subtraction. In this manner, according to this embodiment, the voltages of the reference multi-ramp waves REF1 to REF4 can be set to be lower than those of the multi-ramp waves RAMP1 to RAMP4, the reference multi-ramp waves in the digital driver circuit can be easily handled, and an amplifier having low performance can be advantageously used to generate the reference multi-ramp waves REF1 to REF4.

A digital drive circuit according to the fourth embodiment of the present invention will be described below with reference to FIG. **12** and FIG. **13**. FIG. **12** is a circuit diagram of the digital driver circuit according to the fourth embodiment. FIG. **13** is a timing chart of various signals in the fourth embodiment. The same reference numerals in the second embodiment shown in FIG. **7** and FIG. **9** denote the same constituent elements and the same signals in FIG. **12** to FIG. **13**, and a description thereof will be omitted.

Referring to FIG. **12**, the digital driver circuit of the fourth embodiment is different from that of the second embodiment in the following point. An SC-DAC circuit **25'** includes a switching circuit **25***d* for selectively supplying a power supply Vcenter **25***c* and three capacitors by a reset signal RS3 and an inversion signal RS3' thereof, and a switching circuit **25***e* for selectively supplying selected reference multi-ramp waves to three capacitors by the reset signal RS3 and the inversion signal RS3' thereof The SC-DAC circuit **25'** is formed such that a difference between the potential of

the selected reference multi-ramp wave REF and a potential Vcenter is added to the potential of a selected standard multi-ramp wave RAMP by using a selected capacitor, i.e., charge pumping is performed.

When charge pumping is to be performed as described above, as shown in FIG. **13**, although the waveform of the reference multi-ramp wave REF has a large voltage at a position where the difference between gradation voltages is large, a voltage amplitude smaller than that in case of driving by charge sharing may be used This is because, in the SC-DAC circuit **25'**, when charge pumping is performed, a large voltage can be added by a small capacitor. For this reason, in case of the SC-DAC circuit **25'**, although the number of elements or the like slightly increases, the capacitors can be reduced in size, so that an area occupied by the whole circuit can be reduced.

Although the SC-DAC circuit **25'**, as shown in FIG. **12** and FIG. **13**, performs the charge pumping depending on the value of three low-order bits, the other operation is the same as that of the second embodiment.

Here, a multi-ramp wave generation circuit for supplying standard multi-ramp waves to the digital driver circuit according to each of the embodiments described above will be described below with reference to FIG. **14**.

Referring to FIG. **14**, a multi-ramp wave generation circuit **50** comprises a plurality of memories **51**, a plurality of 10-bit DAC (digital/analog converter) circuit **52**, and a plurality of output amplifier circuits **53**. The memories **51** store discrete voltage values for regulating a series of RAMP waveforms. The 10-bit DAC circuits **52** output analog data according to the voltage values stored in the memories **51**. Although the output amplifier circuits **53** amplify analog data output from the 10-bit DAC circuits **52**, the output amplifier circuits **53** are formed such that multi-ramp waves are generated in response to changes of input voltages to the output amplifier circuits **53**. In this manner, in the multi-ramp wave generation circuit **50**, a through rate is dependent on the performance of the output amplifier circuits **53**, and the 10-bit DAC circuits **52** may supply only voltage values to the output amplifier circuits **53**.

As described above, complex control need not be performed, and the output amplifier circuit **53** may have a low through rate and low output power. For this reason, the multi-ramp wave generation circuit **50** can be constituted by a very simple circuit as a whole, and is very advantageous in practical use. In this case, in particular, when the accuracy of a constant voltage (saturation voltage) which is achieved in each ramp wave included in the multi-ramp waves is set, multi-ramp waves having any waveform can be used. For this reason, a through rate can be set to be small as possible within a range in which constant voltage can be obtained, and power consumption can also be decreased to the limit.

According to the embodiment, step-form changes in voltages in the series of standard multi-ramp waves as described above are changes which increase in steps over a relatively long time period. On the other hand, a drive signal is generated by using a constant voltage which is achieved after a ramp wave rises without using a voltage generated at the leading edge of the ramp wave. For this reason, even if the ramp wave moderately rises, when the accuracy of a constant voltage achieved is high, drive performance can be realized with low power consumption by using standard multi-ramp waves output from the output amplifier circuits **53**, even if the through rates of the output amplifier circuits **53** are low or have low accuracies.

The multi-ramp wave generation circuit arranged as described above may be externally connected to a digital driver circuit or built therein. A multi-ramp wave generation circuit for generating reference multi-ramp waves is formed in the same manner as described above. When parameters stored in the memories are changed, reference multi-ramp waves having voltages which higher or lower than those of standard multi-ramp waves can be generated.

The multi-ramp wave generation circuit arranged as described above may be formed such that γ-correction of digital image signals for a liquid-crystal panel is performed by adjusting the voltages of plural series of standard multi-ramp waves, respectively. In this case, step changes in voltages in the series of standard multi-ramp waves are changes which increase in steps over a relatively long time period. For this reason, accuracies required for the timings of standard multi-ramp waves can be low. In the embodiment in which drive signals are generated by using constant voltages which are achieved after ramp waves rise without using voltages generated at the leading edges of ramp waves, sharp rising characteristics with respect to the ramp waves are not necessary. For this reason, by using a multi-ramp wave generation circuit having a relatively low through rate or a low accuracy of the through rate, γ-correction can be performed at high accuracy while power consumption is kept low and drive performance is improved.

In each of the embodiments described above, selection on a time axis is performed depending on a plurality of high-order bits, a series of standard multi-ramp waves is selected depending on a plurality of medium or low-order bits, and, in addition to this, a voltage is changed by an SC-DAC depending on a plurality of low-order bits. However, the numbers of high-order, low-order, and medium bits are not limited to the embodiments, and the numbers may be arbitrarily set and properly changed depending on the specifications of devices.

The embodiments according to the present invention described above will be compared with a digital driver circuit including the conventional serial dividedvoltage resistor circuit (to be referred to as a "comparative example 1" hereinafter) disclosed in Japanese Unexamined Patent Publication No. 9-54309 and a digital driver circuit (to be referred to as a "comparative example 2" hereinafter) in which all gradation voltages are obtained by the conventional SC-DAC circuit.

About sixteen large-size TFTs are required in portions of the embodiments of the invention described above, but about forty-eight TFTs are required in comparative example 1. This is because a source-drain resistance in a TFT connected to a resistor must be decreased. Therefore, the increase in number of large-size TFTs makes a circuit area large. In comparative example 2, such large-size TFTs are not required.

In comparative example 1, a resistor consisting of polysilicon must be arranged. In case of the embodiment or comparative example 2, such a resistor is not required. On the other hand, in comparative example 2, wiring for charging or resetting a large number of capacitors is required, and a circuit area is increased. When a large-capacity capacitor for improving drive performance is included, the circuit size further increases. For this reason, comparative example 2 is limited to driving a liquid-crystal panel having a size of about 5" in diagonal length. In contrast to this, in case of the embodiment or comparative example 1, a large-size liquid-crystal panel or the like can be driven.

In consideration of a vertical size, when a circuit pitch is 0.15 mm, the digital driver circuit of the embodiment can be micropattemed to be about 3 mm in height. In contrast to

this, in comparative example 1, the vertical size is about 6 to 7 mm. In comparative example 2, the digital driver circuit can be micropattemed to be about 4.2 mm in vertical size.

Finally, in consideration of power consumption, to achieve the same drive performance, in comparative example 1, power consumption in the resistor is high, so that the power consumption of the circuit as a whole is also high. In the embodiment or comparative example 2, power consumption is low.

As described above, it is understood that the digital driver circuit of the embodiment is excellent from the viewpoints of drive performance, power consumption, and circuit area.

Embodiments of liquid-crystal devices serving as examples of electro-optical devices in which digital driver circuits according to the embodiments described above are built will be described below with reference to FIG. **15**, FIG. **16**, and FIG. **17**.

An embodiment of a liquid-crystal device shown in FIG. **15** comprises a liquid crystal held between a pair of substrates. Pixel electrodes **40** for applying voltages to liquid crystals in pixels arranged in the form of a matrix are arranged on a TFT array substrate **100** serving as one substrate. Drive signals from signal lines **41** are supplied as data signals to the pixel electrodes **40** through the sources and drains of TFTs **30** respectively arranged on the pixels. Scanning signals are supplied from the signal lines **41** to the gates of the TFTs **30**.

In the embodiment in FIG. **15**, a signal line drive circuit **101** has one shift register circuit **10** and a number of digital driver circuits **200** equal to that of the signal lines **41**. Each of the digital driver circuits **200** is the same as the digital driver circuit (see FIG. **2**) according to the first embodiment described above, so that the signal lines **41** are driven. Wirings for standard multi-ramp waves RAMP1 to RAMP8 are commonly connected to all the digital driver circuits **200**. For this reason, an amplifier for outputting these multi-ramp waves requires voltage supply performance for saturating the voltages of the plurality of signal lines **41**. However, since plural series of step-form multi-ramp waves are used as described above, time margins which are sufficient to electrically saturate the signal lines **41** with multi-ramp waves can be obtained.

The signal line drive circuit **101** is formed on the TFT array substrate **100**. As described above, each of the digital driver circuits **200** can be micropatterned to be about 3 mm in vertical size, even if the pixel pitch is 0.15 mm.

Another embodiment of a liquid-crystal device shown in FIG. **16** has a number of digital driver circuits **200'** equal to the number of signal lines **41** and each of the digital driver circuits **200'** is the same as one of the digital driver circuit (see FIG. **7**, FIG. **10**, and FIG. **12**) according to the second to fourth embodiments. Wirings for multi-ramp waves RAMP1 to RAMP4 and reference multi-ramp waves REF1 to REF4 are commonly connected to all of the digital driver circuits **200'**. Other portions of the liquid-crystal device in FIG. **16** are the same as that in the embodiment in FIG. **15**.

Still another embodiment of a liquid-crystal device shown in FIG. **17** comprises digital driver circuits **200A** (lower) and **200B** (upper) formed such that the digital driver circuits **200A** and **200B** are each one half of the digital driver circuit (see FIG. **2**) according to the first embodiment described above. More specifically, a lower signal line drive circuit **101A** has a shift resistor circuit **10A** and a number of digital driver circuits **200A** equal to that of even-numbered (numbers X2, X4, . . . , X2*n*) signal lines **41** and which are divided as described above, so that the even-numbered signal lines **41** are driven. An upper signal line drive circuit **101B** has one shift register circuit **10B** and a number of digital driver circuits **200B** equal to that of odd-numbered (numbers X1, X3, . . . , X2*n*−1) signal lines **41**, so that the odd-numbered signal lines **41** are driven. For this reason, each of the numbers of bits of the digital driver circuits **200A** and **200B** is set to be ½ (i.e., m/2 bits) the number of bits (i.e., m bits) of the digital driver circuit **200** according to the first embodiment.

In addition, in the liquid-crystal device according to the embodiment, a check circuit for performing predetermined types of electric characteristic checks during manufacturing of the liquid-crystal device or after the liquid-crystal device is manufactured is vertically divided by two, and the divided check circuits are arranged as a check circuit **210B** and a check circuit **210A** on the lower side and the upper side, respectively. Each of the check circuits **210A** and **210B** includes a plurality of analog switches **211**, e.g., TFTs and or the like, and a plurality of switch opening/closing control circuits **212**, e.g., TFTs or the like. When opening (disconnection), shortcircuit, or the like is checked through the even-numbered signal lines **41**, application of a predetermined voltage or measurement of a current is performed at checking terminals ANGoutT, ToutT, and TinT connected to the upper check circuit **210A**. On the other hand, when checking is performed through the odd-numbered signal lines **41**, application of a predetermined voltage or measurement of a current is performed at checking terminals ANGoutB, ToutB, and TinB connected to the lower check circuit **210B**.

Referring to FIG. **17**, capacitive lines **43** are arranged along the scanning lines **42** every pixel row for adding an accumulated capacity to the liquid-crystal pixels. However, in the embodiments of the liquid-crystal devices shown in FIGS. **15** and **16**, capacitive lines (not shown) are not arranged in the same manner as described above.

The liquid-crystal device according to the embodiment has a compact arrangement as a whole since the check and driver circuits are vertically divided. More specifically, since the digital driver circuit or the check circuit is divided, the number of elements included in each circuit is ½ that of a complete circuit. Therefore, in comparison with a case wherein these divided circuits are formed as one circuit, areas occupied by the circuits are respectively reduced, the elements can be arranged or wired with margins of the respective circuits.

In particular, with respect to an electro-optical panel, such as an liquid-crystal panel that has an image display region formed at the center and peripheral regions formed above and below the image display region, elements can be arranged or wired with well-balanced margins formed in the upper and lower peripheral regions.

The division performed as described above makes it possible to uniformly arrange circuits, and dead spaces on the device substrate can be effectively used. For example, in the case of a liquid-crystal panel, a dead space located immediately below a sealing material for sealing a liquid crystal between both of a pair of substrates adhered to each other can be practically used. More specifically, since the sealing material is formed to be in contact with the peripheries of the substrates with uniform widths such that excessive stress does not act on the substrates, the numbers of elements in the circuits are reduced by dividing the circuits, and the circuits may be uniformly arranged in the region located immediately below the sealing material.

In an electro-optical panel of this type, a pitch of circuit elements in one direction along a scanning line is especially limited.

Since the size of the check circuit is smaller than the element size of the digital driver circuit, further space saving can be achieved by dividing the check circuit, and an advantage on layout design can be obtained.

In addition, since the number of stages of the shift registers **10A** and **10B** is half of that in the first embodiment, an operation frequency also becomes ½, and an advantage in circuit design can be obtained.

In FIG. **17**, when the phases of upper multi-ramp waves RAMP1T to **8T** and the phases of lower multi-ramp waves RAMP1B to **8B** are shifted from each other by 180°, dot inversion drive can be performed. For this reason, flicker or the like of a display image can be prevented, and the liquid crystal can also be prevented from being degraded by applying a DC voltage.

According to the embodiments of the liquid-crystal devices shown in FIGS. **15** to **17**, even if the image display regions are increased in size, the liquid-crystal devices can be driven, the ratio of the image display regions to the device bodies can be increased, and power consumption can be lowered. In addition, γ-correction can also be accurately performed by adjusting the voltage values of multi-ramp waves.

Each of the embodiments of the liquid-crystal devices shown in FIG. **15** to FIG. **17** is formed as a liquid-crystal device comprising the TFTs **30** as switching elements in respective pixels and using a TFT active matrix drive scheme. However, various switches, logical circuits, and the like (see FIG. **2**, FIG. **7**, FIG. **10**, and FIG. **12**) included in the digital driver circuits **200** can be preferably replaced with TFTs. More specifically, various elements can be formed as a whole device by a thin film forming technique, so that an advantage in manufacturing can be obtained.

Embodiments of electronic apparatus including the liquid-crystal devices described above will be described below with reference to FIG. **18** to FIG. **22**.

A schematic block diagram of an electronic apparatus including the liquid-crystal device as described above is shown in FIG. **18**.

Referring to FIG. **18**, the electronic apparatus comprises a display information output source **1000**, a display information processing circuit **1002**, a display circuit **1004**, a liquid-crystal panel **1006**, a clock generation circuit **1008**, and a power supply circuit **1010**. The display information output source **1000** includes a memory, such as a ROM (Read Only Memory), a RAM (Random Access Memory), or an optical disk device and a tuning circuit or the like for tuning a television signal to output the tuned television signal, and outputs display information, such as an image signal having a predetermined format to the display information processing circuit **1002**. The display information processing circuit **1002** includes various known processing circuits such as an amplification-polarity inversion circuit, a phase development circuit, a rotation circuit, a gamma-correction circuit, and a clamping circuit, and sequentially generates digital signals from the display information input on the basis of the clock signal to output the digital signals to the display circuit **1004** together with a clock signal CLK. The display circuit **1004** corresponds to the digital driver circuit in each of the embodiments described above to drive the liquid-crystal panel **1006**. The power supply circuit **1010** supplies predetermined power signals to the respective circuits described above. The display circuit **1004** may be mounted on a TFT array substrate of the liquid-crystal panel **1006** along with the display information processing circuit **1002**.

Examples of the electronic apparatus arranged as described above are shown in FIG. **19** to FIG. **22**.

Referring to FIG. **19**, a liquid-crystal projector **1100** includes three liquid-crystal modules each including the liquid-crystal panel **1006** having the display circuit **1004** mounted on the TFT array substrate that are part of light values **100R**, **100G**, and **100B** for RGB light. In the liquid-crystal projector **1100**, when projection light is emitted from a lamp unit **1102** such as a metal halide lamp, the projection light is divided into light components R, G, and B corresponding to the three primary colors of RGB by three mirrors **1106** and two dichroic mirrors **1108**. The light components R, G, and B are guided to the light values **100R**, **100G**, and **100B** corresponding to the colors, respectively. In this case, in particular, B light is guided through a relay lens system **1121**, which includes an incident lens **1122**, a relay lens **1123**, and an emission lens **1124** to prevent light loss caused by a long optical path. The light components corresponding to the three primary colors respectively modulated by the light valves **100R**, **100G**, and **100B** are synthesized with each other by a dichroic prism **1112**, and the synthesized light is projected on a screen **1120** through a projection lens **1114** as a color image.

In this embodiment, in particular, when a light-shielding layer is also arranged on the lower side of a TFT, even if part (part of R lightand G light) of the light passing through the liquid-crystal panel and penetrating the dichroic prism **1112** is reflected to the TFT array substrate as return light, light shielding for the channel of a switching TFT or the like of a pixel electrode can be sufficiently performed. In this case, even if a prism suitable for reduction in size is used in the projection optical system between the TFT array substrate and the prism of each liquid-crystal panel, an AR filn for preventing return light need not be adhered, or a polarizing plate need not be subjected to an AR coating process. For this reason, the embodiment is considerably advantageous to achieve a compact and simple arrangement.

Referring to FIG. **20**, a multimedia laptop personal computer (PC) **1200** includes the liquid-crystal panel **1006** described above in a top cover case. In addition, the personal computer **1200** includes a main body **1204** which incorporates a CPU, a memory, a MODEM, and the like and in which a keyboard **1202** is built.

Referring to FIG. **21**, a pager **1300** includes a liquid-crystal panel **1006** and display circuit **1004** mounted on a TFT array substrate that form a liquid-crystal module incorporated in a metal frame **1302** together with a light guide **1306**, backlight **1306***a*, a circuit board **1308**, first and second shield plates **1310** and **1312**, two elastic conductors **1314** and **1316**, and a film carrier tape **1318**. In this example, the display information processing circuit **1002** described above (see FIG. **18**) may be mounted on the circuit board **1308**, or may be mounted on the TFT array substrate of the liquid-crystal panel **1006**. In addition, the display circuit **1004** described above can also be mounted on the circuit board **1308**.

Since the example shown in FIG. **21** is a pager, the circuit board **1308** and the like are also included. However, when the display circuit **1004** or the display information processing circuit **1002** is also mounted to the liquid crystal panel **1006** to form a liquid-crystal module, a device in which the liquid-crystal panel **1006** is fixed in the metal frame **1302** can also be produced, sold, and used as a liquid-crystal device or a backlight liquid-crystal device in which the light guide **1306** is additionally built.

As shown in FIG. **22**, the liquid-crystal panel **1006** does not include the display circuit **1004** or the display informa-

tion processing circuit **1002**. Instead, an IC **1324** including the display circuit **1004** or the display information processing circuit **1002** is physically and electrically connected to a TCP (Tape Carrier Package) **1320** packaged on a polyimide tape **1322** through an anisotropic conductive film formed on a peripheral portion of a TFT array substrate **100**. The resultant device can also be produced, sold, or used as a liquid-crystal device.

In addition to the electronic apparatuses described with reference to FIG. **19** to FIG. **22**, a liquid-crystal television, a viewfinder type or direct-vision type video cassette recorder monitor, a satellite navigation system, an electronic organizer, a calculator, a wordprocessor, an engineering workstation (EWS), a portable telephone set, a television telephone set, a POS terminal, a device having a touch panel, and the like are used as examples of the electronic apparatus shown in FIG. **18**.

As described above, according to the embodiments, various electronic apparatuses comprising large-size liquid-crystal devices having low power consumption can be realized.

According to the digital driver circuit of the present invention, when selection of a series of standard multi-ramp waves and selection of a voltage are combined to each other, drive signals corresponding to the value of digital image signals are generated. For this reason, the accuracies of timings required for the respective standard multi-ramp waves are considerably reduced. In addition, even if an amplifier for supplying the standard multi-ramp waves has low performance, a time margin which is sufficient to saturate a signal line with the voltage of a drive signal can be assured. As a result, according to the digital driver circuit of the present invention, drive performance can be improved by using a circuit having a relatively low through rate while keeping power consumption low, and temperature compensation or γ-correction can be relatively easily performed at a high accuracy.

What is claimed is:

1. A driver circuit for an electro-optical device that receives an n-bit (n is a natural number not less than 2) digital image signal supplied from n bit lines, generates an analog drive signal corresponding to the digital image signal, and outputs the analog drive signal to a signal line comprising:

a series selection circuit that selects at least one series from plural series of standard multi-ramp waves, having voltages that change in steps with a passage of time, according to the n-bit digital image signal; and

a time selection circuit that selects a time of at least one of the selected series of standard multi-ramp waves and a wave based on the selected series of standard multi-ramp waves to generate at least one voltage, the time selection circuit having a PWM circuit that generates pulse signals having different pulse widths, and the series selection circuit having a decoder that decodes at least one portion of the digital image signal.

2. A driver circuit for an electro-optical device that receives an n-bit (n is a natural number not less than 2) digital image signal supplied from n bit lines, generates an analog drive signal corresponding to the digital image signal, and outputs the analog drive signal to a signal line comprising:

a series selection circuit that selects at least one series from plural series of standard multi-ramp waves, having voltages that change in steps with a passage of time, according to the n-bit digital image signal;

a time selection circuit that selects a time of at least one of the selected series of standard multi-ramp waves and a wave based on the selected series of standard multi-ramp waves to generate at least one voltage;

a voltage change circuit that changes at least one of the generated voltage and a voltage based on the generated voltage, the voltage change circuit comprising an SC-DAC (Switched Capacitor–Digital to Analog Converter) circuit;

an inversion circuit that inverts a digital value of at least one portion of the digital image signal for input to the SC-DAC circuit, the SC-DAC circuit performing voltage subtraction by charge sharing depending on the inverted portion.

3. A method for driving an electro-optical device, comprising:

selecting at least one series from plural series of standard multi-ramp waves, having voltages that change in steps with a passage of time, according to an n-bit digital image signal; and

selecting a time of at least one of the selected series of standard multi-ramp waves and a wave based on the selected series of standard multi-ramp wave to generate at least one voltage; and

generating a pulse width modulated signal.

4. A method for driving an electro-optical device, comprising:

selecting at least one series from plural series of standard multi-ramp waves, having voltages that change in steps with a passage of time, according to an n-bit digital image signal;

selecting a time of at least one of the selected series of standard multi-ramp waves and a wave based on the selected series of standard multi-ramp wave to generate at least one voltage;

changing the generated voltage;

inverting a digital value of at least one portion of the digital image signal; and

performing voltage subtraction by charge sharing based on the inverted value.

5. A method for driving an electro-optical device, comprising:

selecting at least one series from plural series of standard multi-ramp waves, having voltages that change in steps with a passage of time, according to an n-bit digital image signal;

selecting a time of at least one of the selected series of standard multi-ramp waves and a wave based on the selected series of standard multi-ramp wave to generate at least one voltage;

changing the generated voltage; and

performing one of charge sharing and charge pumping using the generated voltage and a selected reference voltage.

6. A driver circuit for an electro-optical device that receives an n-bit (n is a natural number not less than 2) digital image signal supplied from n bit lines, generates an

analog drive signal corresponding to the digital image signal, and outputs the analog drive signal to a signal line comprising:

a series selection circuit that selects at least one series from plural series of standard multi-ramp waves, having voltages that change in steps with a passage of time, according to the n-bit digital image signal;

a time selection circuit that selects a time of at least one of the selected series of standard multi-ramp waves and a wave based on the selected series of standard multi-ramp waves to generate at least one voltage;

a voltage change circuit that changes at least one of the generated voltage and a voltage based on the generated voltage, the time selection circuit receiving digital values corresponding to a first bit to an m-th bit ($1 \leqq m < p < n$, m and p are natural numbers), the series selection circuit receiving digital values corresponding to an m+1-th bit to a p-th bit, and the voltage change circuit receiving digital values corresponding to a p+1-th bit to the n-th bit.

* * * * *